The Run IIb CDF Detector Upgrade Project

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The CDF Run IIb project exists to keep the experiment vital during high luminosity operation.

Originally, the project was motivated by both high integrated and instantaneous luminosity.

- Reduced integrated luminosity projections reduced the motivation for the silicon detector, resulting in its cancellation.

- Design goal instantaneous luminosity projections are still ~3×10^{32} cm^{-2}s^{-1}
  - Now at 396 ns crossing – higher occupancies than planned

- Portions of the project motivated by instantaneous luminosity are still needed and have been retained
Run IIb Project Scope

- Calorimeter Upgrades
  - Preshower Upgrade
  - Electromagnetic Timing

- Data Acquisition and Trigger Upgrades
  - TDCs for the drift chamber
  - Level 2 Decision crate
  - Fast track trigger Upgrade
  - Event Builder Upgrade
  - Level 3 computer upgrade
  - Silicon Vertex Trigger upgrade

11 November 2004
The preshower upgrade replaces the older gas chamber system with scintillator.

- Fiber/multichannel PMT readout – similar to what’s used on the endplug.

Significant foreign contribution here

- PMT from Japan
- Scintillator/fibers from Italy
System was planned for an assembly hall installation in FY 2006

Schedule was adapted to accommodate accelerator shutdowns
- Accelerated production of scintillator tiles, modules
- Procurement of PMTs by Tsukuba was advanced
- The project targeted Fall 2004
  - Shutdown for 2005 projected to be shorter

11 November 2004
Calorimeter Installation

- Preshower installation involves detector installation on the inner surface of the calorimeter
  - Never serviced in the collision hall previously.
- Phototube and cables are installed on the back.
- All parts but optical fibers were available by Sep. 2004

- All scaffolds, detector elements, people, passed through this opening.
Preshower/Crack Installation

Stefano Moccia
The fourth arch was replaced into operating position on 8 Nov. 2004. All front face work is done.

The CPR is now being incorporated into the full data stream

- Tile response measured at Argonne, PMT gain measured at Tsukuba
- Light yield is well above the specification.
- Gains are well understood at this stage – 13% spread
- CPR is 99.7% live. Remaining problems are electronics

The system is installed and working
CPR occupancy

- A cosmic ray run of the CPR system

11 November 2004
The electromagnetic timing upgrade splits a small portion of the phototube signal off for timing:

- Reduces cosmic ray or halo backgrounds for photons

Entire system was installed during the fall 2004 shutdown. Cosmic ray commissioning is in progress.
### DAQ/Trigger Specification

#### Run IIa vs IIb

<table>
<thead>
<tr>
<th></th>
<th>Run IIa Specification</th>
<th>Run II Achieved</th>
<th>Run IIb Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Luminosity</td>
<td>8.6x10^{31}</td>
<td>1x10^{32}</td>
<td>3x10^{32}</td>
</tr>
<tr>
<td>L1 Accept</td>
<td>45 kHz</td>
<td>25 kHz</td>
<td>30 kHz</td>
</tr>
<tr>
<td>L2 Accept</td>
<td>300 Hz</td>
<td>400 Hz</td>
<td>1000 Hz</td>
</tr>
<tr>
<td>Event Builder</td>
<td>75 MB/s</td>
<td>75 MB/s</td>
<td>500 MB/s</td>
</tr>
<tr>
<td>L3 Accept</td>
<td>75 Hz</td>
<td>80 Hz</td>
<td>100 Hz</td>
</tr>
<tr>
<td>Rate to Storage</td>
<td>20 MB/s</td>
<td>20 MB/s</td>
<td>40 MB/s</td>
</tr>
<tr>
<td>Deadtime Trigger</td>
<td>5%</td>
<td>10%</td>
<td>5% + 5% †</td>
</tr>
</tbody>
</table>

- Run IIa L1A not achieved due to higher than specified Silicon Readout + L2 Trigger execution times
- † Assume ~5% from readout and ~5% from L2 processing
- Reminder: IIb trigger & bandwidth rates estimated based upon Run IIa, significant underestimate possible (assumes linear growth in fake contribution)

11 November 2004
Trigger/DAQ Upgrades for Run IIb

- COT TDC upgrade
  - Original readout rate insufficient
- COT Track Trigger Upgrade
  - L1 trigger rate reduction needed
  - Complexity of events (occupancy)
- Silicon Vertex Trigger upgrade
  - Occupancy demands processing speed
- L2/L3 trigger upgrades
  - Processing speed/modernization
- Event builder upgrade
  - Processing speed upgrade needed
  - Level 2 accept rate is insufficient

11 November 2004
Run IIa TDC Limitations (2002)

- On-board processing (DSP)
  Time grows with # of hits
  - \( t = 1200\mu s/\text{event} \) for SL1 (4 hits/ch) at \( 4 \times 10^{32} \text{ cm}^{-2}\text{s}^{-1} \)

- VME Readout
  - Read sequentially by one block transfer (~14MB/s at high lum.)

- VME – Event builder link limited to 12 MB/s

- 2002 Internal review recommended replacement
Run IIb TDC

- **840MHz Diff LVDS inputs**
- **TDC**: Serial to 10bit parallel conversion (1.2ns/bit)
- **L1/L2 Buffering, hit processing + Readout (CBLT)**
- **XFT Hit Generation**

**Altera Stratix FPGAs** (48chan/chip)

**Input Connectors And LVDS Repeaters**

**DC Power convertors**

**VME Interface**

**CDF Clock and Control Interface**

**Trigger Output Drivers (to XFT)**
TDC Performance Reviews

- **Run 2a TDC**
  - DSP execution now about factor of 2 faster than in 2002
  - New compressed data format (based in Run 2b TDC), halves the data volume.
  - Measured performance with 3 hits/channel of 5% deadtime at 1kHz
  - Need to implement Fast Clear on TDCs in SL5,6 (already on SL1-4) to keep these from taking longer than SL1
  - **Meets the Run 2b readout specification**

- **Run 2b TDC**
  - 5 preproduction boards received in September pass tests
  - Implemented 64 bit VME transfer (was 32bit like rest of FE/Trig)
    - In bench tests 18MB/s (32bit VME) → 36MB/s
    - Can achieve 2kHz with less than 5% deadtime
  - **Exceeds all Run 2b specifications**

11 November 2004
Future TDC Plans

- The review committee recommended retaining the current TDCs for the remainder of the run.
- This was motivated by the perceived risk associated with commissioning a new system.
  - Installation time will require an 8 week shutdown, followed by commissioning period during Tevatron operations.
- Some modifications of the current TDCs are needed (outer layer modules).
- Final testing of new TDCs will document their performance.
Run IIa Level 2 Decision Crate

- 6 flavors of interface board
  - (XTRP, SVT), L1, ISO, MUON, CES, Cluster
  - each uses different input format, different board designs
- 1 board with Alpha processor for L2 processing/decision
  - system designed to run with 4 Alphas
  - Data input with custom bus (MagicBus)
- Diversity makes system challenging to test & maintain
- DEC α processors obsolete
- Did not achieve design execution time
- CDF internal review recommended replacing Alphas for Run IIb
- Upgrade with PULSAR board as universal interface

11 November 2004
Level 2 Status

- All hardware has been procured for the Level 2 upgrade.
- Testing with beam occurred in summer 2004
  - Parasitic operation, trigger decisions, can be tested without disruption of operations
- Installation review in Sep. identified the “to do” list
- Expect system to be in full operation by March 2005.
Run IIa XFT Configuration

Ansley trigger cable (220 ft) ~2 m copper Cable Data Neighboring cards
Data @45MHz LVDS @33MHz (channel link) connected over backplane

168 TDC from COT axial layers
24+24 Axial Finders
24 Linkers
24 LOMs

24 crates 3 crates 3 crates

TDC Hits Binned into 2 bins: “Prompt” and “Delayed”

~10 m of cable to XTRP

11 November 2004
Original XFT Upgrade

Ansley trigger cable (220 ft)
Data @45MHz LVDS

~2 m copper Cable Data
@33MHz (channel link)

Neighboring cards
connected over backplane

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168 TDC from COT axial layers

24 crates

24+24 New Axial Finders

3 crates

24 New Linkers

3 crates

24 LOMs

~10 m of cable to XTRP

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New TDC or XTC for stereo layers

1 crate

12 Stereo Finders SL7

1 crate

Styro Association Modules

- Retain cable infrastructure
- 4 Layers → 5 layers (add SL7)
- Finer resolution input to all
XFT II Scope Reviews

- Two CDF reviews (5/21 and 6/21) to evaluate performance and scope of the XFT upgrade and recommend course of action.
  - Hardware progress was slow
  - Not enough good Ansley cables (TDC to XFT) to instrument stereo SL7
- Significant progress in simulation since Fall 2003.
  - Reproduces trigger rates of recent higher luminosity operation
  - Performance degradation of IIa system smaller than original projections
- Committee Conclusions
  - Simulations demonstrate that original XFT upgrade can achieve goals
  - However, original XFT upgrade no longer feasible, given the time available to complete and commission the project.
  - Consensus (Committee, XFT proponents, Run IIb management) that addition of more stereo (SL 3, 5 and 7) is the most reasonable course.
Revised XFT Upgrade

Ansley trigger cable (220 ft)
Data @45MHz LVDS

168 TDC from COT axial layers
24 crates

XTC

24+24 Axial Finders
3 crates

4 Superlayers → 7 Superlayers
3 Layer Stereo tracking
Finer resolution input to Stereo
Allows parasitic testing

24 Linkers
3 crates

24 SLAMs
2 crates

New cable (~150ft)
Optical Data
~45MHz

12+12+12 Stereo Finders
SL3+5+7
2 crates

~10 m of cable to XTRP

New TDC or XTC for stereo layers

~3m optical Cable
@60.6MHz

5 Stereo Pulsars in L2 Decision Crate

Data to L2
XFT Hardware Progress

- Prototype XTC under test at Illinois and FNAL since July
  - Tested w/2 time bin and 6 time bin firmware
  - Production review Nov 12
  - Start fabrication by December

- Prototype TDC transition board and fiber transmitter mezzanine card (Illinois) under test at Illinois
  - Mezzanine card also used on finder for SLAM and L2 connections

- Target data for completion is the August, 2005
  - These components require collision hall installation

11 November 2004
XFT Hardware Progress

- **Stereo Finder (Fermilab)**
  - Schematics and layout complete, design review Nov 5
  - Parts in hand, out for fabrication/assembly by Dec 1
  - Most functionality for Finder FPGA firmware complete

- **Stereo Linker Association Module (SLAM - OSU)**
  - Schematics and layout complete, design review Sept 24
  - Parts ordered, Out for fabrication this week
  - Implemented “Pass-through” firmware

- These items are in the counting room
  - Commissioning can be largely parasitic to operations.
SVT Upgrade for SVXII

- New AM++ hardware with narrower roads (32K to 512K) reduces number of tracks to fit
  - Developed by Pisa, bought by INFN
- New AMSequencer/Road Warrior (12 Pulsars)
  - Interface for AM++
- New Hit Buffer (12 Pulsars)
- Faster Track Fitters reduce processing time on found roads (12 Pulsars)

Note 12 Pulsars will be “recycled” from current use as “Road Warrior” boards
SVT Progress

- AM++ (not on project funds) at INFN
  - Testing of new AM chips progressing - Low yield may require an additional production run. Should not be a significant project delay.
  - AM++ and LAMB mezzanine boards passed printed circuit board review Nov 3.
- Hardware for AMS/RW, HB, TF defined:
  - Quote request for 34 Pulsar boards (includes XFT) issued by Chicago
  - Design of two 2 Pulsar mezzanine boards (memory) at Chicago
    - First passed design review Nov 2, prototype parts in hand, board fabrication in progress
    - Design of second started should be ready for prototype by end of 2004
- Firmware making good progress
  - AMS/RW firmware making good progress at Pisa
  - TF firmware largely transferred from existing design to Pulsar
- Note, this installation is decoupled from collision hall access.

11 November 2004
Run IIb Event Builder Upgrade

<table>
<thead>
<tr>
<th></th>
<th>Run IIa</th>
<th>Run IIb</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rate:</td>
<td>300Hz</td>
<td>1kHz</td>
</tr>
<tr>
<td>Event size:</td>
<td>250kB</td>
<td>500kB</td>
</tr>
<tr>
<td>Throughput:</td>
<td>75MB/s</td>
<td>500MB/s</td>
</tr>
</tbody>
</table>

**SCPU:** MVME2600        VMIC7805

**SCPU OS** VxWorks       Linux

**Switch:** ATM           Cisco 6509 (gigabit ethernet)

- New Cisco 6509 switch
- New software (much less than IIa)
- New VMIC 7805 boards (SCPUs)
Event Builder

- Hardware in hand (ahead of schedule)
- Software development and testing on schedule for installation in Aug 05
  - No collision hall access is required, but installation will require down time for the experiment.
CDF Upgrade Conclusions

- Calorimeter - **installations are complete**
- DAQ/Trigger projects are making good progress
  - New direction on TDCs – improvements in the current device and the installation risk motivate a new strategy.
  - Level 2 – entering the final integration phase
  - Track triggers (XFT and SVT) are beginning construction
    - Both have simplified their design recently
  - Event builder hardware is in hand, and software is in progress.
- All projects are targeting completion/installation by the end of FY 2005.

11 November 2004