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# **Magnetic Compression Circuits and Kicker Drive Options**

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**March 9, 2002**

# Kicker Pulsar Options

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## ✧ **Magnetic Circuit/Systems**

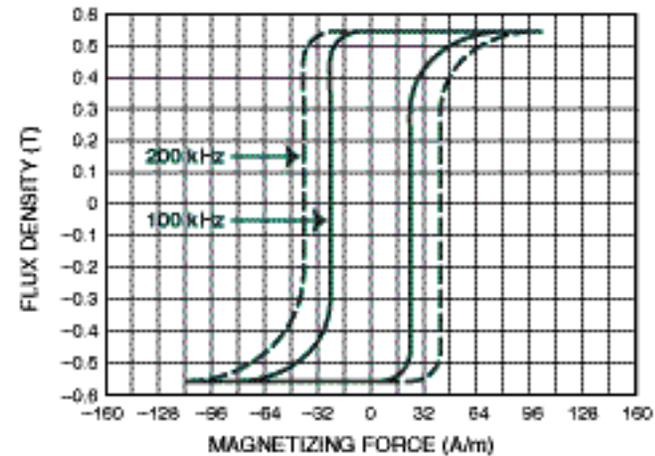
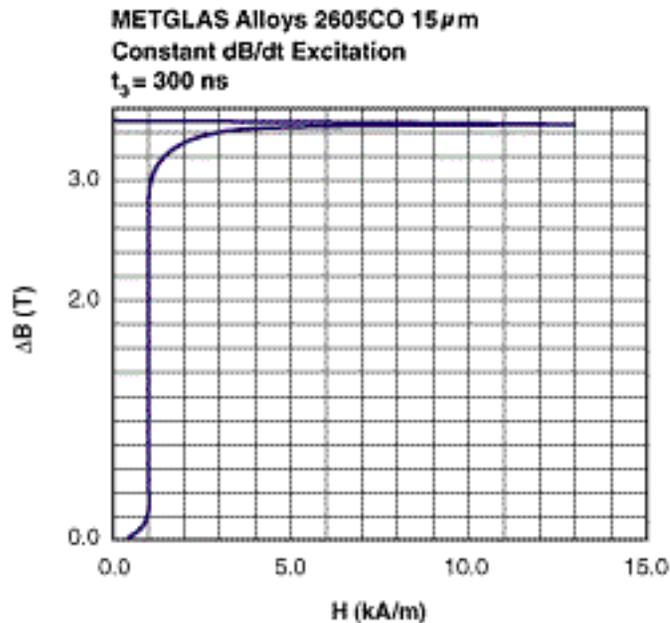
- **Basics**
- **Relevant Equations**
- **Limitations**
- **Examples of Operational Systems**
- **References**

## ✧ **Adder Circuits**

- **Concept**
- **Examples of Operational Systems**

# Magnetic Switch Principles

- ✧ A magnetic switch is a device, usually constructed as a winding around a magnetic core, that uses the non-linear properties of magnetic materials to achieve a large change in impedance
- ✧ The impedance of a magnetic switch varies from a large inductance (magnetic core unsaturated) to a small inductance (magnetic core saturated)

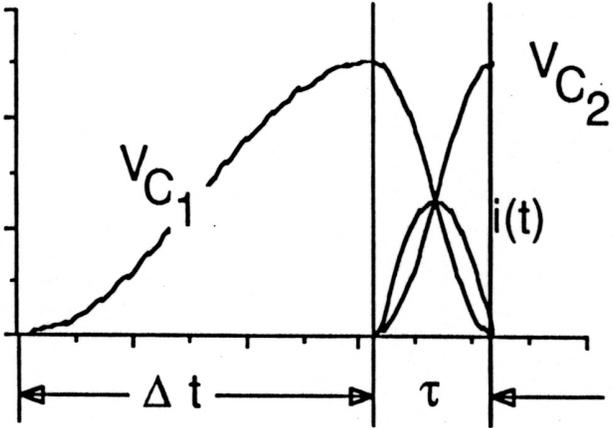
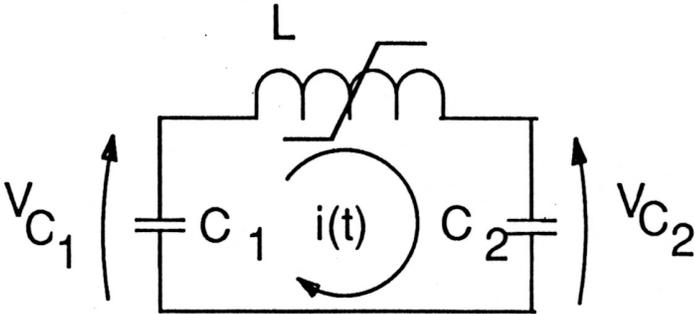


# Definition of Terms

Term	Definition	Units
$L_n$	the $n^{\text{th}}$ stage of magnetic compression	
$Vol_n$	minimum magnetic core volume of $L_n$	meters <sup>3</sup>
$A_n$	magnetic cross-sectional area of $L_n$	meters <sup>2</sup>
OD	outer diameter of magnetic core (toroid)	meters
ID	inner diameter of magnetic core (toroid)	meters
$\mu_s$	saturation magnetic flux density	tesla
$N_n$	number of turns on the $L_n$ winding	
$w_n$	axial length of $L_n$ winding	meters
$r$	radial thickness of magnetic core	meters
$\langle r \rangle$	mean radius of magnetic core	meters
pf	packing factor - cross-section area of magnetic material divided by total area enclosed by windings	
$L_n^{\text{sat}}$	saturated inductance of $L_n$	henries
$G_{in_n}$	ratio of charge to discharge inductor for $L_n$	
$C_n$	capacitance at the input of $L_n$	farad
$E_{C_n}$	per pulse energy stored on $C_n$	joules
$\langle V_{C_n} \rangle$	average charge voltage on capacitor $C_n$	volts
$\tau_{C_n}^{\text{chg}}$	time required for capacitor $C_n$ to charge to peak voltage	second
$\tau_{L_n}^{\text{sat}}$	hold-off time - time required to saturate $L_n$ at given average charge voltage	second
$t_{\text{pro}}$	total propagation delay through the modulator - equal to the sum of the hold-off time of all the stages	second
$\mu_0$	free space permeability = $4 \times 10^{-7}$	henries m/amp <sup>2</sup>
$\mu_r$	relative permeability	
$\mu_r^{\text{sat}}$	saturated value of relative permeability	
$\langle \mu_r^{\text{sat}} \rangle$	average relative permeability during saturation	
$\sigma$		
$\Delta t$	time jitter	second
$\Delta V$	pulse-to-pulse variations in pulse charge voltage	volts

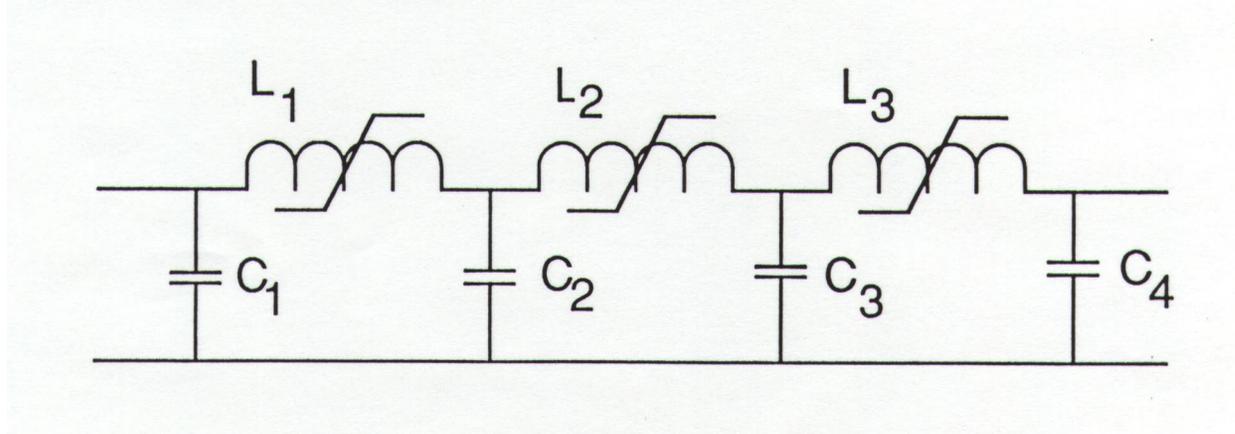
# Magnetic Switch Operation

- The Magnetic Switch is designed to saturate at the voltage peak on  $C_1$  and transfer all the stored energy to  $C_2$



$$\text{GAIN} = \frac{\Delta t}{\tau}$$

# Magnetic Compression Circuits



- ❖ **To achieve higher overall gain, multiple switches may be used**
  - **Switches are designed to saturate sequentially**
  - **Multiplying individual switch gains yields the overall gain**
- ❖ **Capabilities of magnetic compression systems**
  - **High repetition rate**
  - **High average power**
  - **Very high peak power**
  - **High reliability**
- ❖ **Note: A “real” switch (one that can be controlled by external trigger is required to initiate the magnetic compression sequence**

# Basic Compression Circuit Equations

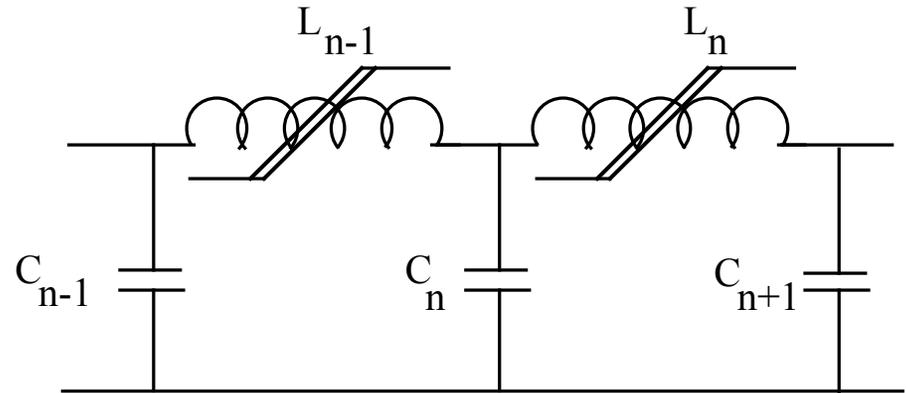
$$\tau_{C_n}^{chg} = \pi \sqrt{L_{n-1}^{sat} C_{eq}} = \pi \sqrt{L_{n-1}^{sat} \frac{C_n}{2}}$$

$$\frac{L_{n-1}^{sat}}{L_n^{sat}} = \left( \frac{\tau_{C_n}^{chg}}{\tau_{C_{n+1}}^{chg}} \right)^2 = Gain_n^2$$

$$\tau_{C_n}^{chg} \approx \tau_{L_n^{sat}} = \frac{N_n A_n \Delta B_s}{\langle V_{C_n} \rangle}$$

$$Gain_n^2 = \frac{2 \Delta B_s^2 A_n^2}{10^{-7} \pi^2 \mu_r^{sat} \omega_n \ln \left( \frac{OD}{ID} \right) E_{C_n}}$$

$$Vol_n \approx \frac{Gain_n^2 E_{C_n} \pi^2 \mu_r^{sat} \mu_o}{4 \Delta B_s^2}$$



**Note: The capacitors are usually equal in value**

# Magnetic System Limitations - Jitter

- ❖ Time Jitter - caused by variations of voltage and  $\Delta B$  as per:

$$\tau_{C_n}^{chg} \approx \tau_{L_n}^{sat} = \frac{N_n A_n \Delta B_s}{\langle V_{C_n} \rangle}$$

- Jitter is proportional to the total propagation delay through the magnetic system (sum of the individual switch hold-off times)
    - Example: If the total propagation delay is  $10\mu s$  and the average input voltage variation is 1% the minimum time jitter ( $\Delta B$  variation is zero) is:
      - $\Delta t \sim 10\mu s \cdot 0.01 = 100ns$
  - Jitter can be minimized by:
    - Precisely resetting the magnetic cores prior to the next pulse
    - Precise voltage regulation or real-time adjustment of trigger pulse to compensate for  $\Delta V$
- ❖ Jitter of  $< \pm 2ns$  can be reasonably anticipated for systems having propagation delays  $< 10 ns$

# Magnetic System □ Limitations - Risetime & Repetition Rate

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- ✧ **Risetime:** the pulse risetime is determined by the saturated inductance of the winding geometry. It is possible to obtain single turn inductance in the nH range. In practice, output risetimes in the range of 10-20 ns are routinely achieved for high voltage systems
  
- ✧ **Repetition Rates:**
  - **Burst Repetition Rate**
    - Parallel systems (Branch Magnetics) can operate at 10's of MHz
    - Single pass systems can probably work up to ~ 100 kHz (the limitation is that all the magnetic cores need to be reset between pulses)
  - **Constant Repetition Rate**
    - Single pass systems can operate into the 10-20 kHz region (liquid cooling is required to remove heat generated in the magnetic cores and capacitors)
      - Metglas™ is limited to < 5 kHz for the fastest saturation rates (output stages) but may easily be used for earlier stages. Another limitation of Metglas™ at fast saturation rates (high  $\frac{dB}{dt}$ ) is voltage breakdown between laminations
      - Ferrites are often used for the output stages in high rep-rate systems

# Magnetic System □ Limitations - Number of Stages

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- ✧ The total gain required by the system determines the number of stages where the total gain is the product of the individual switch gains

- Individual switch gain is restricted by the core volume relationship:

$$Vol_n \approx \frac{Gain_n^2 E_{C_n} \pi^2 \mu_r^{sat} \mu_o}{4 \Delta B_s^2}$$

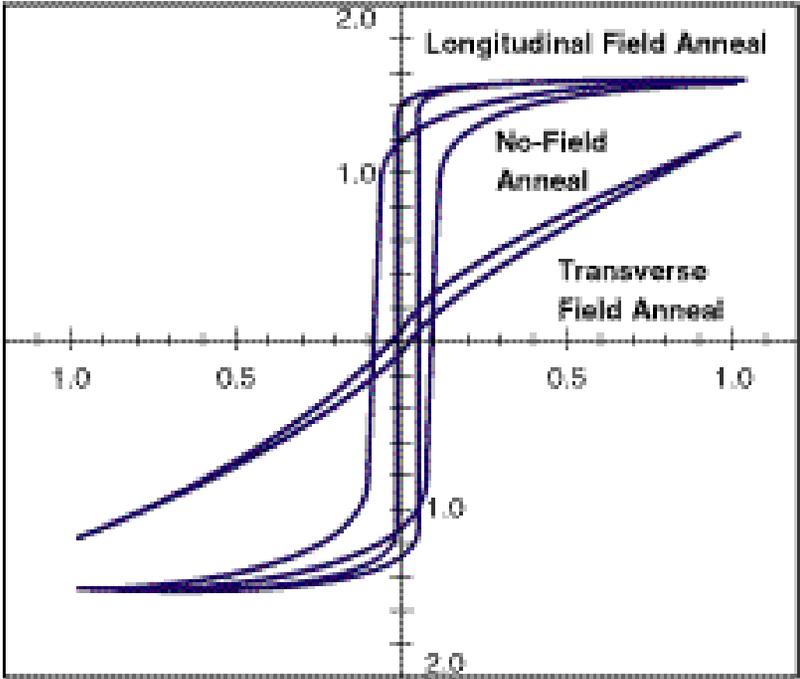
- Maximum reasonable core gain:

- ~ 3 for ferrite
- 5-10 for Metglas™ and other amorphous materials

- ✧ When more than two switches are required, a step-up transformer is normally needed (eliminates trying to design fractional turn switches)
- ✧ Usually only 3 magnetic switches are required to cover the range of microseconds (initial conduction time) to nanoseconds (output risetime)

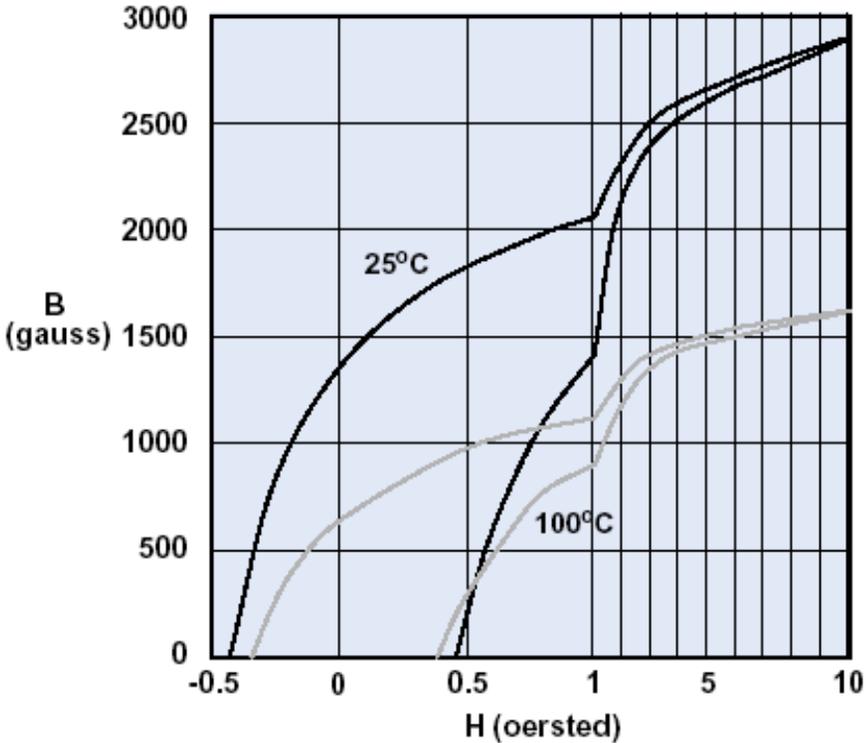
# B-H Loops for Metglas™ and Ferrite Cores

MAGNETIC INDUCTION-B-TESLAS



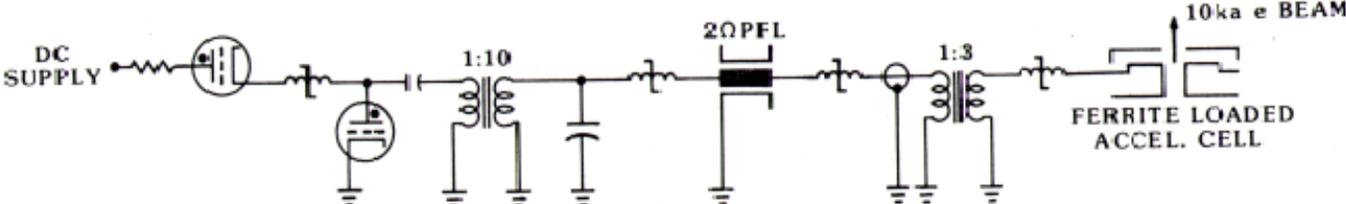
MAGNETIZING FORCE-H-OERSTEDS

Hysteresis Loop

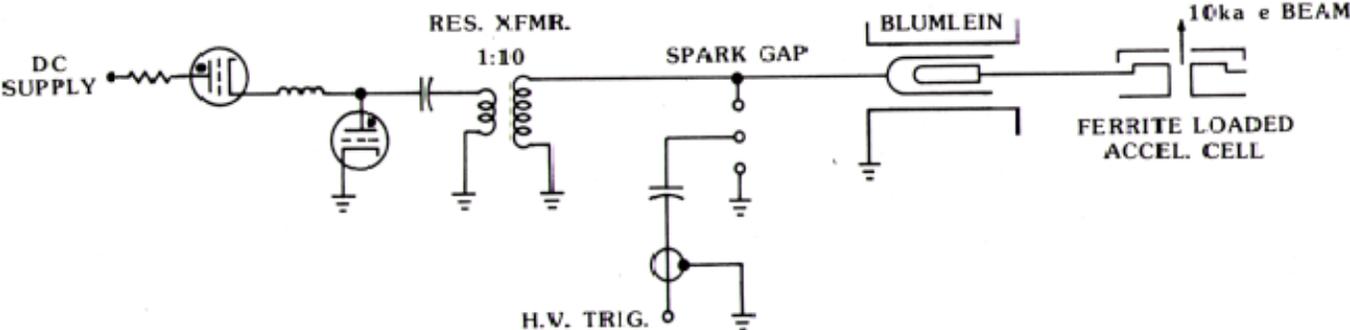


# Circuit Schematics - ATA Sparkgap Triggered vs. Magnetic Compression System

INDUCTION LINAC NONLINEAR MAGNETIC DRIVE

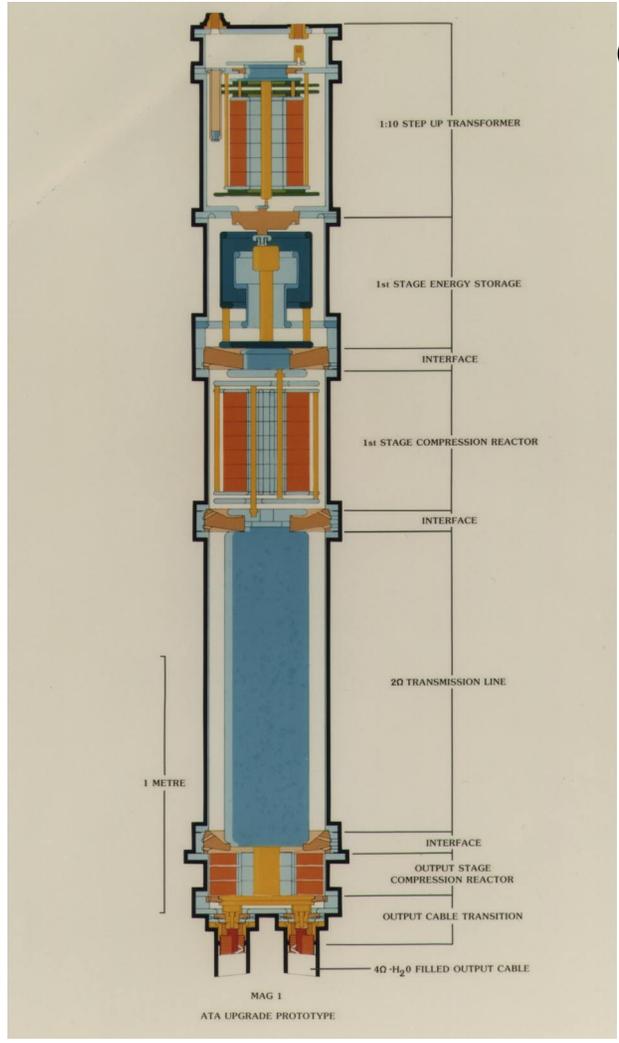
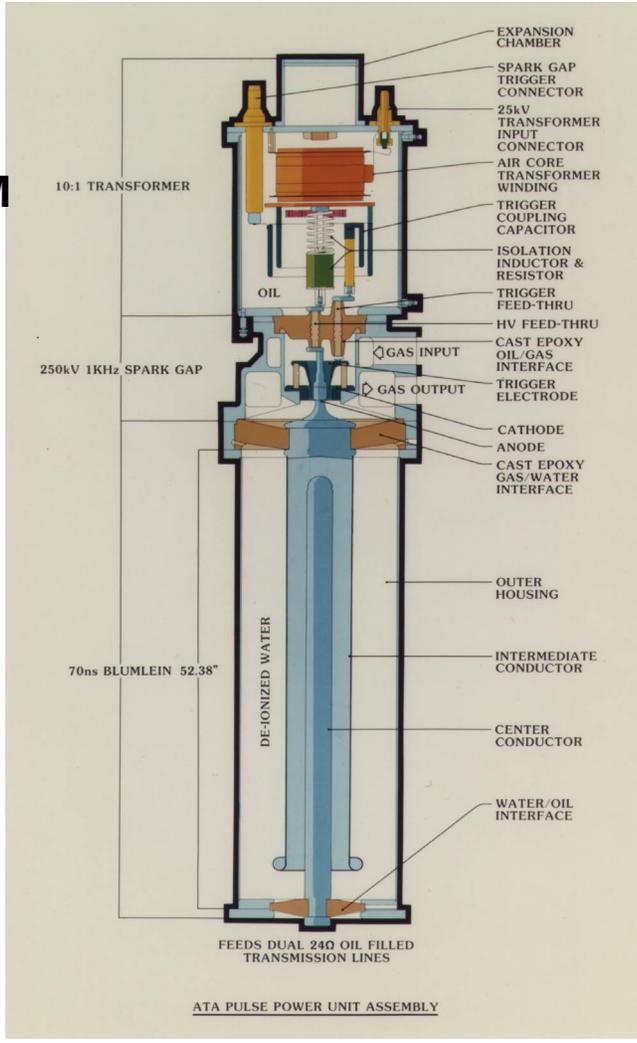


INDUCTION LINAC CURRENT PULSE POWER DRIVE



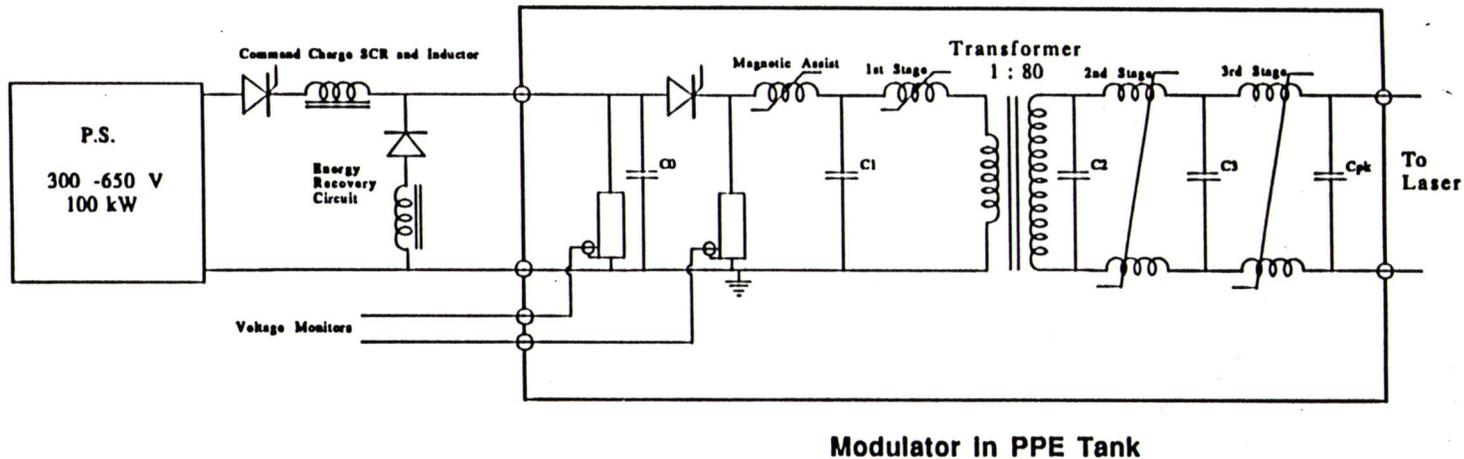
# Comparison of Sparkgap Triggered System and Multi-Stage Magnetic Compression System

Output:  
 250 kV  
 ~ 20kA  
 90 ns FWHM  
 $\tau_{\text{rise}} \sim 20 \text{ ns}$   
 1kHz burst  
 5 pulses



Output:  
 150 kV  
 ~ 75kA  
 75 ns FWHM  
 $\tau_{\text{rise}} \sim 20 \text{ ns}$   
 5kHz burst

# Schematic for 3 Stage -High Rep-Rate Modulator 1kV Input - 80kV Output

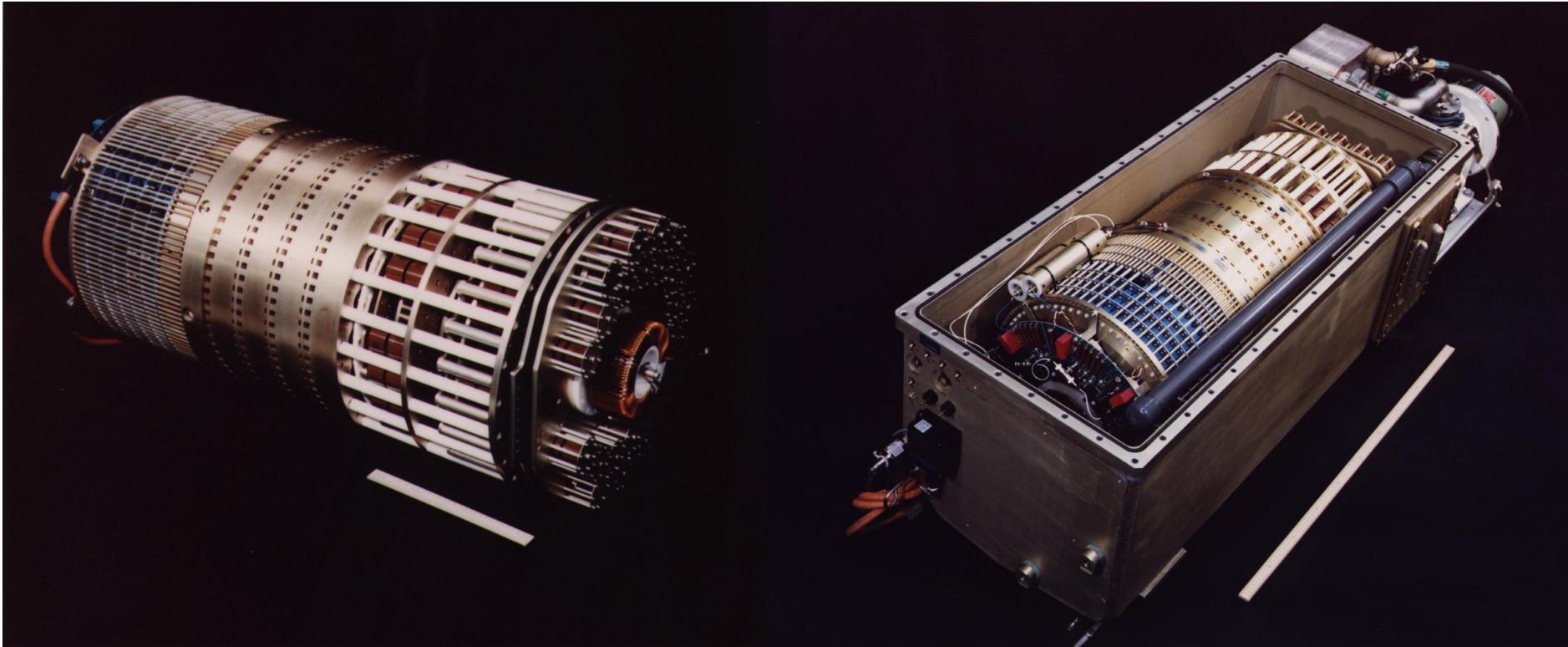


## ❖ Operating Parameters:

- 80 kV @  $\sim 4 \text{ kA}_{\text{peak}}$  (non-linear load)
- $\tau_{\text{rise}} \sim 30 \text{ ns}$
- $> 4 \text{ kHz}$  continuously
- liquid cooled
- MTBF  $> 5000$  hours

# 3 Stage -High Rep-Rate Modulator 1kV Input - 80kV Output

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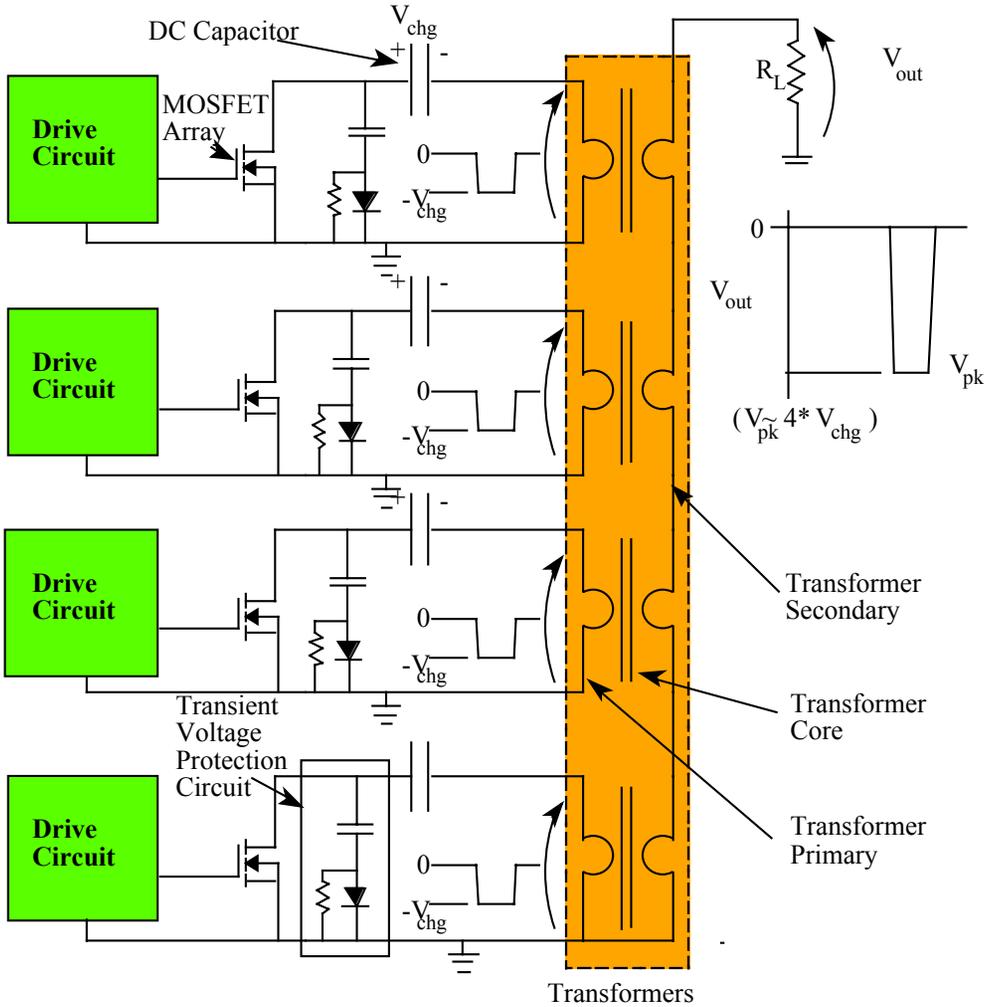


# References

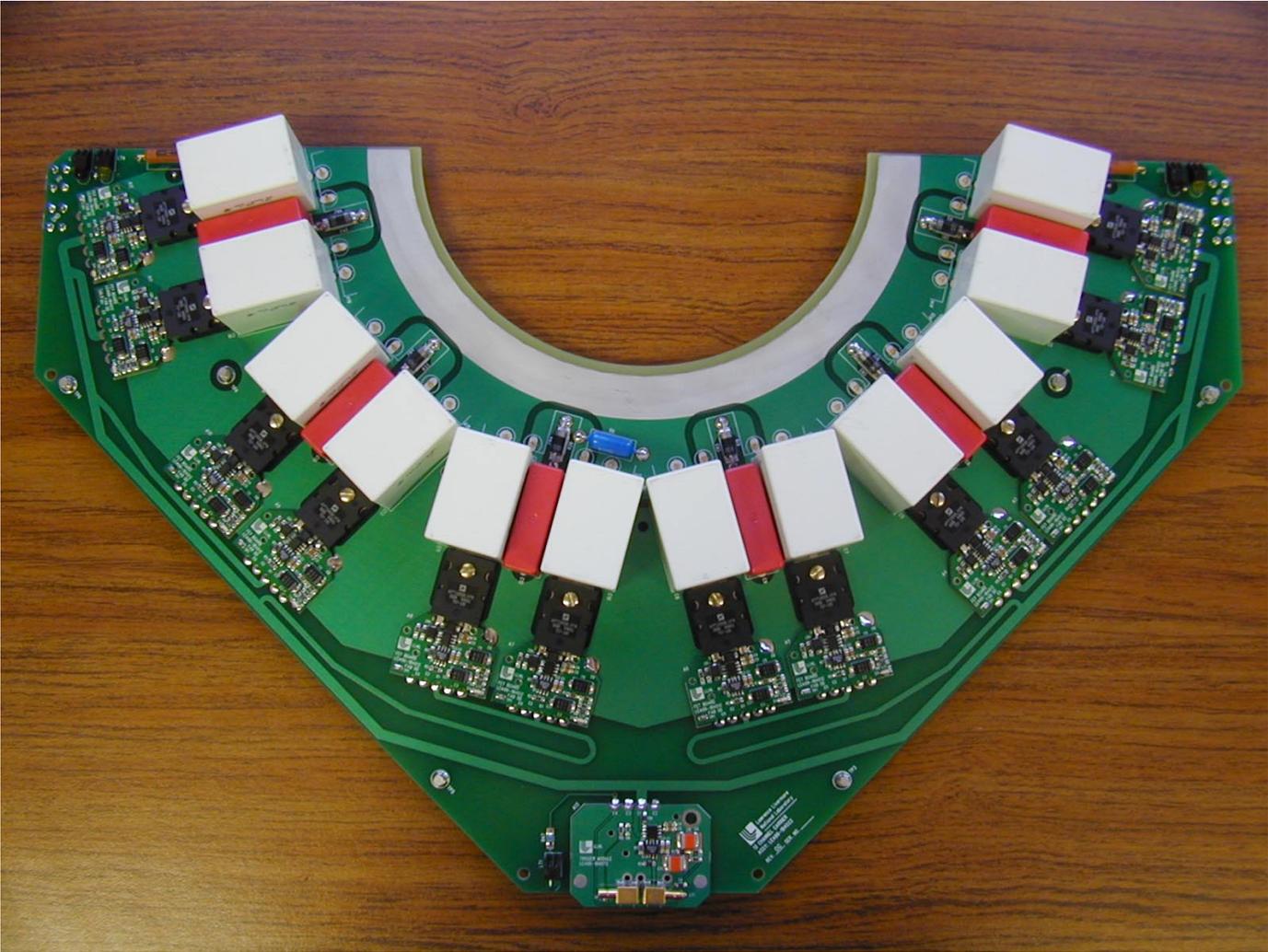
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- ❖ 1. W.S. Melville, “The Use of Saturable Reactors as Discharge Devices for Pulse Generators,” Proceedings Institute of Electrical Engineers, (London) Vol. 98, Part 3 (Radio and Communication), No. 53, 1951,p.185.
- ❖ 2. E.M. Lassiter, P.R. Johannessen, and R.H. Spencer, “High Power Pulse Generation Using Semiconductors and Magnetic Cores,” Proceedings Special Technical conference on Nonlinear Magnetics and Magnetic Amplifiers, September 1959, p.215.
- ❖ 3. D.L. Bix, “Basic Principles Governing the Design of Magnetic Switches,” UCID 18831, Nov. 18 1980.
- ❖ 4. D.L. Bix, L.L. Reginato, J.A. Schmidt, “An Investigation into the Repetition Rate Limitations of Magnetic Switches,” Fifteenth Power Modulator Symposium, Baltimore, MD, June 1982.
- ❖ 5. D.L. Bix, et al., “Magnetic Switching, Final Chapter Book I: The ATA Upgrade Prototype,” 1983 High-voltage Workshop, Harry Diamond Laboratories, Adelphi, MD, Oct 1983.
- ❖ 6. D.L. Bix,” Induction Linear Accelerators,” American Institute of Physics Conference Proceedings 249 - Volume Two The Physics of Particle Accelerators, 1992, pages 1553-1613.
  
- ❖ **General References:**
  - IEEE International Pulsed Power Conferences
  - IEEE Power Modulator Symposiums
  - IEEE International High Voltage Workshops

# Adder Concept - Simplified Schematic

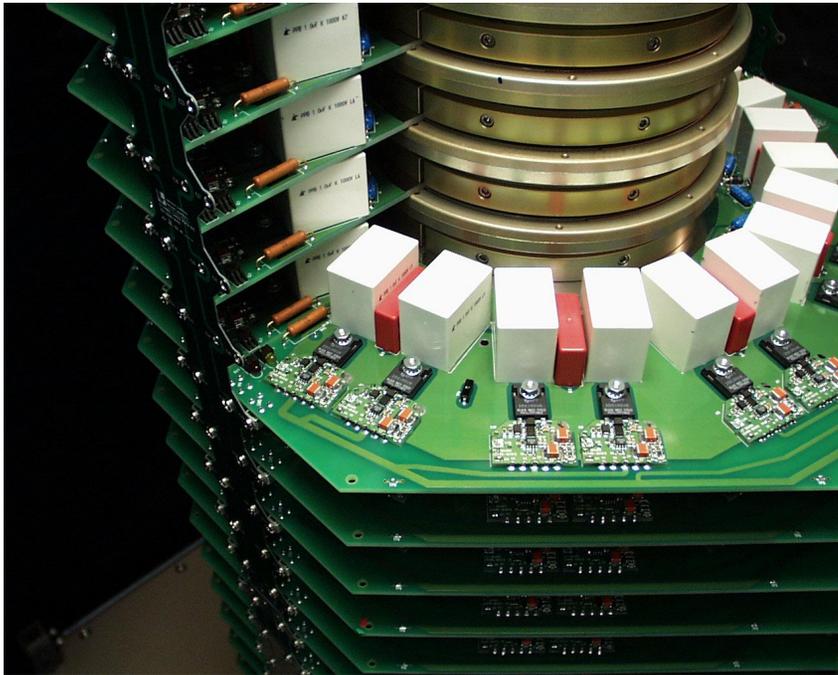


# Adder Drive Board



# Adder Assembly

Partial assembly as drive boards are being loaded



One assembled pulser stack

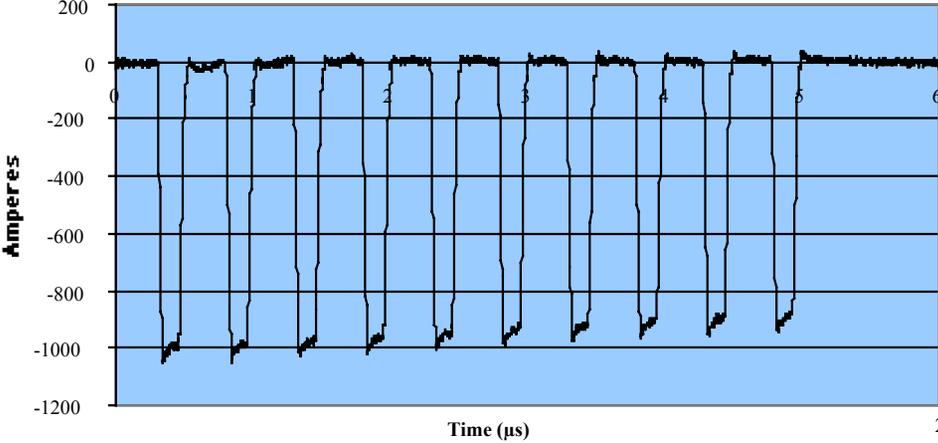


# Completed Prototype 50kV Adder Stack Assembly

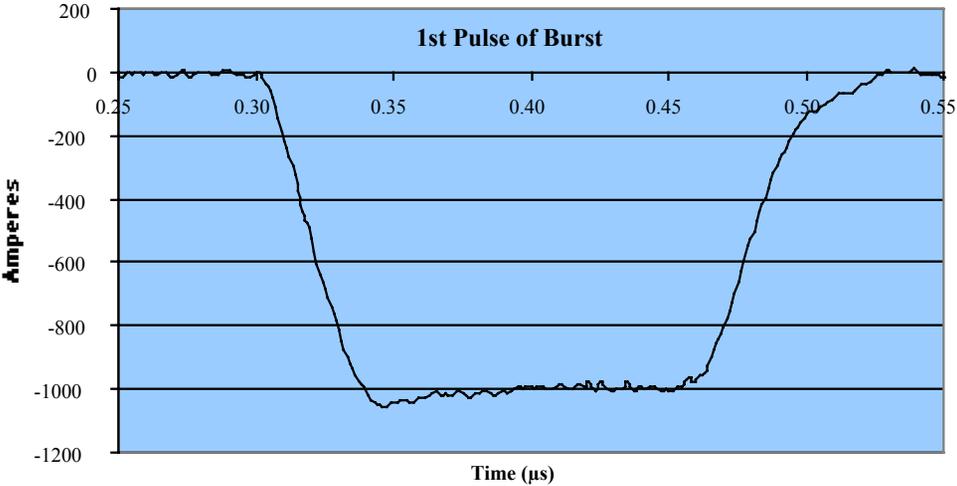


# 10 Pulse Burst @2MHz - 50kV Adder Circuit

Current @ 50Ω Load  
10P Burst @ 2MHz, 100ns PW, w/o reset

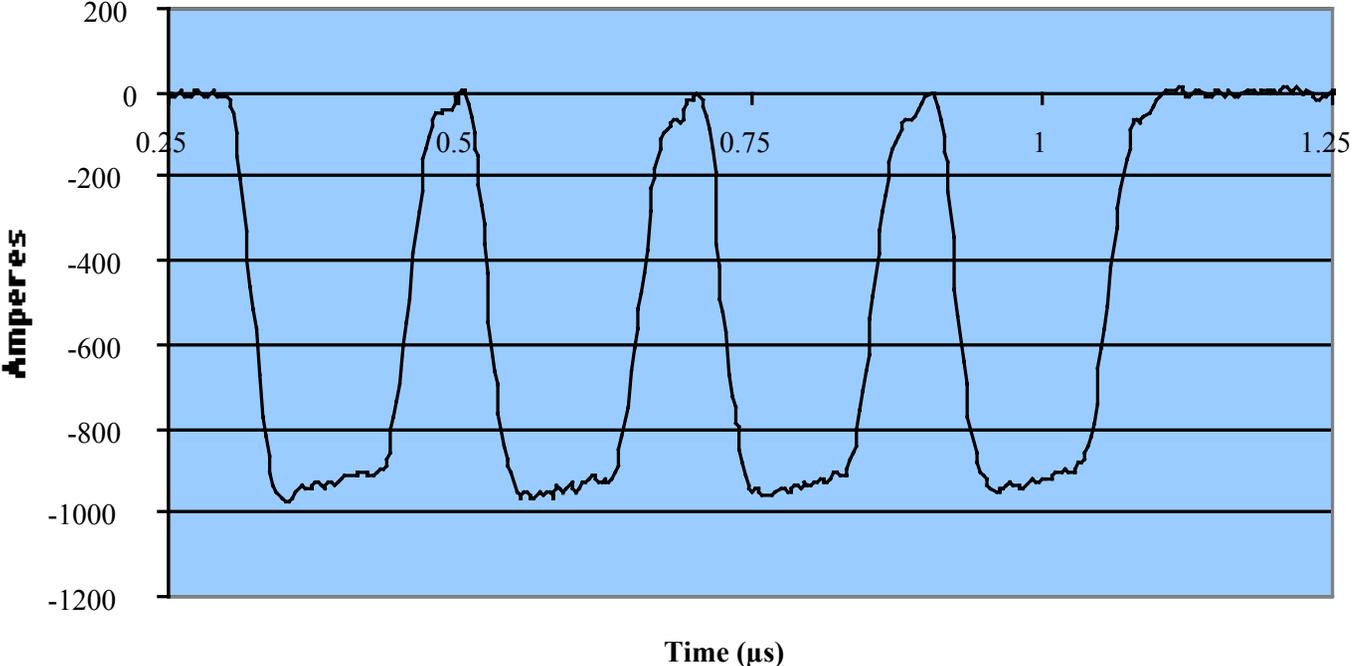


**Voltage sag is due to capacitor bank discharge during burst**



# 4 Pulse Burst @ 5MHz

Current @ 50 $\Omega$  Load  
4P Burst @ 5MHz, 70ns PW, w/o reset



# 20 kV Adder Stack Tests

## ❖ Burst Measurements - Variable Burst Frequency/Variable Pulse Width

