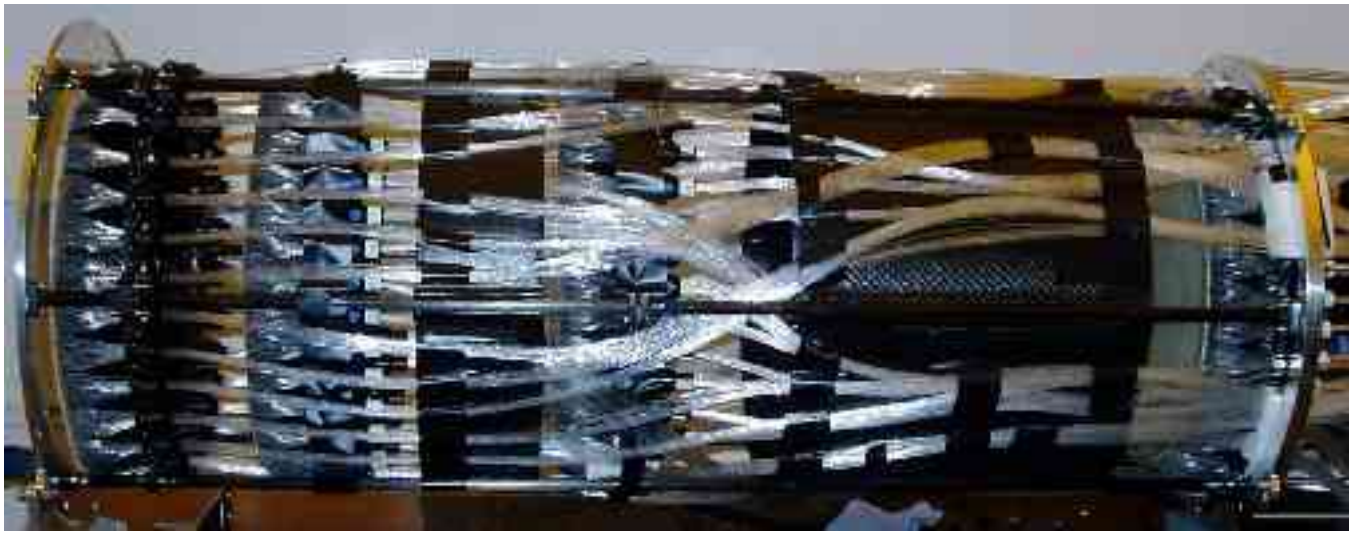
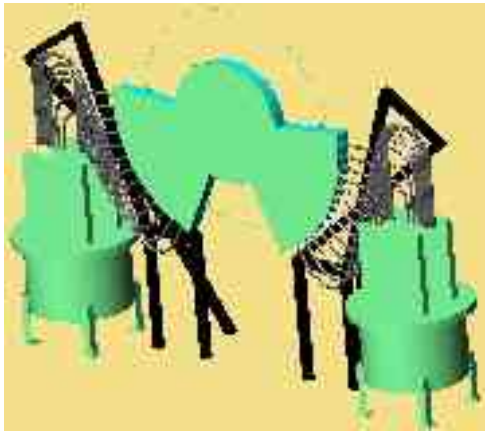
MICE Tracker Readout

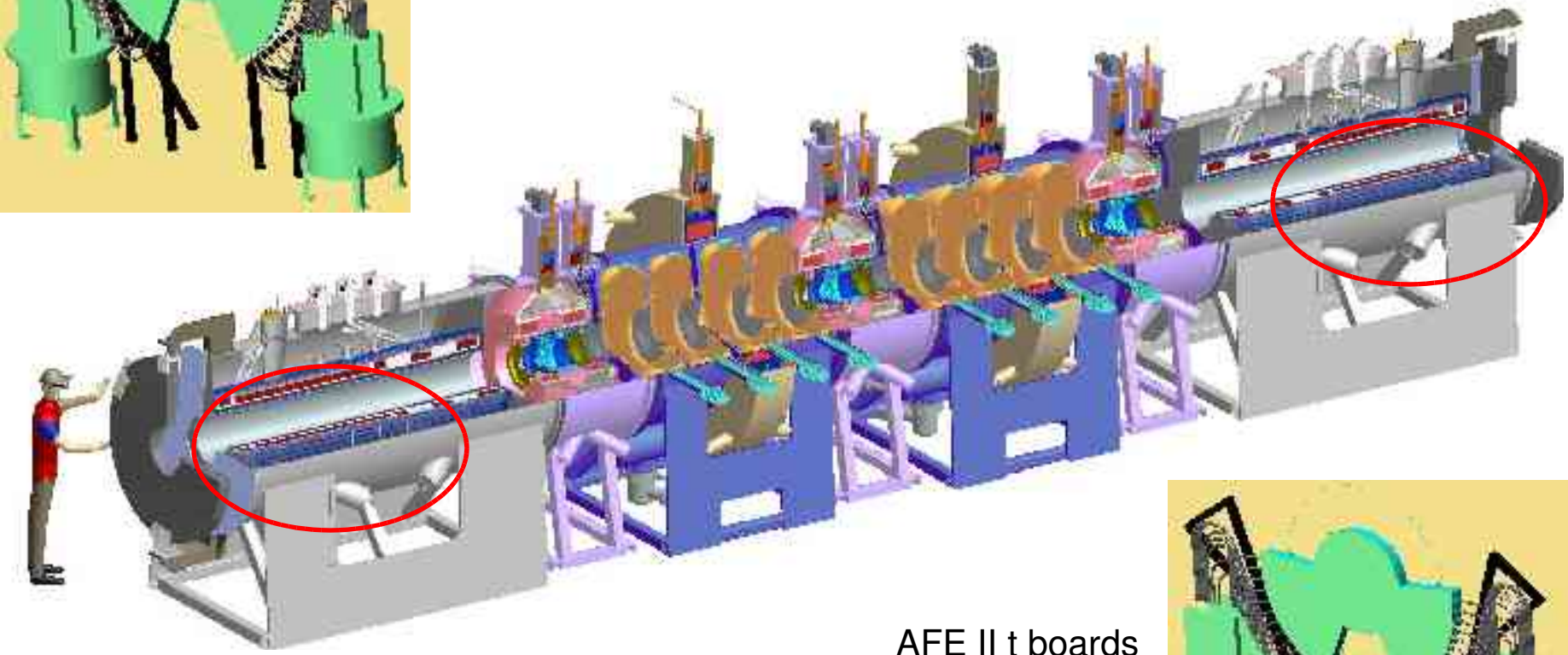


- AFE II t boards for D0 and MICE
- Revisions for MICE
- Current Status
- Plans and Schedule

Terry Hart,
NFMCC Meeting,
September 22, 2006

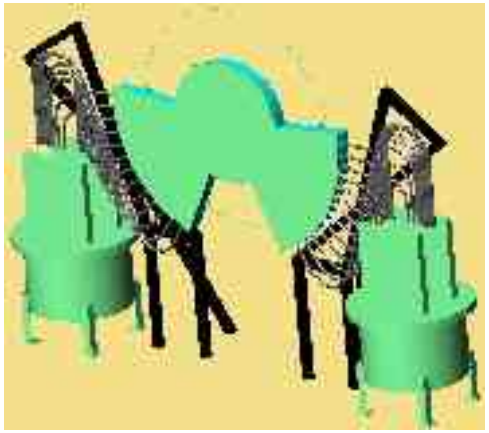
MICE Trackers





AFE II t boards
in cassettes

Cryostats



MICE IIT group is developing readout electronics for trackers.

MICE Tracker Readout Contributers

- IIT
  - Dan Kaplan, Adviser
  - Terry Hart and Bill Luebke, firmware developers and testing
  - Ben Freemire and Michael Wojcik, Electronics Board Testers
- Fermilab
  - Paul Rubinov, supervising board testing for D0 tracker upgrade
  - Tom Fitzpatrick and Kwame Bowie, assisting with development and electronics
  - Malcolm Ellis, assisting with MICE DAQ integration
- Rutherford Appleton Lab.
  - Senerath Galagedera and Craig MacWaters – assisting with firmware development and testing

MICE Tracker Readout with AFE II t boards

- Analog Front End II t (AFE II t) boards are developed for D0 tracker upgrade and used by MICE.
  - Inputs: Analog charge and time signals from 512 channels
  - Outputs: Digital hit pattern, charge amplitudes, time amplitudes

- MICE IIT group helped test AFE II t ~300 boards for D0 and will receive 25 (16 + spares).
  - Paul Rubinov supervised testing
  - IIT students Ben Freemire and Michael Wojcik carried out phases of tests.

MICE Requirements for Tracker Readout

- Data Rate: MICE has established goal of reading out 600 muons/ms.
  - D0 tracker readout optimized for TeVatron beam.
  - For MICE, current coding allows ~225 muons/ms.

- Data Readout: MICE tracker data will be read out to VLSB banks.
  - D0 data read out to digital boards and SVX sequencers.

MICE IIT group is modifying AFE II t firmware to realize these MICE requirements.

Data Rate

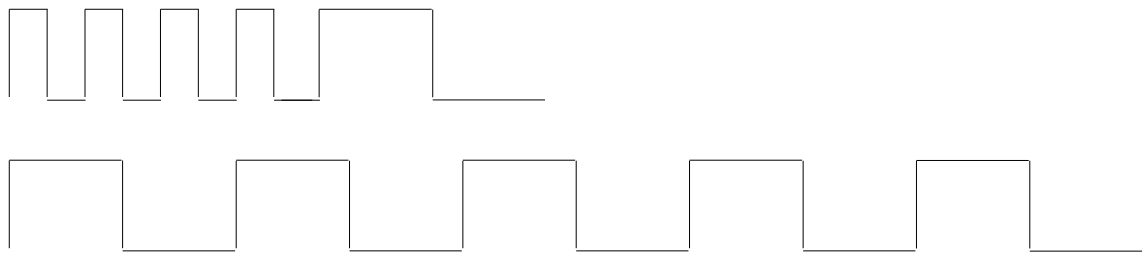
- D0 firmware uses 6 clock cycles for every AFE II t channel.

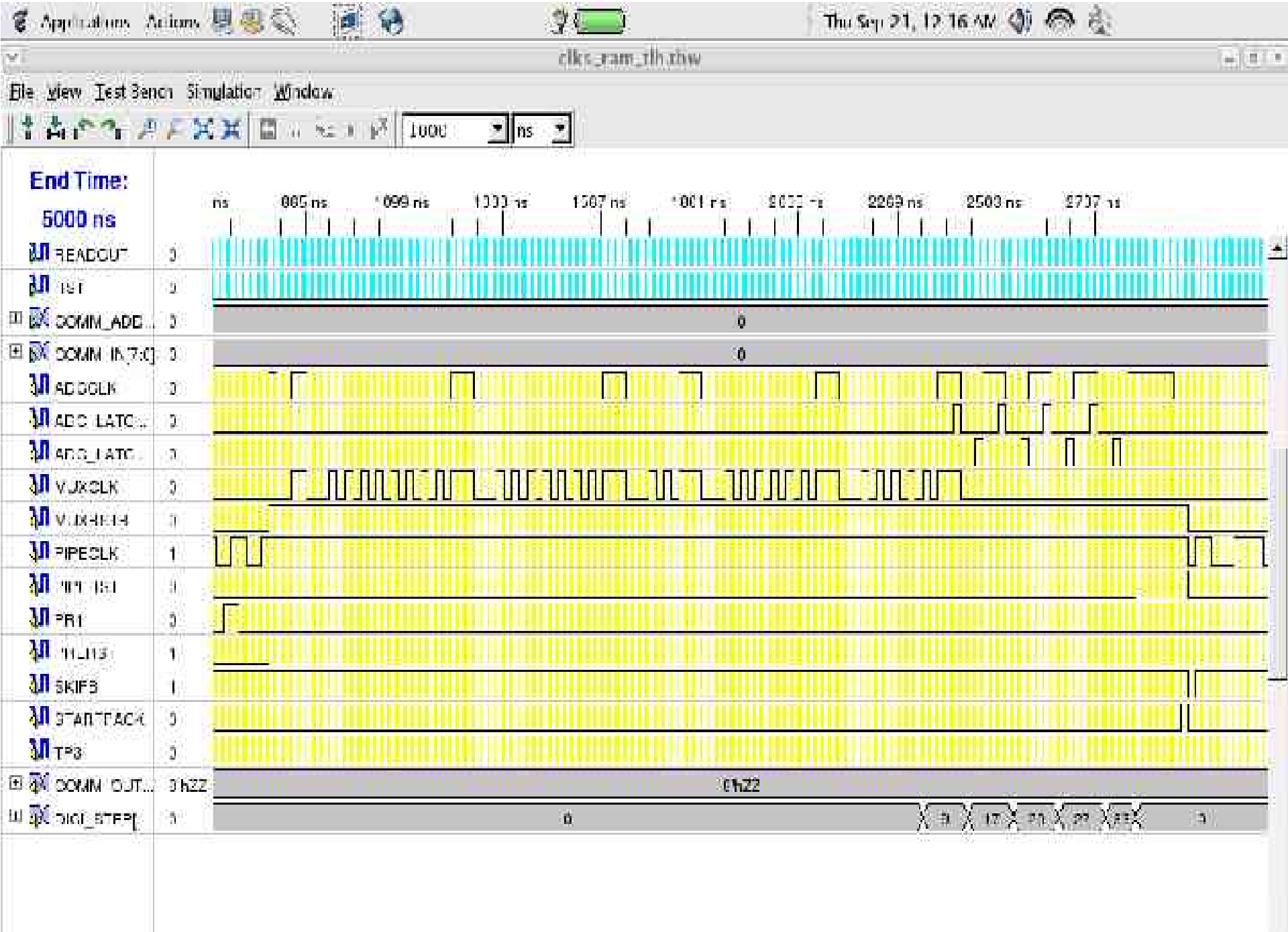
- For channels above threshold, ~100 ns or about 6 clock cycles is needed for digitization.

(1 clock cycle = 1/53.104 MHz = 18.831 ns)

Reduce digitization time by using only 2 clock cycles for channels below threshold.

Illustration of timing of 4 channels below threshold followed by 1 channel above threshold for compression scheme and nominal scheme.




Applications Actions
Thu Sep 21, 12:16 AM
clks_ram_tlh.tbw
File View Test Bench Simulation Window
1000
ns
End Time:
5000 ns
ns
885 ns
1099 ns
1587 ns
2269 ns
2503 ns
2737 ns
READOUT
COMM_ADD...
COMM_IN[7:0]
ADCCLK
PIPECLK
PR1
SKIPB
TP3
COMM_OUT...
0hZZ

Data Compression

- What's done:
  - Modified analog FPGA (AFPGA) firmware generating sequences of digitizer and raw data pipeline clock signals appropriate for data rate scheme. (Bill, Terry)
  - Signal simulations verifying that code logic is correct. (Bill, Terry)

- What needs to be done:
  - Firmware providing bitmap to the AFPGA to implement data rate scheme. (Senerath, Bill, Terry)
  - Verification of digitization with input signals. (Craig, Bill, Terry)

Data Readout

- What's done:
  - Firmware written which transfers data to VLSB banks in an added test mode. Signal simulations verify that the code logic is correct. (Bill, Terry)
  - Format for tracker readout suitable for MICE DAQ has been decided. (Malcolm, Bill, Terry)

- What needs to be done:
  - Transfer of test data to VLSB banks needs to be verified. (Bill, Terry)
  - Data transfer along LVDS links to VLSB banks needs to be made to work for D0 and MICE. (Craig, Bill, Terry)

Anticipated Schedule

- Early October: 25 AFE II t boards reserved for MICE
- Late October: Firmware development should be done or nearly done
  - Most progress on code for data rate increase
  - Data readout is well underway.
- Late November: Firmware testing
  - Data readout LVDS test mode written, but not yet tested.
  - Data rate scheme testing with input signals to board needs to start.