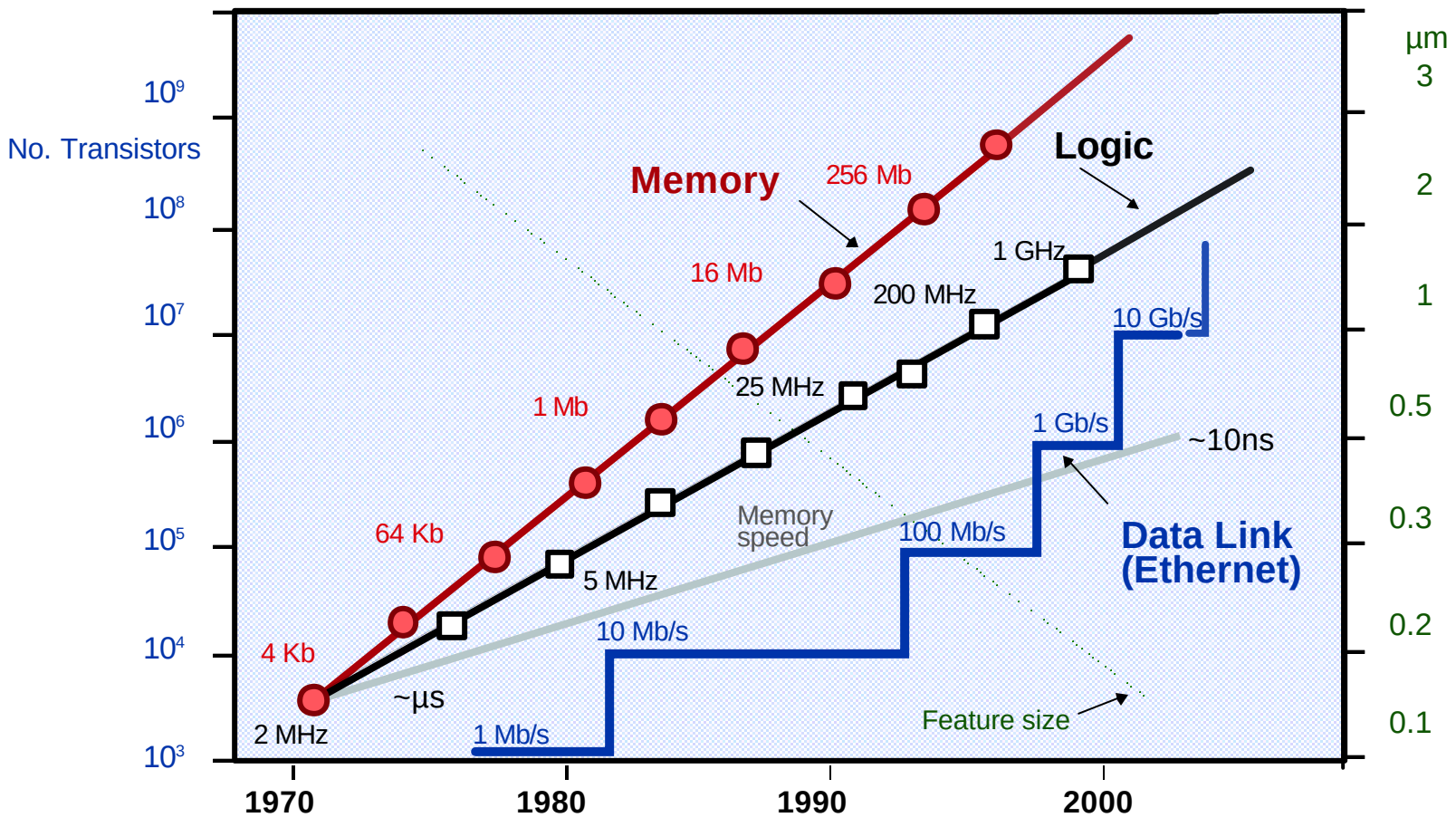
DAQ, etc.

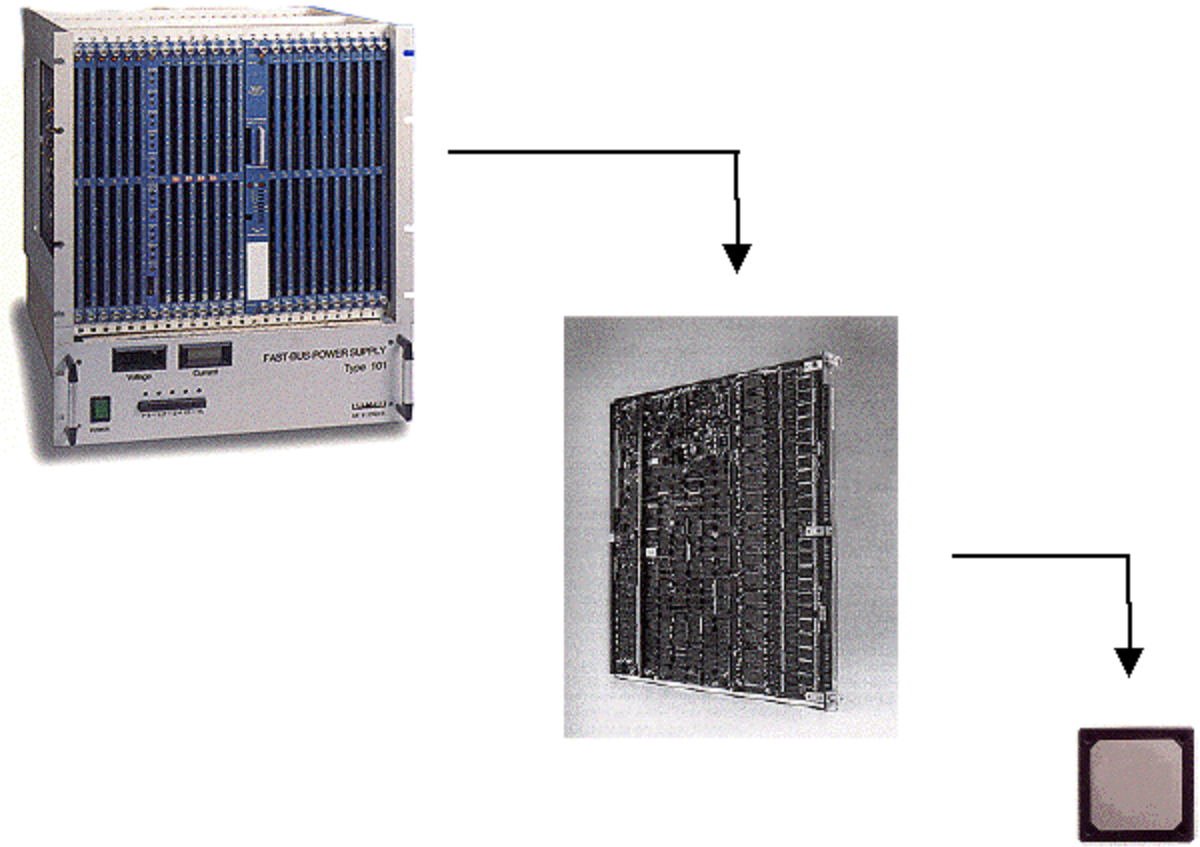
Guaranteed 99% content free

Technologies trends

(the obligatory Moore's law slide)

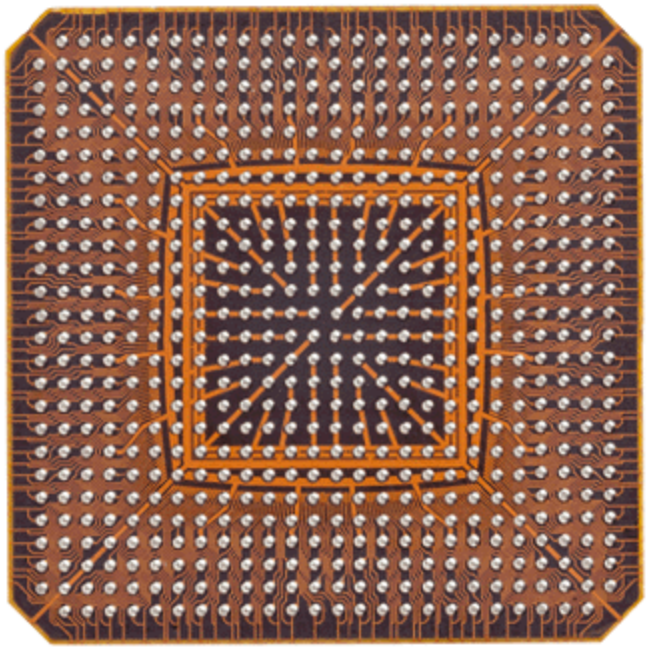


* slide borrowed from LHC



Integration

What once fit in a crate, now fits on a board…what once fit on a board now fits on a chip…most subsystems can be implemented on a single board with serial interconnects.

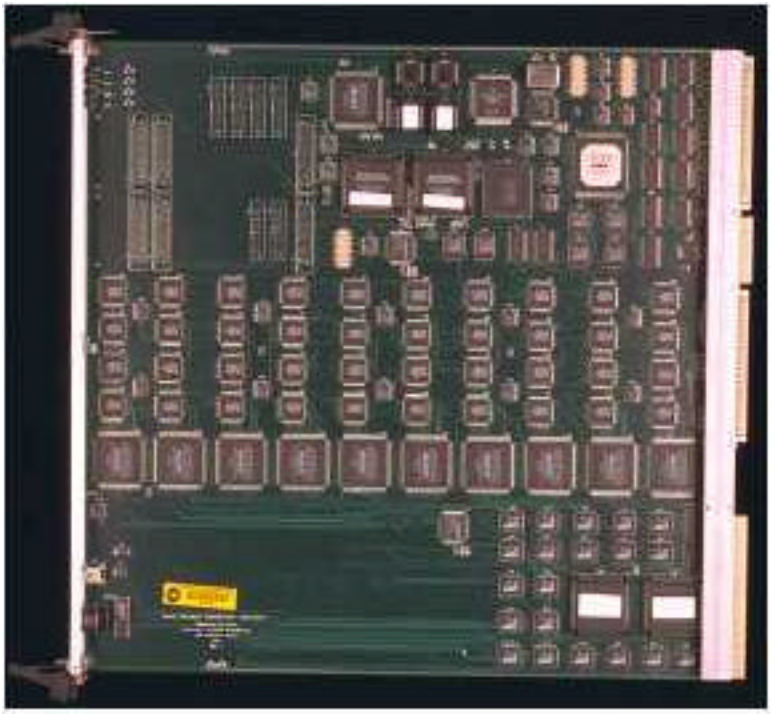


Big Chip Standard

Many new chips have high-speed serial interfaces, which can be used for both chip-to-chip and board-to-board interconnect.

Conversion to a parallel bus is inefficient and unnecessary.

Example

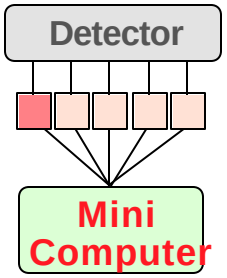


VRB (1995)

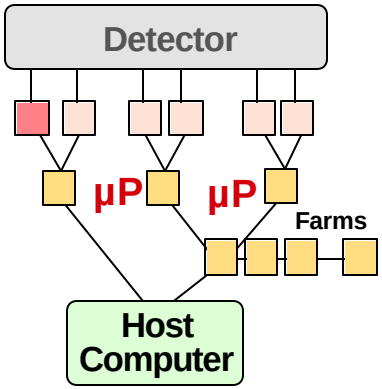
VRB (if done today)

Evolution of DAQ technologies and architectures

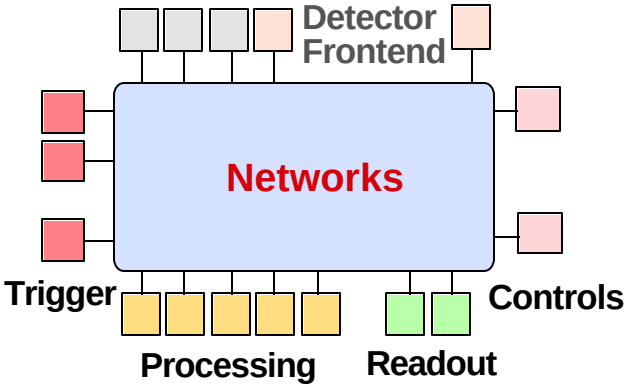
1970-80
MiniComputers
First standard CAMAC
Custom design
- **kByte/s**



1980-90
Microprocessors
Industry standards
Distributed systems
- **MByte/s**

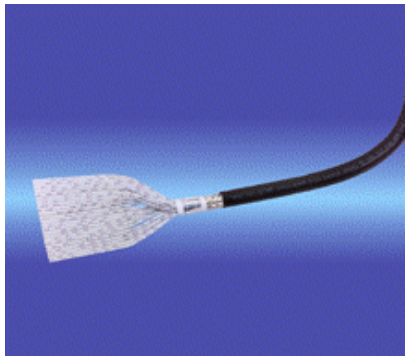


2000
Networks
Commodities
Data and control networks
- **GByte/s**



* slide borrowed from LHC

Data Links



Optical link (> 30 meters)

12 channels at 2 Gbps each

~ $200/channel

Copper link (< 30 meters)

12 channels at 2 Gbps each

~ $100/channel

Copper is still improving.

> 100 ft on cheap coax at

3 Gbps with equalization.

4 Results

Table 1 shows a summary of bit rates, lengths, and deterministic jitter for the different media samples. Figure 2 shows that the MAX3800 can restore high-frequency information that is 30dB down. The upper trace is the output of the cable that is applied to the input of the MAX3800. The lower trace of Figure 2 is the fully restored signal at the output of the MAX3800. Figures 3 through 6 are eye diagrams for the different cables operating at 2.5Gb/s. Figures 7 and 8 are eye diagrams for the FR4 sample operating at 2.5Gb/s.

5 Conclusion

Equalizing gigabit signals with the MAX3800 offers new distribution and interconnection possibilities to a world starving for more bandwidth.

Table 1. Equalized Media Performance (PRBS-7)

Medium	Length (ft)	Bit Rate (b/s)	Deterministic Jitter (UI)
W.L. Gore–type 89 matched 50Ω coax pair	115	3.2G	0.04
		2.5G	0.03
		622M	0.01
RG179B coax single-ended 75Ω	100	3.2G	0.16
		2.5G	0.09
		622M	0.04
Belden 9207 twin-axial 100Ω	100	3.2G	>0.67
		2.5G	0.20
		622M	0.04
Madison #14887 shielded twisted-pair 100Ω	50	3.2G	0.16
		2.5G	0.12
		622M	0.02
Stripline, FR4 6mil wide, 50Ω	4.2 (50in)	3.2G	0.09
		2.5G	0.06
		622M	0.03

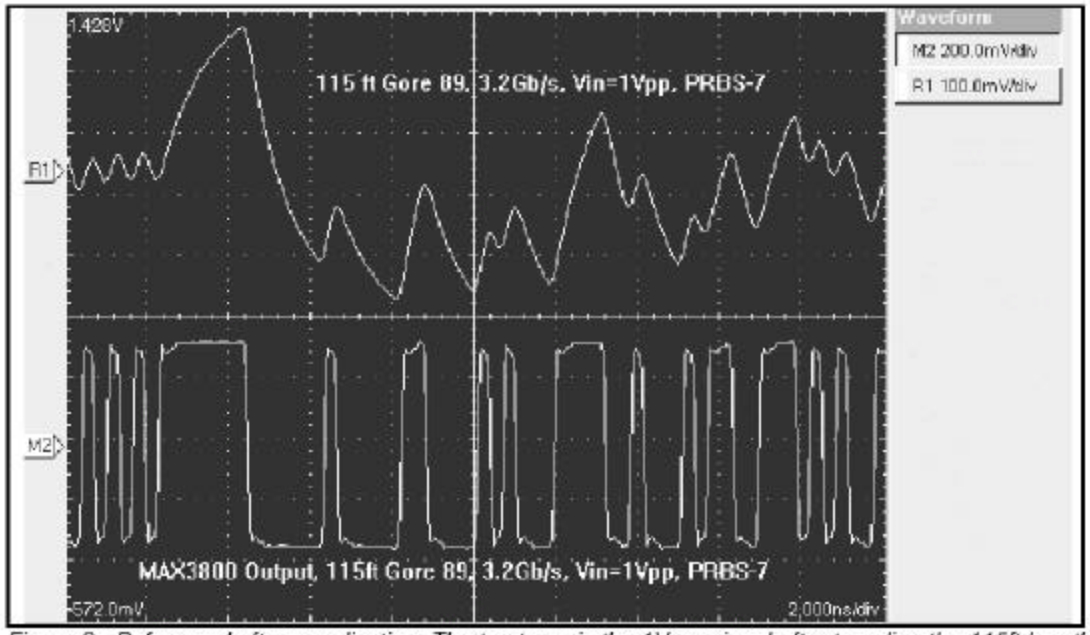


Figure 2. Before and after equalization. The top trace is the 1Vp-p signal after traveling the 115ft length of the Gore-type 89 cable. Note the small ripples and bumps. These are single bits that have encountered 30dB of loss. The lower trace is after the upper trace was equalized by the MAX3800. All of the bits are fully restored.

MINDSPEED
A CONEXANT BUSINESS

1–3.4 Gbps SerDes Transceiver with Amplif–Eye2™

M27211 Octal SkyRail™

Low-power (1.6 W) octal 1-3.4 Gbps CMOS SerDes transceiver for high-speed backplane applications

The M27211 Octal SkyRail from Mindspeed Technologies™ is a flexible 1-3.4 Gbps eight-channel serializer/deserializer (SerDes) transceiver chip ideal for backplane applications addressing today's wide range of data rate standards (1 Gigabit Ethernet and 10 Gigabit Ethernet, Fibre Channel, InfiniBand, SONET/SDH). The chip can operate at bit rates as low as 1 Gbps per channel and provide up to 27.2 Gbps of duplex raw data bandwidth. It is the first octal SerDes transceiver to operate at 3.4 Gbps. The device integrates eight transmitters and receivers, a SerDes function, clock and data recovery and synthesis circuits, clock forwarding capability, 8B/10B encoders and decoders, termination resistors, channel-to-channel synchronization circuitry, and is capable of detecting a variety of special characters and COMMA for byte alignment. It requires no external components for operation.

The M27211 Octal SkyRail high-speed serial outputs are equipped with Amplif-Eye2™ second generation signal-conditioning circuitry and 7-level pre-emphasis settings to optimize and maximize the device's reach over very long traces and standard connectors.

The M27211's 8B/10B encoding/decoding logic can be bypassed to enable SONET/SDH scrambling or a customer's proprietary encoding algorithm. The M27211 can tolerate more than 90 consecutive identical digits to support these alternate encoding schemes. The M27211 can also operate in a clock-forwarding mode with no encoding required and is the first device to support the DIF Gel-5 interface capability for DC-768 applications. When operating in a clock-forwarding mode, the M27211 delivers an effective baud rate of 27.2 Gbps or 34 Gbps of 8B/10B equivalent data.

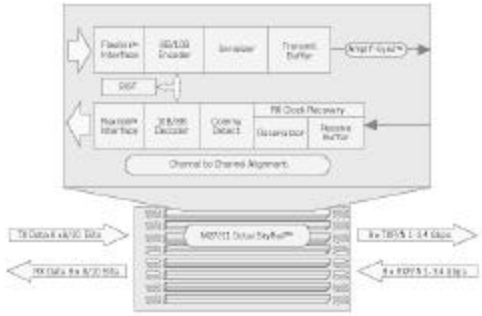
The M27211 Flexlink™ parallel interface is SSTL-2 tolerant and can be configured as 1.5 V or 1.8 V HSTL, TBI (Ten Bit Interface) or XGMII for 1-Gb or 10-Gb Ethernet. It can also be configured as 32 or 40 bits wide, depending on whether the encoding and decoding functions are performed within the M27211 or off-chip, or if clock forwarding is employed. The Flexlink interface can accommodate source-synchronous and source-centered data, simplifying board and ASIC design.

KEY FEATURES

- Ultra low power consumption of 1.6 Watts-first SerDes transceiver to consume 200mW per channel
- Wide range, low-jitter PLL enables scalability and backward compatibility with legacy systems
- Amplif-Eye2 signal conditioning circuitry with 7-level settings and less than 60 mV receiver input sensitivity provides signal integrity over one meter of FR-4 with four connectors
- Flexlink™ parallel interface simplifies system design, provides low power 1.5–1.8 V HSTL and SSTL-2 interface options
- De-skewing circuitry for channel-to-channel alignment simplifies system design
- Supports 802.3ae 10 Gigabit Ethernet, 10 Gigabit Fibre Channel, InfiniBand, ANSI X3T11 Fibre Channel and 802.3z Gigabit Ethernet data rate standards
- All controls available through external pins, simplifying design and debug and eliminating the need for an external CPU

The interface can operate at single data rate in half-speed mode or double data rate in full-speed mode. The incoming clock samples the data on both the rising and falling edges when running in full-speed mode.

The M27211 Octal SkyRail can operate as eight independent serial links, each with an eight- or 10-bit HSTL or SSTL2 parallel interface and up to 3.4 Gbps of serial data transfer. The Octal SkyRail can also be configured as a single bundled link providing up to 27.2 Gbps of synchronous data bandwidth.



M27211 functional block diagram

Product Features

Features

- Eight full-duplex serial transceivers capable of bit rates from 1 Gbps to 3.4 Gbps each
- Low-power CMOS technology (typically 1.6 W @ 3.125 Gbps)
- Built-in 8B/10B encoder and decoder and special character detection with bypass option
- Supports ANSI X3T11 Fibre Channel, 802.3z Gigabit Ethernet, 802.3ae 10 Gigabit Ethernet and InfiniBand data rate standards
- COMMA detection for byte alignment
- Internal 50 Ohm serial termination
- Monolithic clock synthesis and clock recovery with automatic lock-to-reference function — no external components required
- Data can be clocked with the local reference clock, with each channel's recovered clock or with a single master channel's recovered clock when all eight channels are aligned
- Programmable transmit pre-emphasis for optimum performance over long cables and 40" PCB trace lengths
- Current mode logic (CML) high-speed differential signaling
- Supports both AC and DC coupling
- High-speed and low-speed loopback modes and built-in self test (BIST) with PRBS random number generation for at-speed internal and external self-testing and diagnostics
- Suitable for printed circuit boards, coaxial cables and as an interface to optical modules
- 324-ball HSFBGA (23×23 mm^2) package
- 1.8 V core supply with 1.5 V–1.8 V HSTL interface, 2.5V SSTL2 tolerant

Benefits

- High level of integration reduces system cost and board space
- Wide range of operation allows forward and backward compatibility
- Ultra low power consumption enables higher part densities with no increase in overall system power
- Fully integrated design with no external components for design simplicity and optimal board layout
- Amplif-Eye2 signal conditioning circuitry enables high-speed operation with existing backplanes and connectors and good signal integrity over 40" of FR-4 material

Applications

- High-speed serial backplane interconnects
- Chassis-to-chassis serial connections

Ideal For

- High-end and midrange routers
- Enterprise and carrier-class switches
- Storage Area Network (SAN) equipment
- Add/drop multiplexers
- Optical crossconnects
- Network aggregators
- WAN access concentrators
- Server clusters
- High-speed automatic test equipment and high-bandwidth testers

Ordering Information

Evaluation boards are available and the M27211 device can be ordered in four data rates:

1–1.25 Gbps

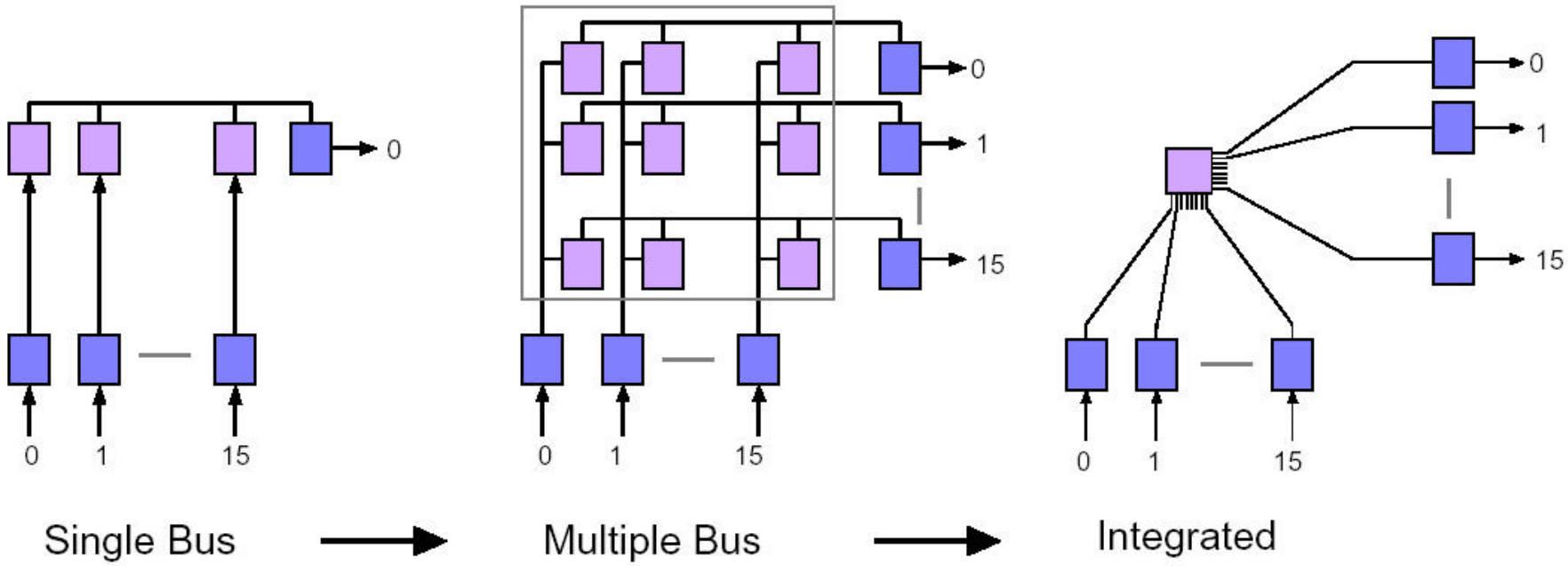
1–2.5 Gbps

1–3.125 Gbps

1–3.4 Gbps

Please contact your local sales representative for details or visit us at www.mindspeed.com

Octal serializer/deserializer… 8 X 3 Gbps…~$130



Event Building

CDF Event Builder

Fore (Marconi) ASX-1000 ATM Switch

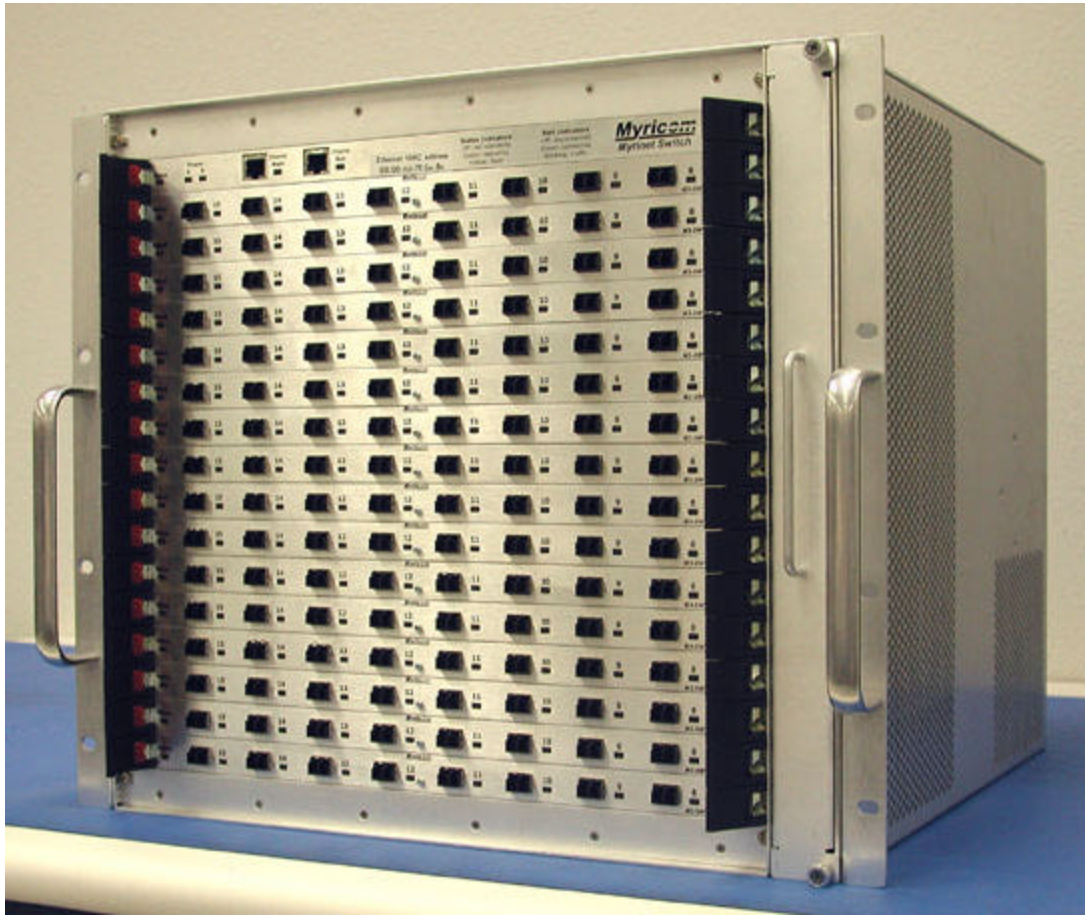
64 ports at 155 Mbps or 16 ports at 622 Mbps (~1 GByte/sec total bandwidth)

Foundry Networks Bigiron Ethernet Switch.

130 ports at 1 Gbps (~13 GBytes/sec total bandwidth)

Brocade Fibre Channel Switch.

128 ports at 1 Gbps (~13 GBytes/sec total bandwidth)

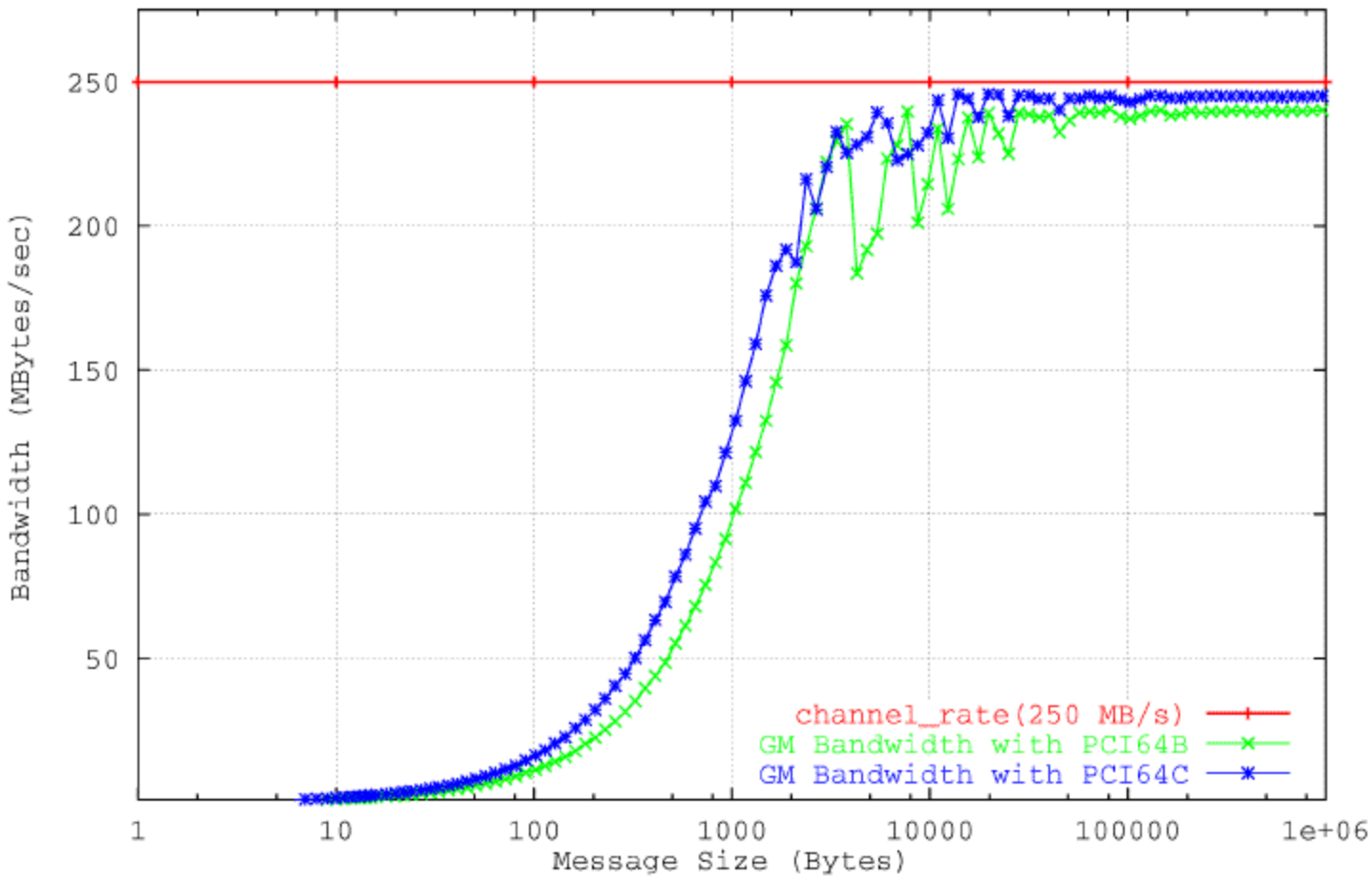


Myrinet Switch.

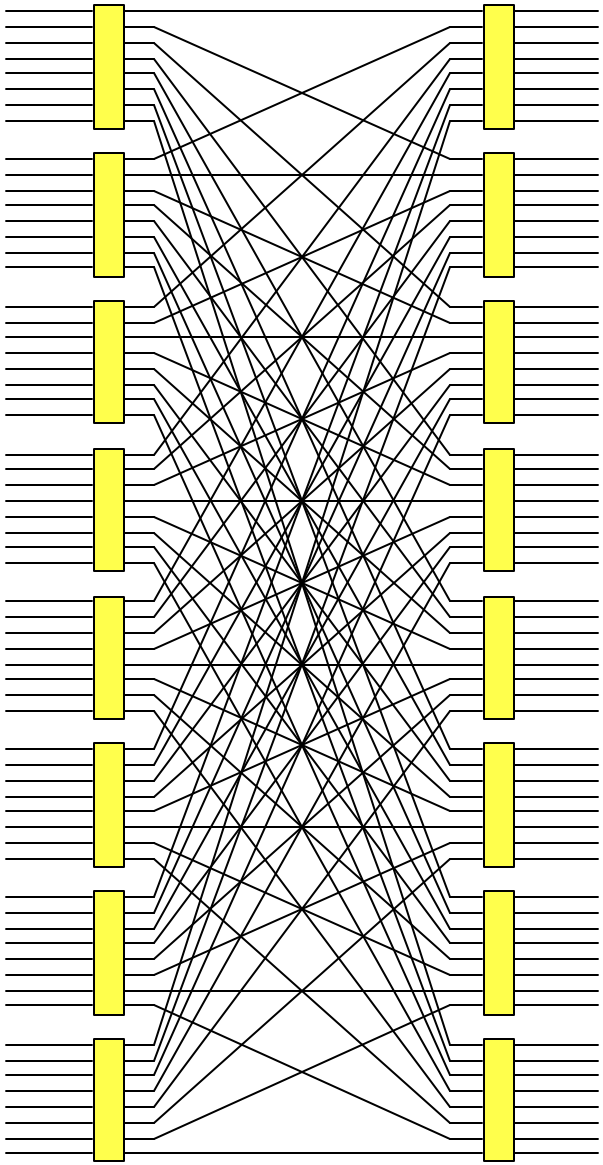
128 ports at 2 Gbps (~ 25 GBytes/sec total bandwidth)

Qlogic Infiniband Switch.

15 ports at 2 Gbps (~ 3 GBytes/sec total bandwidth)



Packet size is the most important factor.



Switch Expansion

A simple two stage interconnect is sufficient for event building.

Clos network not required.

MINDSPEED
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144x144 3.2 Gbps Crosspoint Switch with Integrated CDR and Programmable Input Equalization

M21155

Most integrated, highest performance crosspoint switch reduces system cost and complexity

Built on two generations of industry-leading crosspoint switches and CDRs, the M21155, designed for today's demanding telecom an datacom applications, is a low-power CMOS, high-speed 144x144 crosspoint switch with integrated CDRs, input equalization and built-in system test features.

To simplify board design and increase system reliability, each input has a high-jitter tolerant, low-jitter generation CDR with internal loop filter. All CDRs use a common, single frequency reference clock (19.44 MHz) for internal calibration and acquisition. Each CDR operates independently at any data rate from 1.0 to 1.6 Gbps, or 2.0 to 3.2 Gbps. As a result, the device supports any combination of OC-48, OC-48 FEC, Fibre Channel (1x, 2x, 10x), InfiniBand, Gigabit Ethernet, 10 Gbps Ethernet traffic or other types of traffic.

To achieve the best possible signal, each CDR is preceded by a programmable input equalizer (IE), which removes ISI jitter, usually caused by PCB skin effect losses. The IE circuit opens the input data eye in applications where long PCB traces and cables are used. As a result, the device exceeds the SONET requirements with jitter tolerance of 0.65UI, and jitter generation of less than 1.5mUI (rms) or 8mUI (pp).

The device consumes as low as 18W of power (typical), with all channels and CDRs operational. In addition, the

KEY FEATURES

- Integrated per-channel multi-rate CDRs, with bit rates of 1.0-3.2 Gbps
- Programmable input equalizer to remove deterministic jitter (ISI), caused by board traces and cables
- Performance far exceeding the SONET requirements with 0.65UI jitter tolerance and 1.5mUI (rms) jitter generation
- Supports SONET, DWDM, GbE, 10 GbE, Fibre Channel (1x, 2x, 10x) and InfiniBand applications
- Low power consumption of 18W, nearly 60% power savings compared to an equivalent circuit with external CDRs
- PowerScaler for further power reduction based on system needs
- Built-in system test features such as Jitter Meter and PRBS Tx/Rx

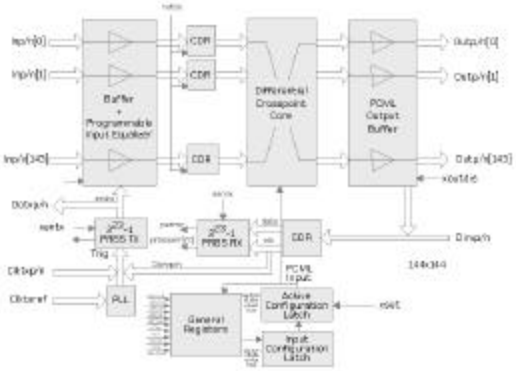
PowerScaler features offer dynamically scalable switch settings to further reduce power consumption. Each CDR can be independently bypassed and turned off if not in use. In addition, unused portions of the core can be automatically (Smart Power) or manually turned off, without affecting the operation of the remaining channels.

Built-in system test features simplify design, verification and production testing of the system. These features include a third generation PRBS transmitter/receiver, and Jitter Meter. The switch includes a pair of on-board 2^{31}-1 pseudo-random bit sequence transmitters (PRBS Tx) and receivers (PRBS Rx). In addition, the Jitter Meter feature allows the host controller to measure jitter of an incoming signal.

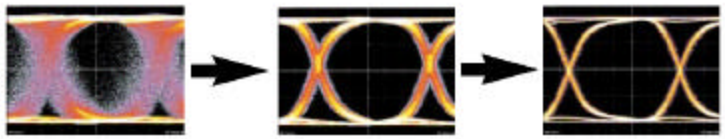
Three-stage switch fabrics with up to 1036x1036 ports, carrying up to 33 Terabits per second of traffic, can be designed using this non-blocking switch, with multi-cast and broadcast abilities. All inputs and outputs are differential PCML (positive current mode logic) with supply voltages ranging from 1.2V to 2.5V. The output levels are programmable at 500mV, 900mV, and 1200mV.

The M21155 is available in a 1156-terminal, 35mm, CBGA (Ceramic ball Grid Array) package, operating at temperatures from 0°C to 85°C.

Also, for applications that do not require an integrated CDR, the M21150 144x144 Crosspoint Switch with Input Equalization can be used.



M2115 functional block diagram



Signal with ISI and Random Jitter (Eye Closed) | Input Equalizer Removes ISI Jitter | CDR Removes ISI and Random Jitter

Product Highlights

Applications

- Large N x N cascaded switch fabrics, up to 33 Terabits/second
- DWDM Switches
- Fiber-optic Telecom Systems (OC-48/OC-48 FEC)
- Telecom and Datacom Switches
- Packet Switching
- Storage Area Network (SAN) Switches (Fibre Channel, 2x Fibre Channel, 10x Fibre Channel)
- 10 GbE parallel and GbE networks
- High-speed Automated Test Equipment

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MINDSPEED
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Next Generation Switch

Event builder on a chip…144 ports at 3 Gbps (~ 40 GBytes/sec total bandwidth)

Product Summary

3.2 Gbps Cross Point Switches with Integrated Clock and Data Recovery

0.95 - 3.2 Gbps 140x140 Lane (VC3003) and 72x72 Lane (VC3002) Repeating (Eye Opening) Multi-Rate Cross Point Switches with Clock, Data Recovery at Each Serial Input, Output, and Pre-Emphasis at Each Serial Output for Best of Breed Signal Integrity in Optical and Electrical Links

GENERAL DESCRIPTION

VC3003 and VC3002 are flexible data rate, repeating (eye opening), cross point switches capable of continuous serial data rates from 0.95 to 3.2 Gbps. Each serial input goes through a clock, data (CDR) recovery unit, thus eliminating the need for external CDR devices at the inputs. This conserves board space and reduces power consumption. The incoming serial data lines are switched toward their programmed output. At the serial outputs, care is taken that the output jitter is very low. In addition, pre-emphasis is applied to the outputs to remove the deterministic jitter introduced by the interconnect. These features eliminate the need for discrete CDR devices at the outputs. VC3003 and VC3002 utilize Velio's high-speed Gigacores (SERializer and DESerializer cores) for their serial I/O circuitry. The user-selectable features of each GigaCore address Inter-Symbol Interference (ISI) and help ensure signal integrity at multi-gigabit speeds. The integrated Gigacores enable these devices to link across electrical backplanes directly and make optical links work better as well. VC3003 and VC3002 may be used as multi-lane CDR devices for large port count optical applications.

VC3003 & VC3002 Features and Benefits

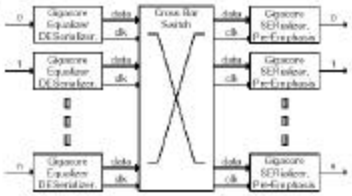
FEATURES	BENEFITS
140 x 140 switching matrix with 2 Configuration Tables	Enables 8K x 8K 3-stage Clos architecture
DESerializer at Serial Inputs with Clock and Data Recovery	Removes the need for external CDR devices at inputs
SERializer at Outputs with Programmable Amplitudes	Provides for low output jitter with all 140 lanes transmitting data
Programmable Pre-Emphasis at the Serial Outputs	Removes the need for external CDR devices at outputs
Host Bus Interface or MDIO / MDC Interface	Two ways to access internal register sets of multiple devices
3 Reference Clocks and 5 Multiplier Values	A maximum of 15 different Multi-Rate connections

APPLICATIONS

- Building Block for Multi-Stage, Clos Networked, Large Optical Routers
- CDR farm for large port count Optical Transceivers
- Support for Tiled Cross Connect Switch Architectures
- Patch Panel for Mesh Based Switching Routers
- Repeater for Optical Transponders
- Repeater for Very Short Reach Optics
- Repeater for Back Planes

PHYSICAL SPECIFICATIONS

- 1296 Pin Flip-Chip BGA (36 x 36 Array at 1 mm Pitch)
- Low Power (17W at 2.5Gbps with Ability to Turn Unused Lanes Off)
- 1.8V (Serial I/O) and 2.5V (Control I/O) Power Supplies
- JTAG with Ability to Test Each Serial I/O Pin for Connectivity
- Integrates 140 SER and DES Block Pairs for Each Serial I/O



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May 22, 2001
REVISION 1.2

EFFECT OF CLOCK AND DATA RECOVERY ON DETERMINISTIC AND RANDOM JITTER

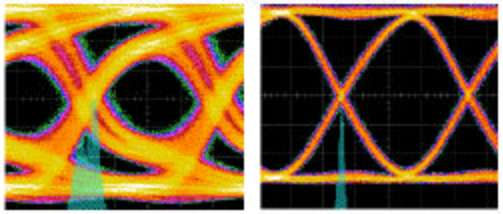

Figure 1: The eye diagram on the left shows the electrical output from an optical receiver at 2.5Gbps. The histogram contains deterministic and random jitter. The eye diagram on the right shows the output jitter from VC3003. The histogram shows that deterministic jitter has been removed and random jitter is narrowed. VC3003 output jitter is less than 0.20UI at 3.125 Gbps with all 140 lanes transmitting data. Similar reductions in deterministic and random jitter are observed with signals that cover long backplane traces and connectors.

EFFECT OF LOW OUTPUT JITTER AND PRE-EMPHASIS ON OPTICAL LINKS

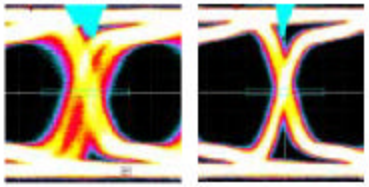

Figure 2: VC3003 also ensures that outgoing signals are free of deterministic jitter at their destination using adjustable levels of pre-emphasis. In these pictures, the positive effect of pre-emphasis on optical links is described. The picture on the left shows a 2.5Gbps electrical output of an optical receiver after 200 meters of fiber without pre-emphasis. The picture on thoright shows the effect pre-emphasis. Deterministic jitter is markedly reduced.

EFFECT OF LOW OUTPUT JITTER AND PRE-EMPHASIS ON BACK PLANE SIGNALS

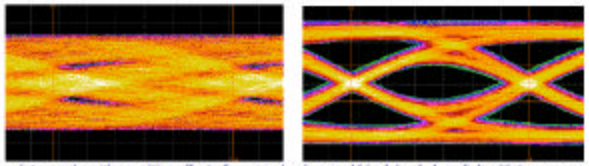

Figure 3: These pictures show the positive effect of pre-emphasis on a 44 inch backplane link with two connectors. The picture on the left shows a 3.125Gbps signal at the end of the link when no pre-emphasis is applied. The picture on the right shows the signal at the end of the link when pre-emphasis is applied.

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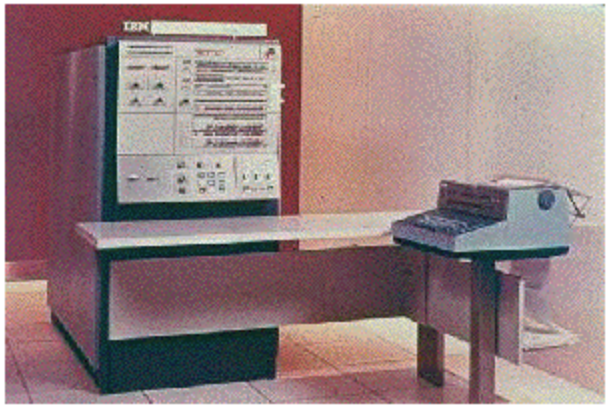
May 22, 2001
REVISION 1.3

Processor Farms



IBM 360 $1,000,000
(mainframe, 1960s)

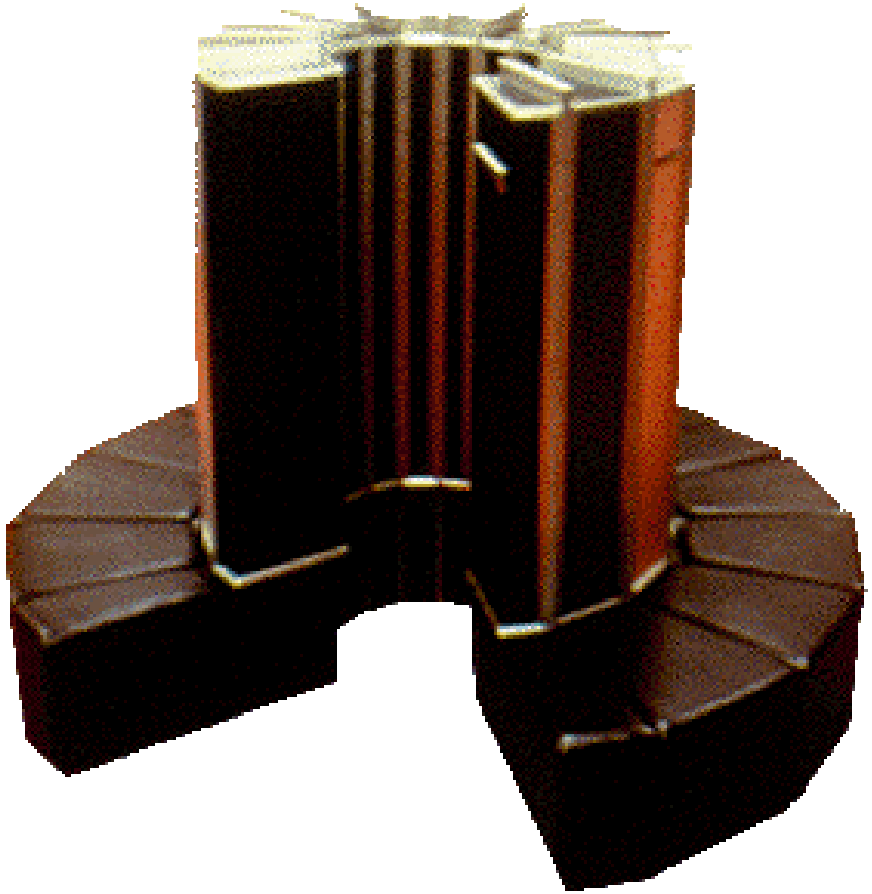
VAX 780 $100,000
(minicomputer, 1970s)

SUN 3 $10,000
(workstation, 1980s)

PC $1,000
(desktop, 1990s)

Interactive Barney $100
(embedded, ...)

A short history
of computing



Cray-1 (1976)

160 MFLOPS

$20,000,000

Generic PC motherboard (2001)

6,000 MFLOPS

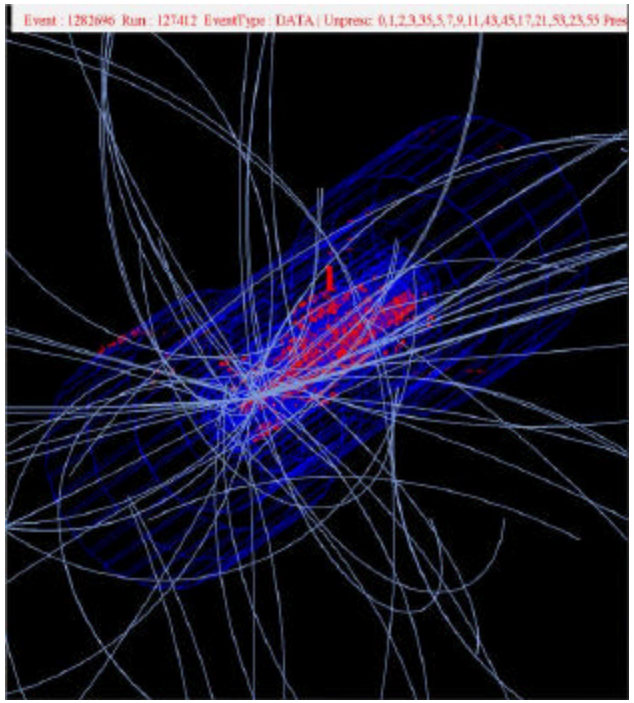
$200

Xbox (2001)

3,000 MFLOPS

$300

SETI model



Don’t build a processor farm. Just write a screen saver, post all the data on a server somewhere and invite the public to analyze it on their home PCs.

Data Storage

Tape ~ $1.00/GByte

CDR ~ $0.30/GByte

Philosophy on Standards

(opinion)

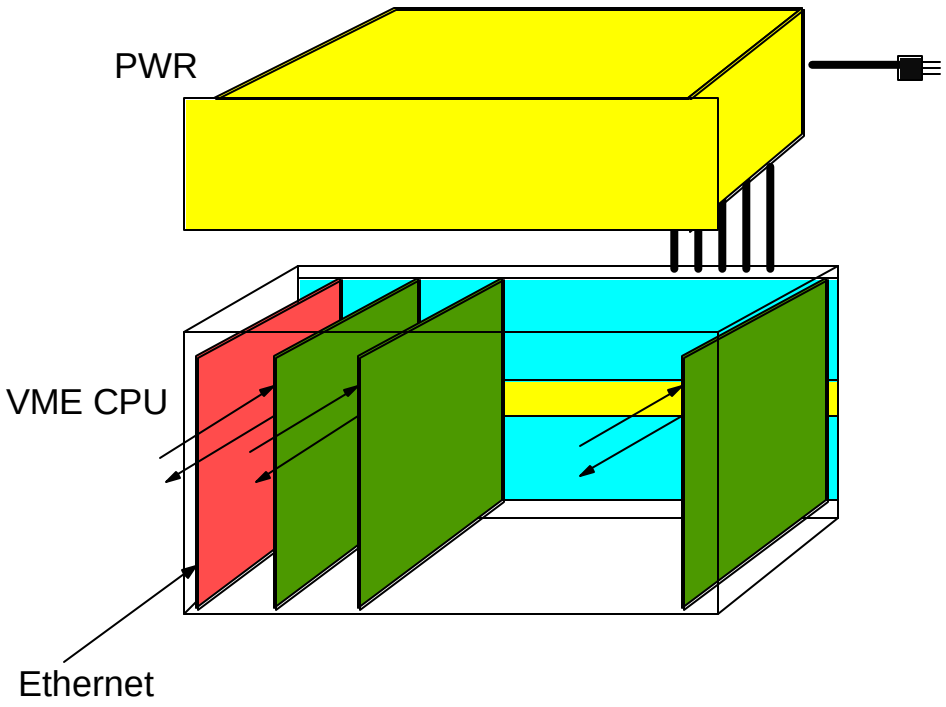
If you can't get it at Best Buy, then it probably isn't a standard.

Standards	Not Standards
Ethernet, USB, 1394	ATM, Fibre Channel, Myrinet
PCI	VME/Eurocard
Windows, Linux	VxWorks

PC Motherboard - $200

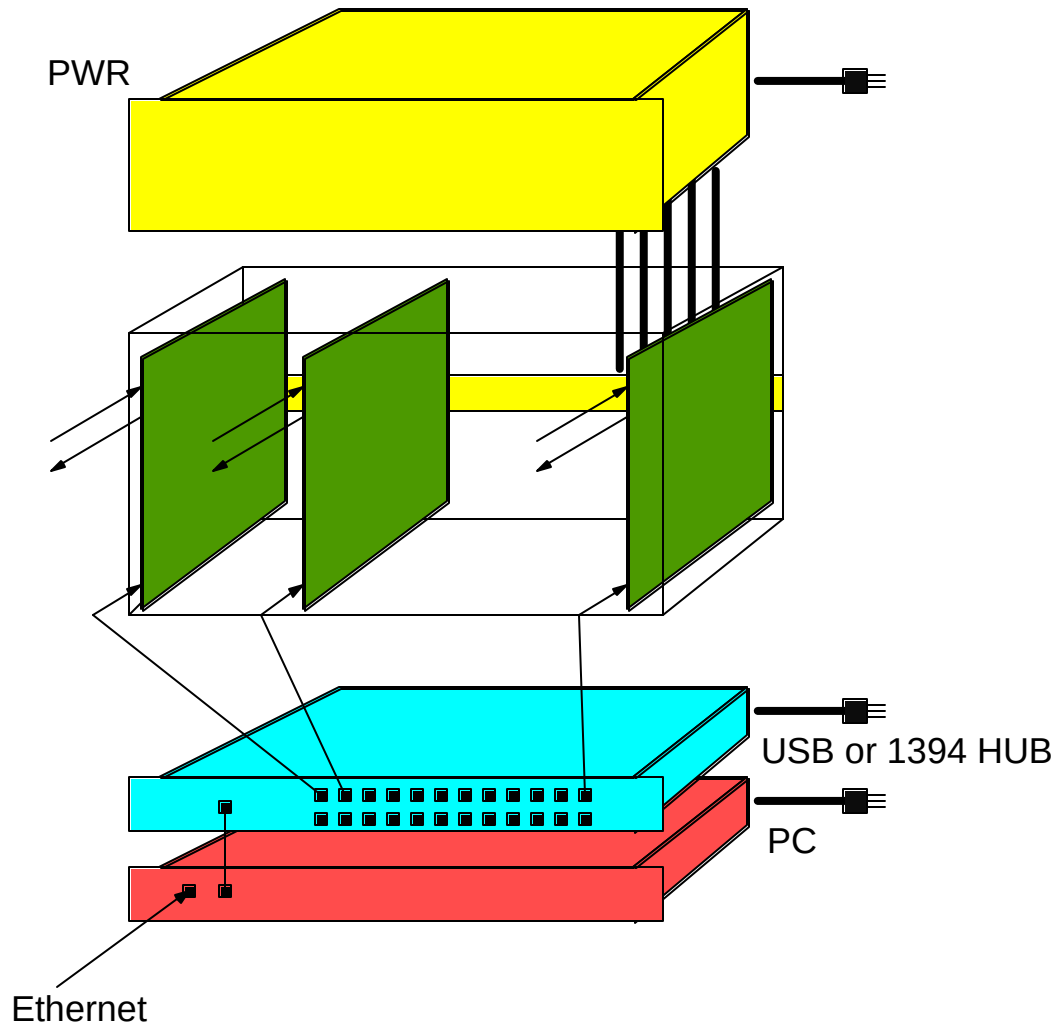
VME Processor - $2,000

Packaging



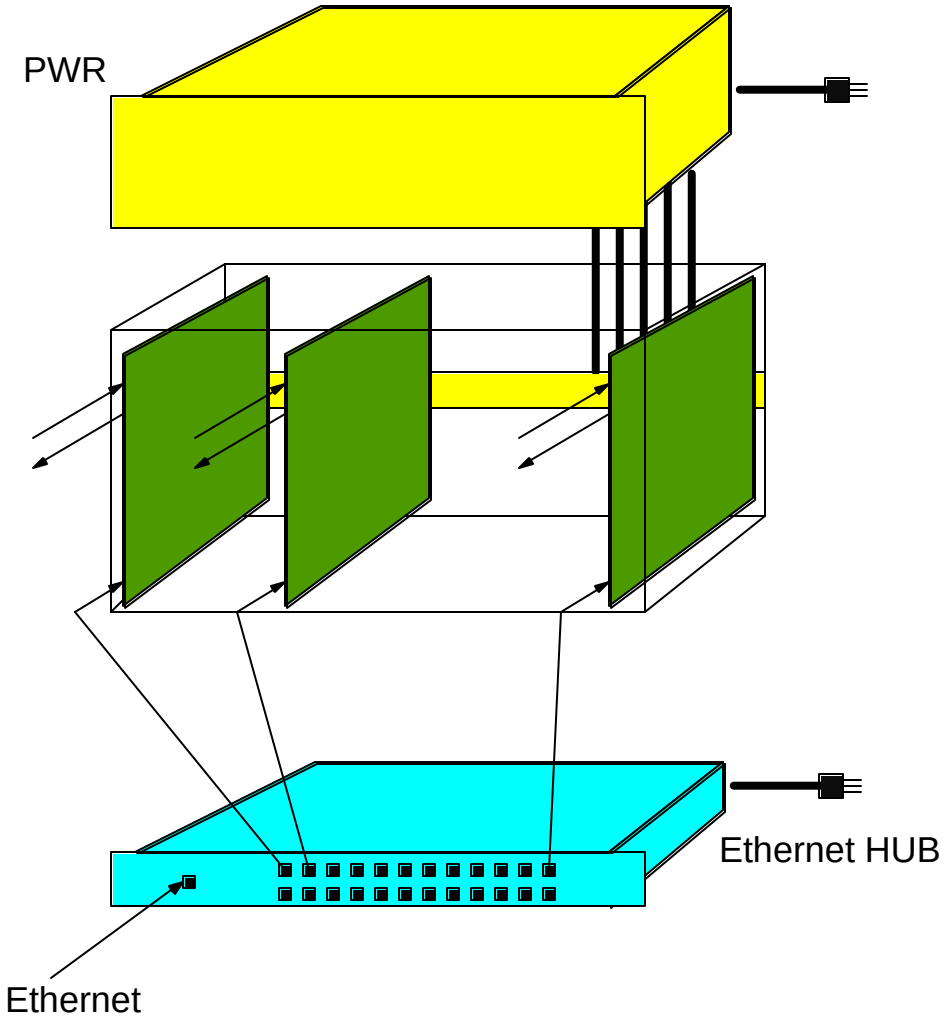
Typical Subsystem

Subrack with backplane and separate high current power supply.

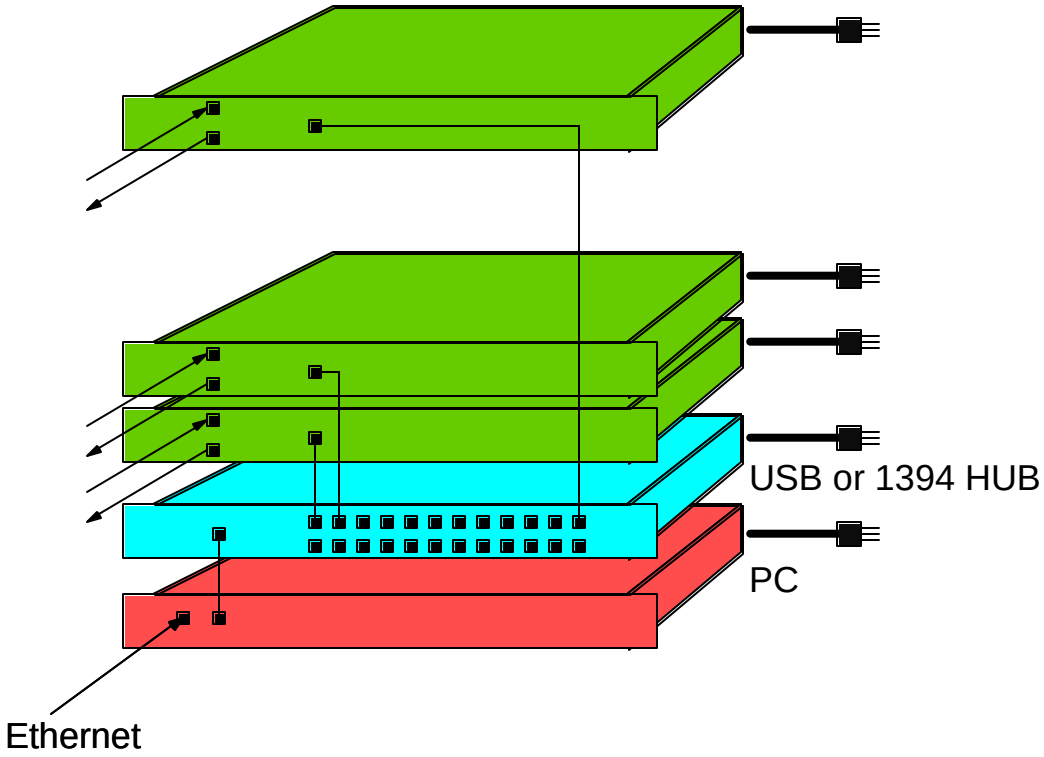


The backplane is slow and noisy, replace it with point-to-point serial connections.

The VME CPU can be replaced by a cheap PC.



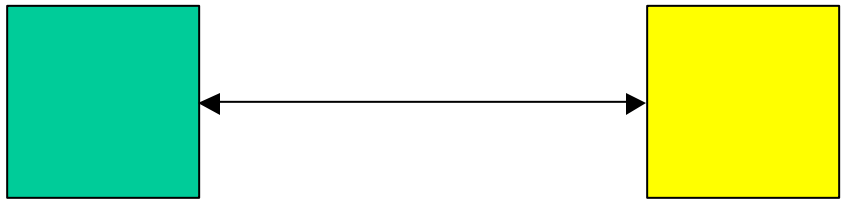
Or put a little intelligence on the front-end boards and get rid of the PC too.



Maybe distribute the power and eliminate the backplane altogether.

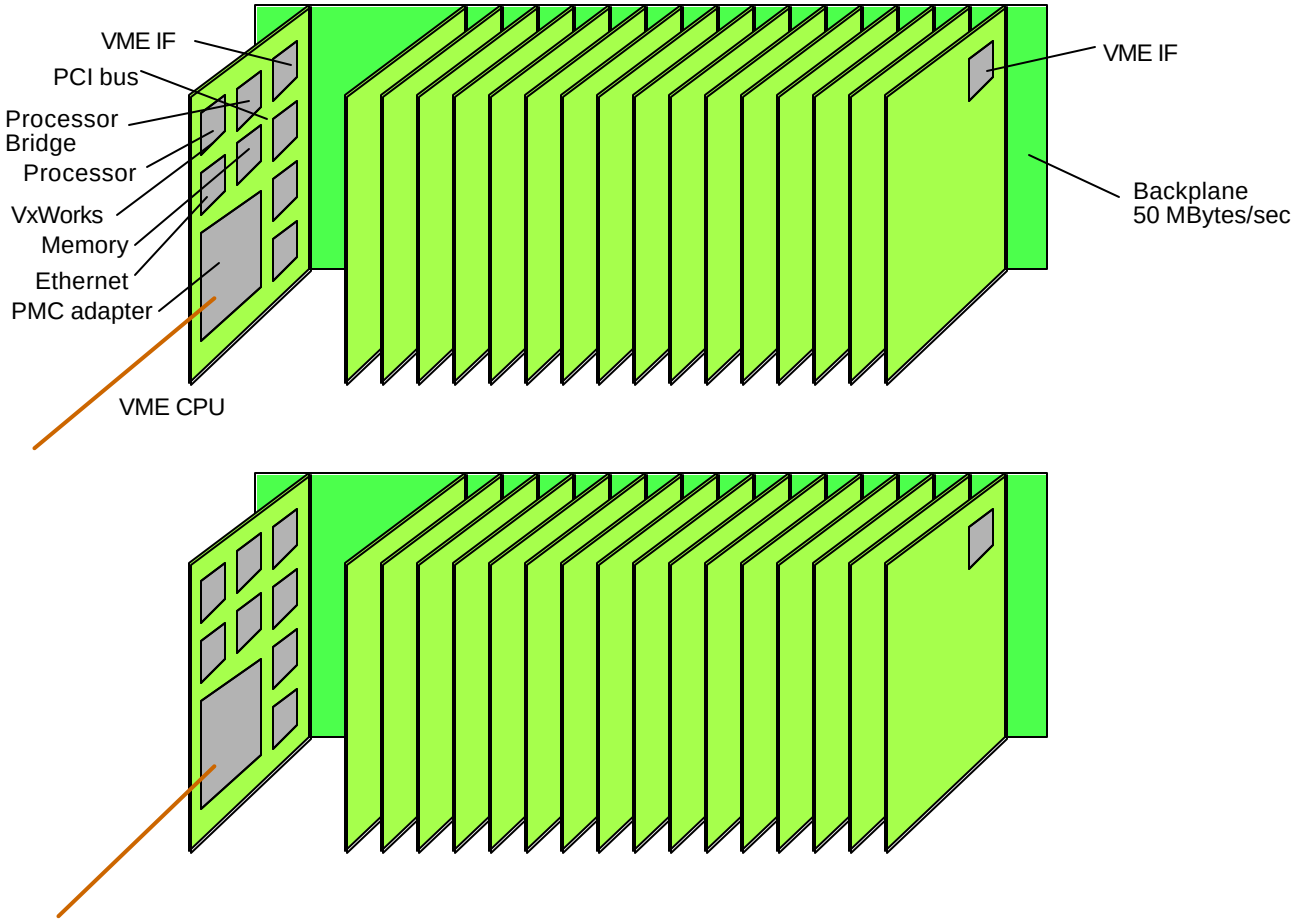
Standard power supply.

Philosophy on “Buy vs. Build”

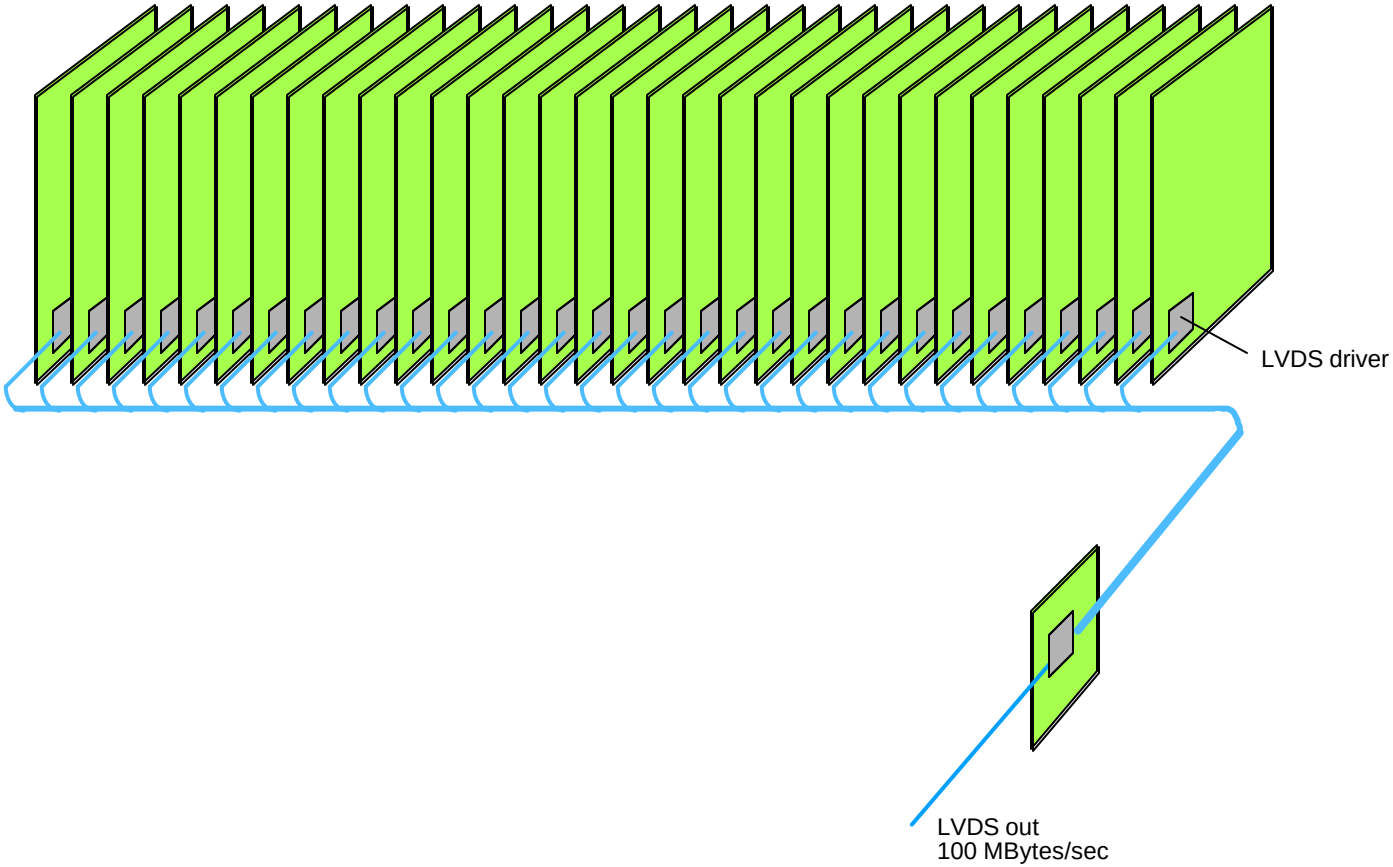


If you can buy both ends, then buy.

If you have to build one end, sometimes it’s easier to build both ends.



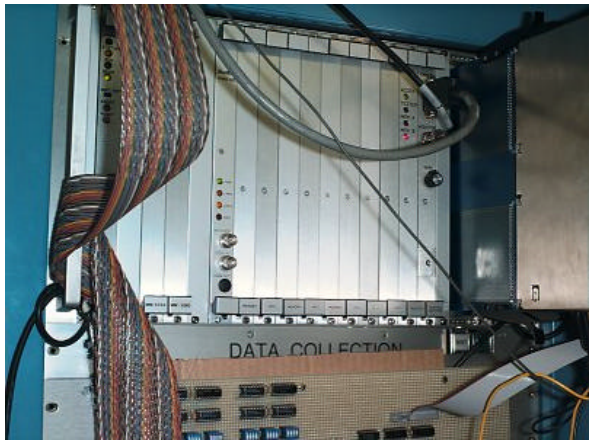
Typical … mixed (buy/build) system.

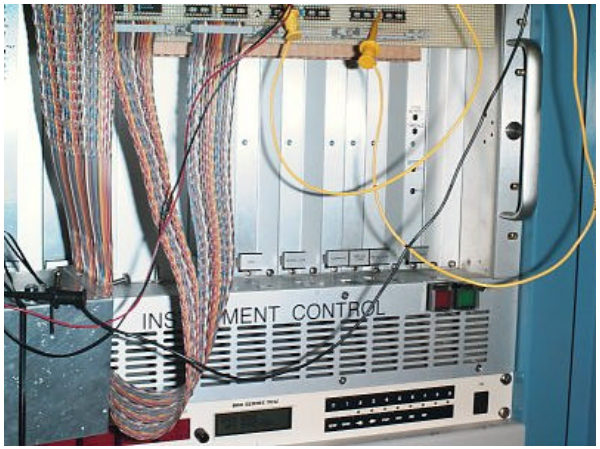


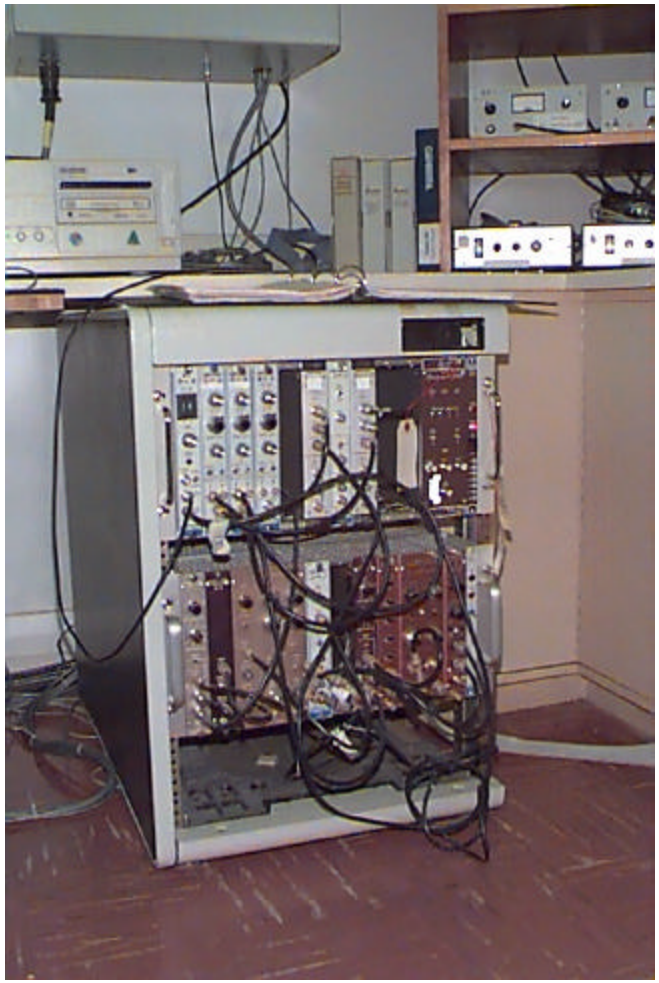
Easier? … (build/build) system.

Aesthetics

(It doesn’t have to look like this)







PC style enclosures.

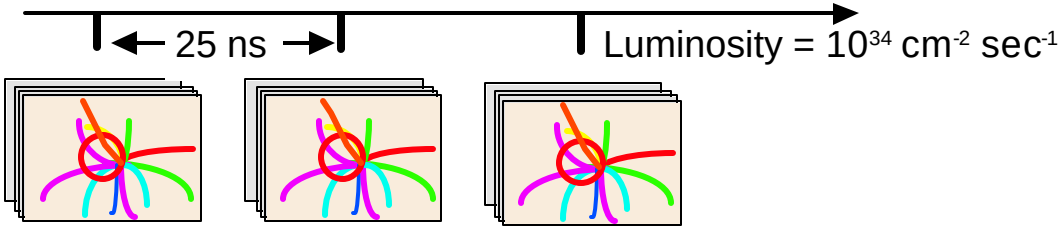
Non-eurocard rack mount

Low volume machined plastic enclosures/panels are same cost as sheet metal.

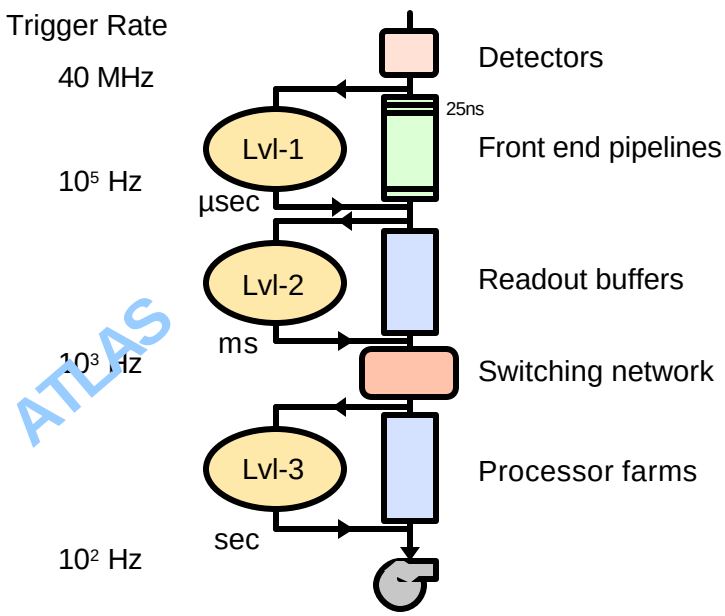
Trigger and readout structure at LHC

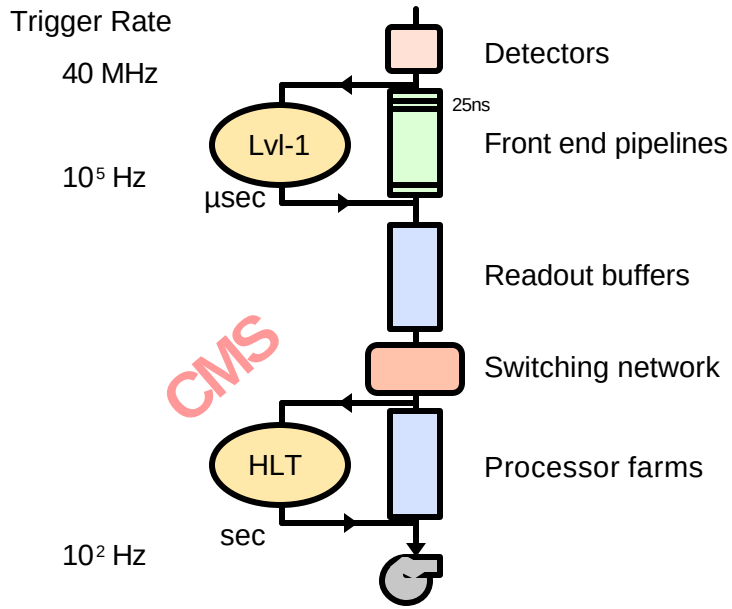
- 30 Collisions/25ns
(10^9 event/sec)

10^7 channels
(10^{16} bit/sec)



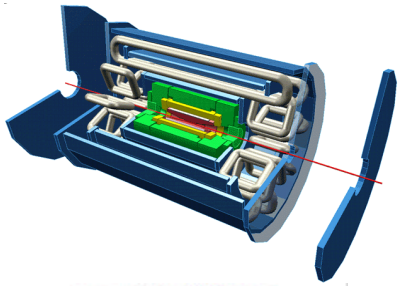
Multilevel trigger and readout systems

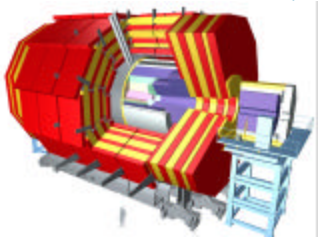


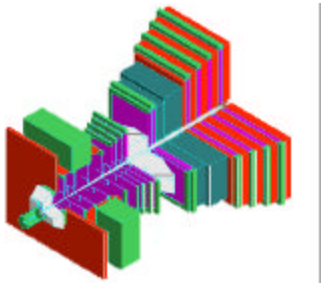


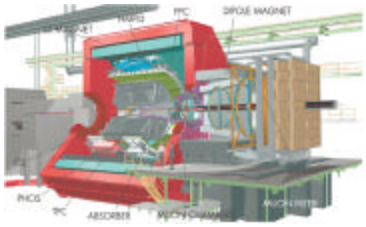
* slide borrowed from LHC

LHC experiments trigger and DAQ summary







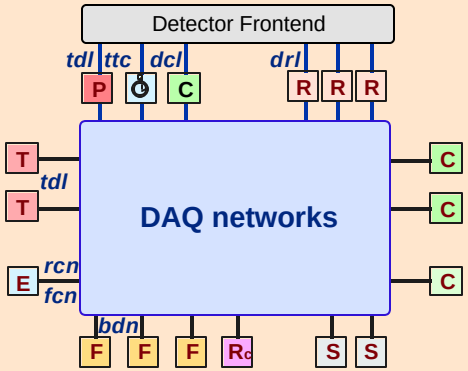


	Level-1 kHz	Event MByte	Storage MByte/s
ATLAS	100	1	100
CMS	100	1	100
LHCb	400	0.1	20
ALICE	1	25	1500

* slide borrowed from LHC

LHC trigger and data acquisition systems

LHC DAQ : A computing&communication network

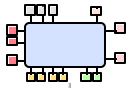


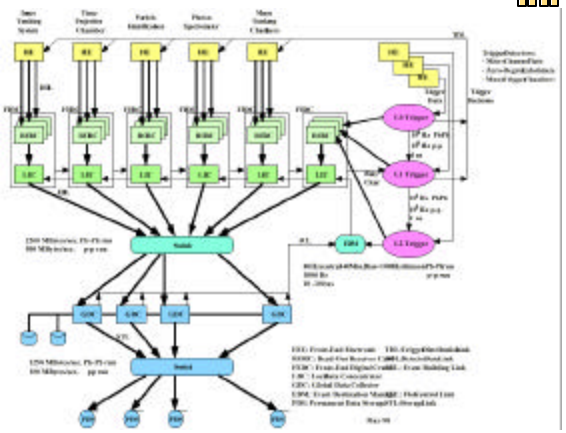
COMPUTING SYSTEMS
- **P** :Primitive generators
- **T** :Trigger processors
- **E** :Event Flow Controls
- **C** :Detector Controls
- **R** :Readout data formatters
- **F** :Event Filters
- **S** :Computing Services
- **Rc** :Run control

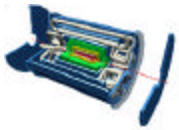
COMMUNICATION NETWORKS
- ***ttc*** :Timing and trigger signals
- ***tdl*** :Trigger data links
- ***dcl*** :Detector control links
- ***drl*** :Detector readout links
- ***rcn*** :Readout control network
- ***bcn***:Builder control network
- ***bdn***:Builder data network
- ***dsn*** :DAQ services and controls
- ***csn*** :Computing services network

A single network cannot satisfy at once all the LHC requirements, therefore present LHC DAQ designs are implemented as multiple (specialized) networks

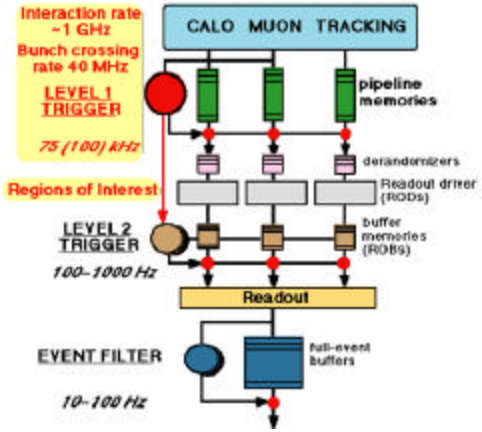
Alice



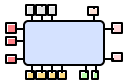


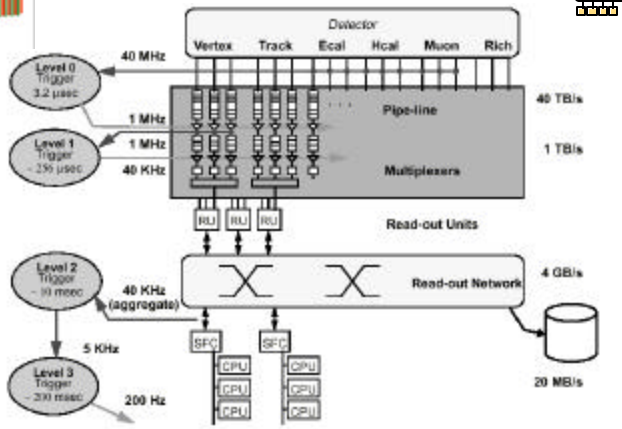


ATLAS



LHCb





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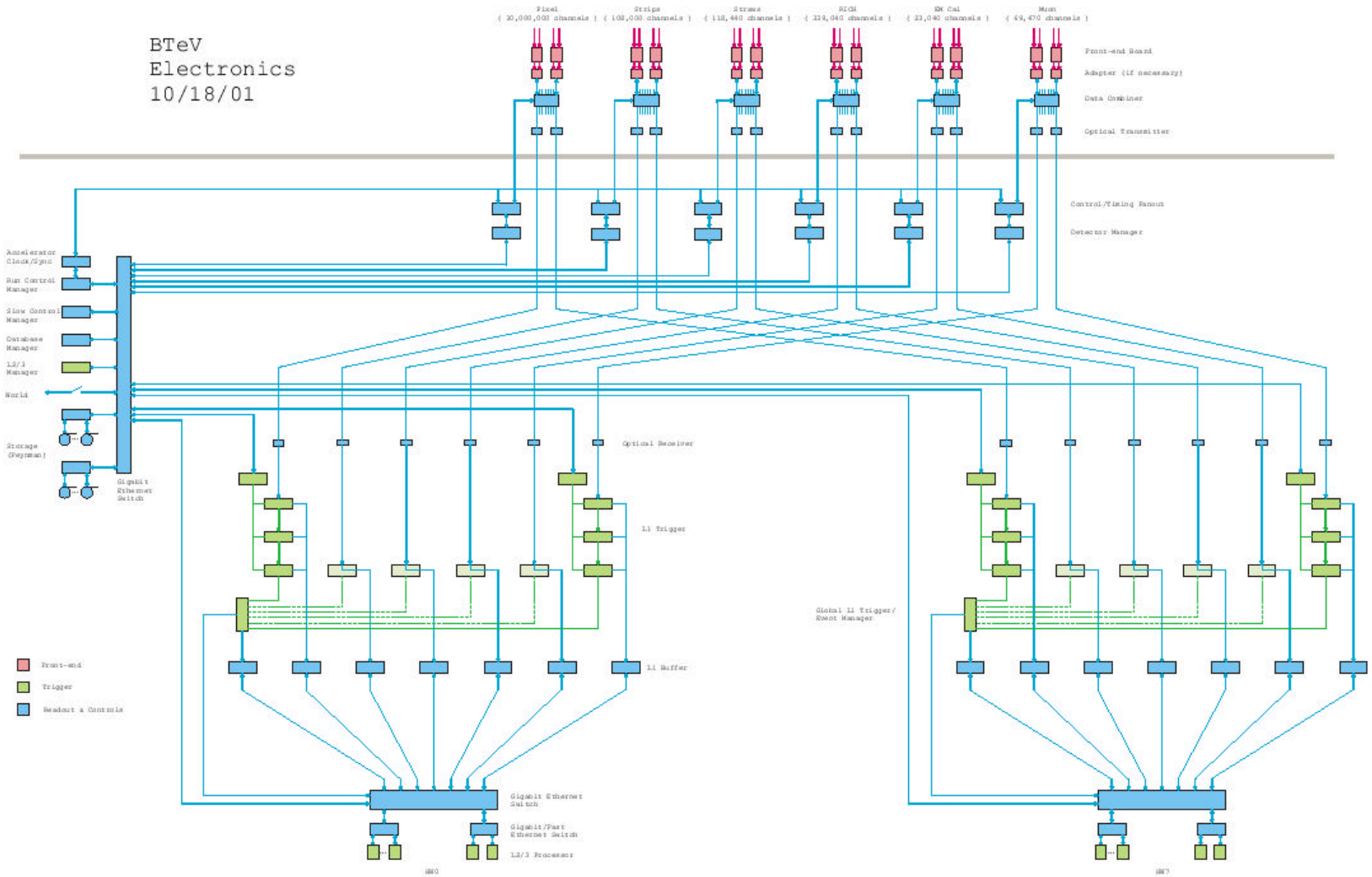
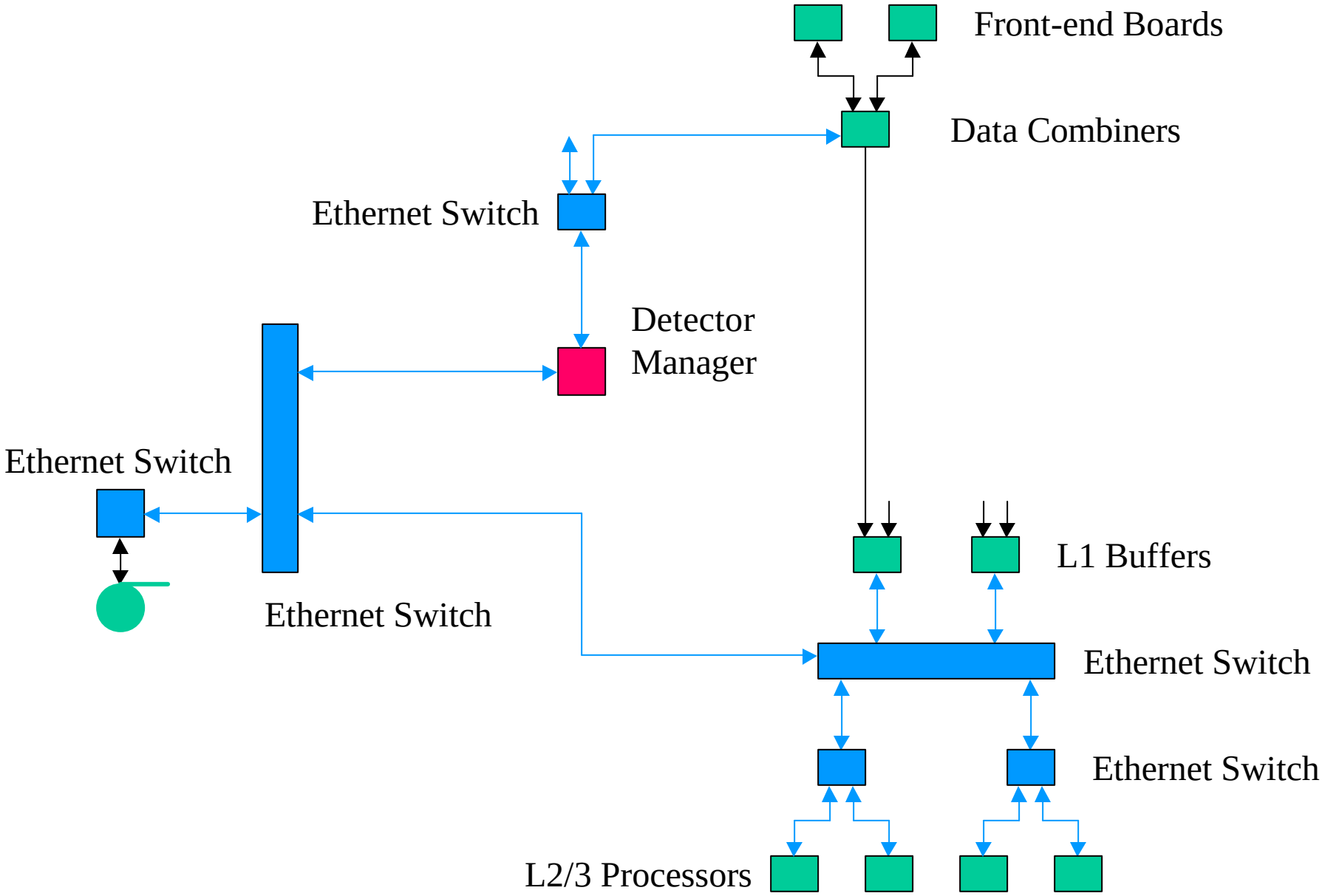
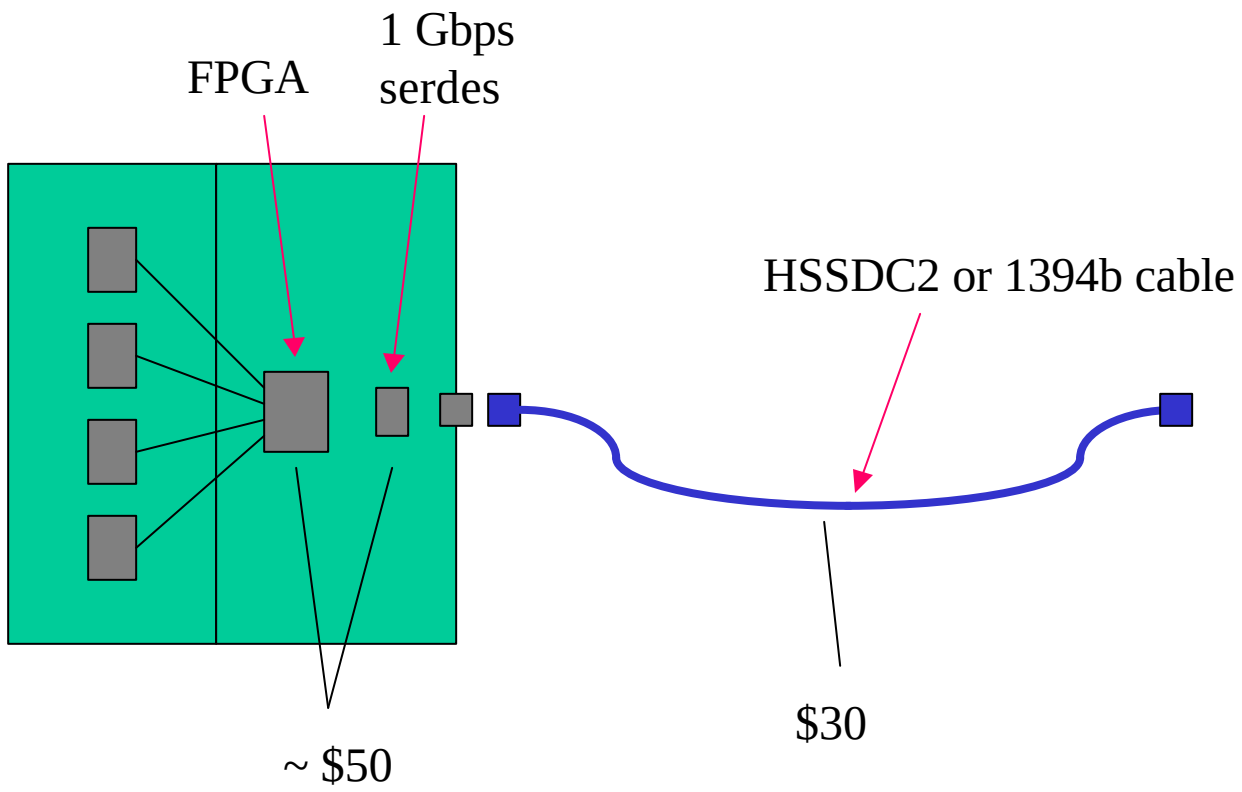


BTeV System Proposal


Front-end Boards
Data Combiners
Ethernet Switch
Detector
Manager
Ethernet Switch
Ethernet Switch
L1 Buffers
Ethernet Switch
Ethernet Switch
L2/3 Processors



Serial interface (FEB to DCB)

BTeV Features

all data transmitted off detector at crossing rate

6000 high speed serial links (1.5 TBytes/sec)

8 way split

data is not time ordered

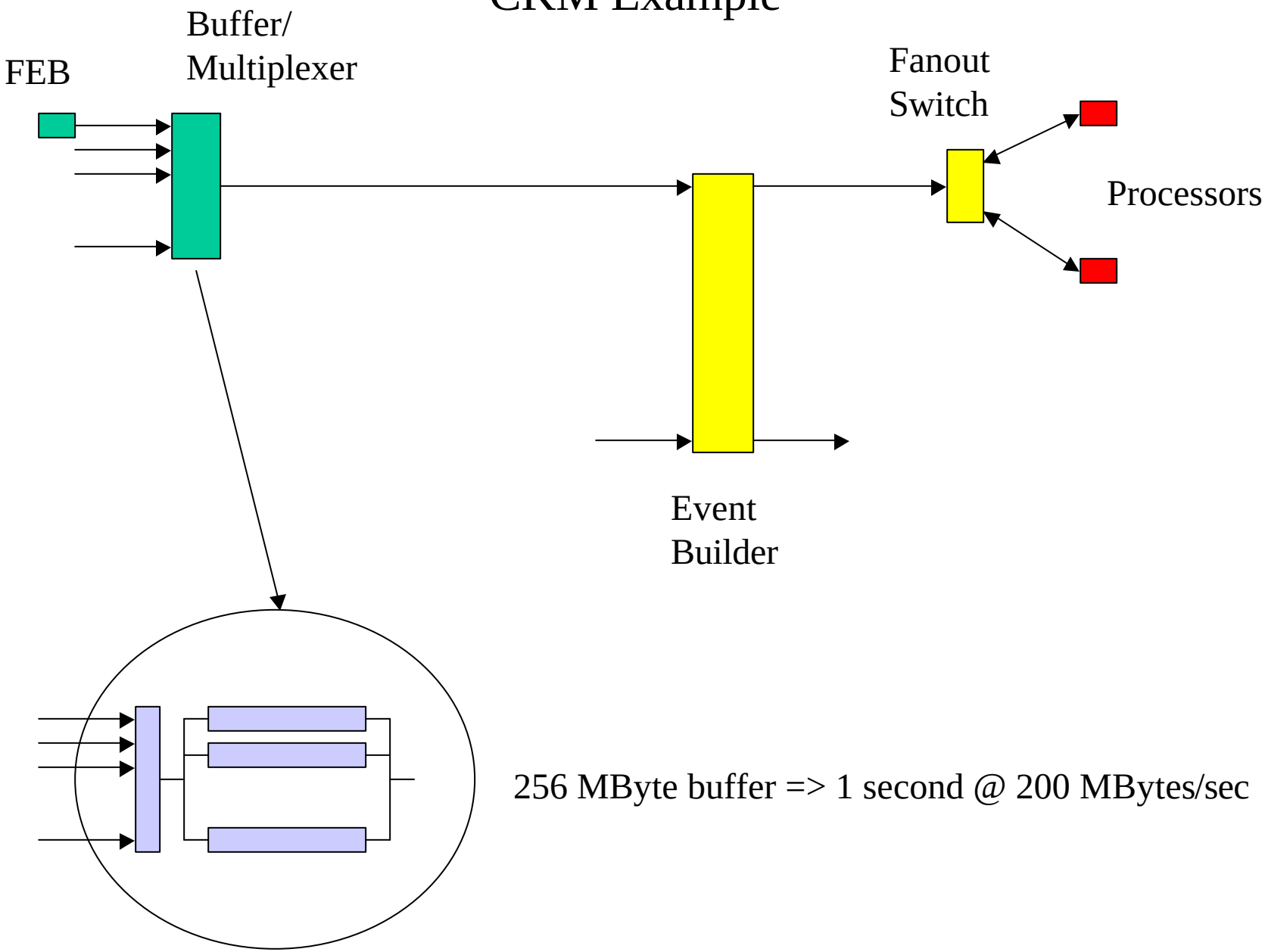
50 millisecond L1 buffer (200 GBytes)

combination FPGA/DSP for L1 trigger (100X rejection)

general purpose processors for L2/3 trigger

200 MBytes/sec to tape

CKM Example



256 MByte buffer => 1 second @ 200 MBytes/sec

Triggerless Architecture

<u>DAQ</u>

~$10/MByte/sec (DAQ component costs only, doesn't include front-end boards or processors… also doesn't include development costs for custom boards or vendor markups for commercial boards)

10 GBytes/sec => $100K
100 GBytes/sec => $1M

<u>Processing</u>

2000 Processors => $1M