



Why a Silicon detector in CDF?

A SILICON VERTEX DETECTOR FOR CDF

Presented by P. Badeschi

P. Badeschi^{a)}, S. Belforte^{b)}, G. Bellottini, L. Buzisio,
F. Cervelli, G. Chiarelli^{c)}, E. DeFabbro, M. Dell'Orso^{d)},
A. DiVirgilio, E. Focardi, P. Giacomelli, M. Giorgi,
A. Menzione, L. Riaturi, I. Scribano, P. Sestini^{d)},
A. Stefanini, G. Tonelli, F. Zetti

Istituto Nazionale di Fisica Nucleare
Pisa, Italy

Summary

The major reason for building a vertex detector for CDF is the tagging of decay vertices of particles with lifetimes in the $10^{-13}/10^{-12}$ sec. range. This is a complementary approach to heavy flavour physics with respect to missing E_T and large p_T leptons. The method can be best applied to tag hadronic decays of heavy flavours, which have the largest branching ratios, but have eluded any specific tagging until now. It also works, although with somewhat reduced efficiency, in events with a semileptonic decay. All in all it promises to be a powerful tool in the search of rather elusive processes like Higgs, top, or fourth generation quark production [1].

The additional information provided by the vertex detector will also improve significantly the resolution of the CDF central tracking system [2].

^{a)} Now at Fermi National Accelerator Laboratory.

^{b)} INFN and Rockefeller University.

^{c)} Now at Rockefeller University.

Microstrip Detectors

We plan to use detectors made out of 3 in. n-type silicon wafers with bulk resistivity in the 3000-5000 ohm-cm range and an implanted junction on the microstrip side. The electrodes are parallel to the beam axis with a pitch of 25 microns. The readout pitch is 30 μ m in the two innermost layers, 100 μ m in the two outer layers, providing an Δx resolution of 15 and 30 μ m, respectively. These resolutions can improve significantly by charge interpolation provided a sufficiently large signal to noise ratio can be retrieved.

Given the geometry of the electrodes, only the event projection in the plane transverse to the beam can be studied. Our calculations have convinced us that this is not a serious limitation.

Electronics

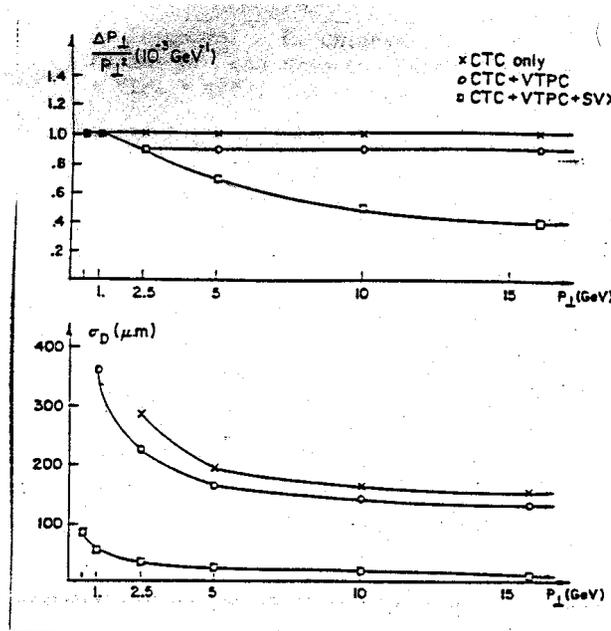
The feasibility of such a narrow pitch detector relies entirely on the existence of suitably miniaturized integrated preamplifiers. We plan to use the Minplex chip [4] to read out the strip signals. Given their very small dimensions these chips can be mounted very close to the silicon wafer (Fig. 3) and the inputs microbonded directly to the strips. 128 parallel inputs are multiplexed into a single analog serial line, with a corresponding reduction of the number of cables required.



Why a Silicon detector in CDF?

CDF note 362 (October 1985)

- Will improve significantly the resolution of the central tracking system.
- Will allow tagging of decay vertices of particle with lifetime in the 10^{-13} - 10^{-12} sec range
- All in all it promises to be a powerful tool in the search of rather elusive processes like Higgs, top, or fourth generation quark production.



- Improves momentum resolution (x 2 at large p_t).
- Improves impact parameter resolution ($\sim 20 \mu\text{m}$)



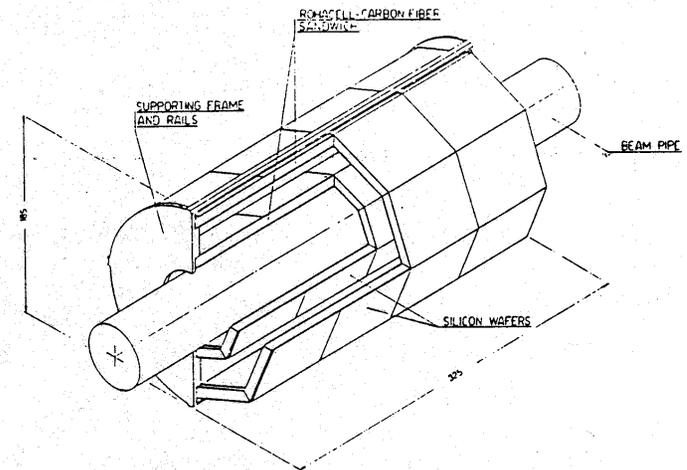
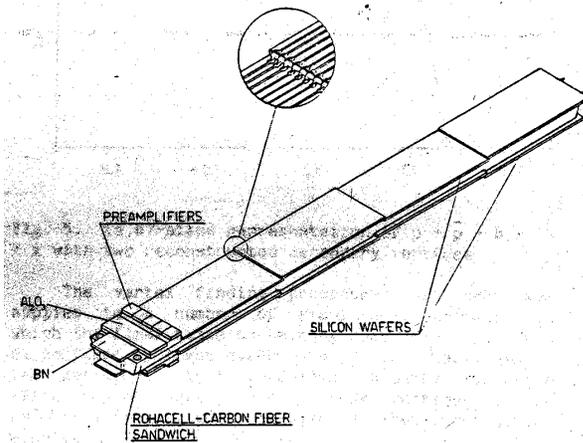
What should it look like?

CDF note 362 (October 1985)

Proposal:

► Design (conceptual)

- 2 barrels (total length of 60 cm)
- 4 octagonal layers (2 equipped on both sides)
- 37888 channels



► Use of established technology

- Feasibility relies entirely on the existence of suitably miniaturized integrated preamplifiers

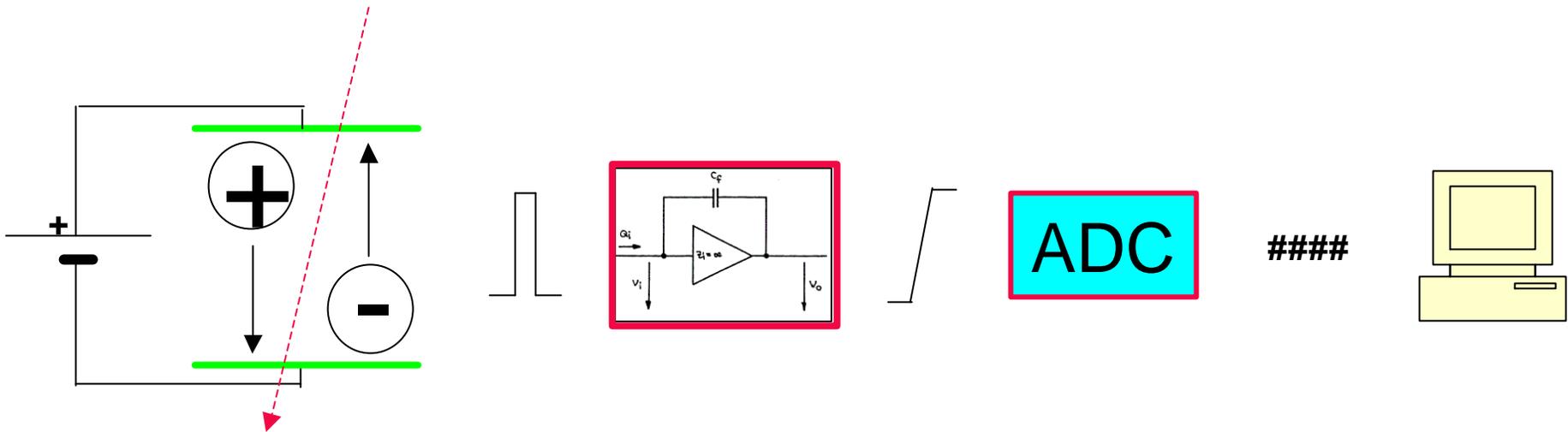


What is it?

A silicon detector is a **ionization chamber**

- Sensitive volume with electric field
- Energy deposited creates e-h pairs
- charge drifts
- Gets integrated
- Then digitized
- And finally readout and stored

(Buffering and discrimination stages could be implemented)

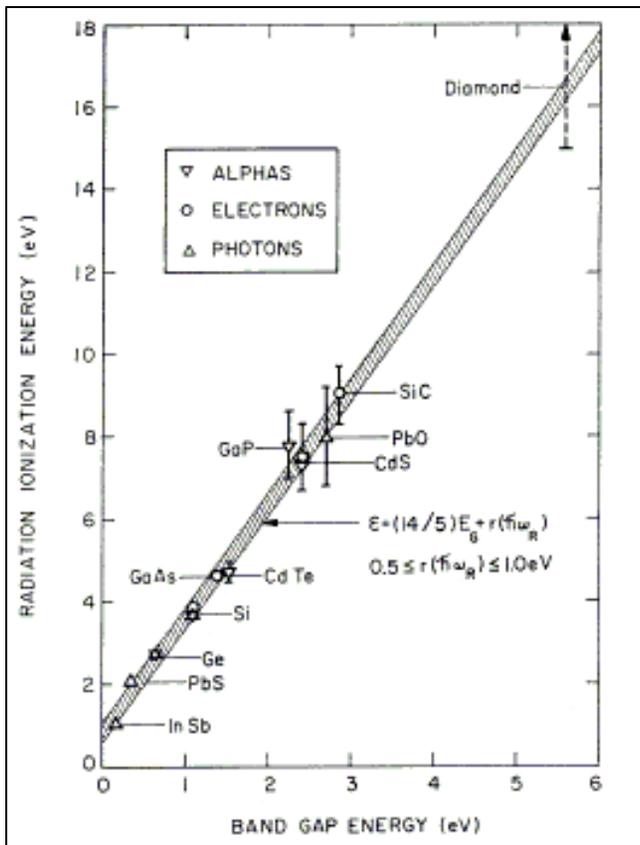




Why Silicon ?

Why solid?

- Increase charge yield dq/dE
- Fast response
- Better charge collection efficiency



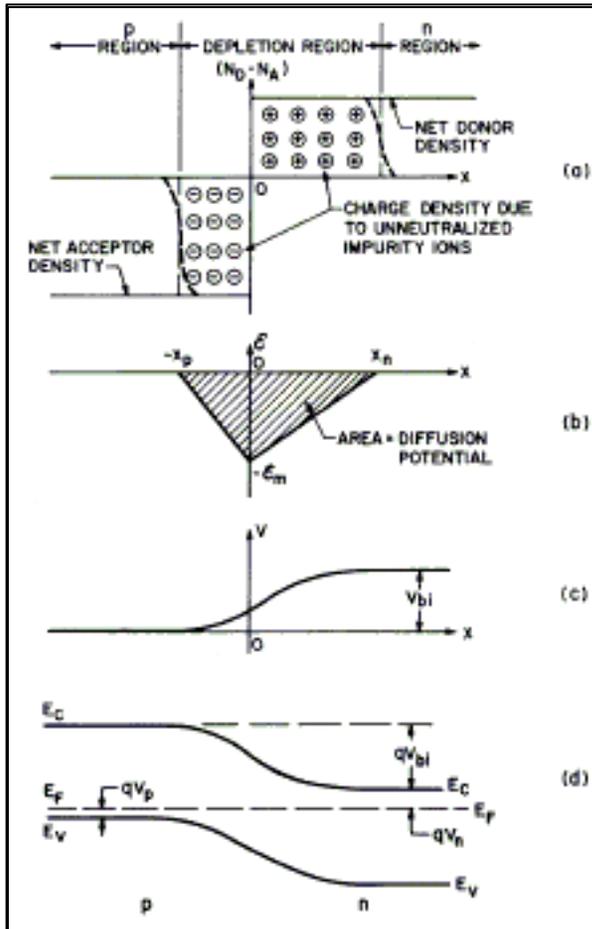
	GAS	Liquid	Solid
Density	low	Moderate	High
Atomic number Z	low	Moderate	Moderate
Ionization energy e_i	Moderate	Moderate	Low
Signal speed	Moderate	Moderate	Fast

Why semiconductor?

- Conductor
 - Small electric field
 - Large DC current
- Insulator
 - Small signal charge
- Semiconductor
 - High electric field
 - "Large" signal charge
 - Small DC current
 - Reversed biased p-n junction



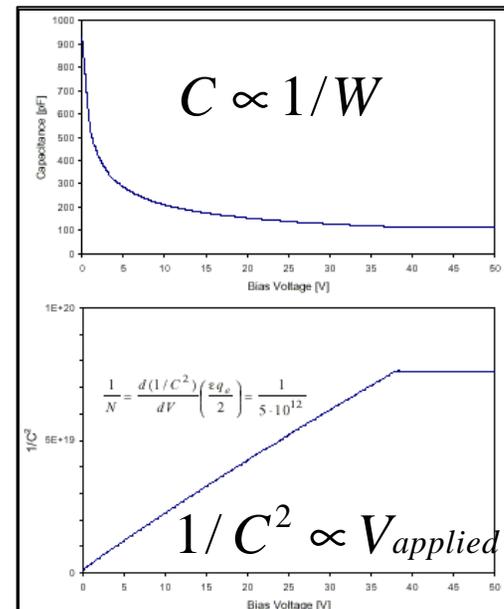
Reverse biased p-n junction (depletion)



When reverse bias is applied the silicon is depleted of the majority carriers.

In asymmetric junctions (usually $N_A \gg N_D$)

$$W = \sqrt{2\epsilon\mu_n\rho_n(V_{\text{applied}} + V_{\text{bi}})}$$

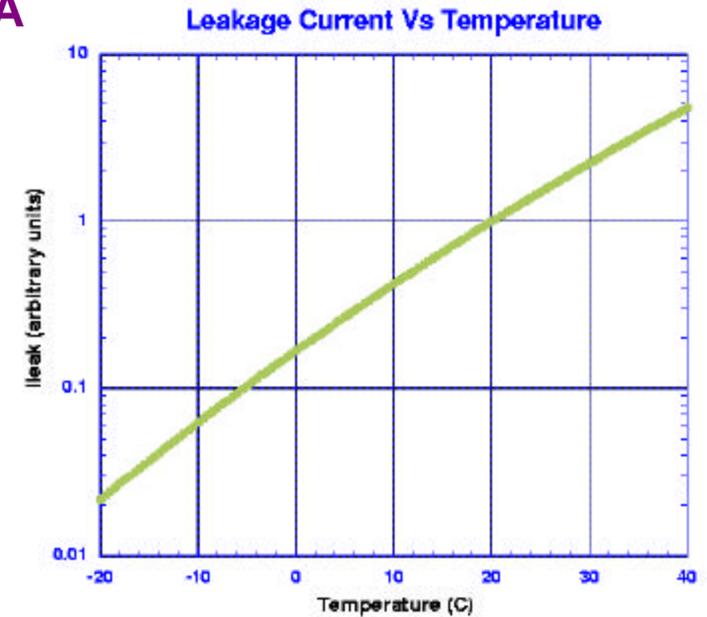
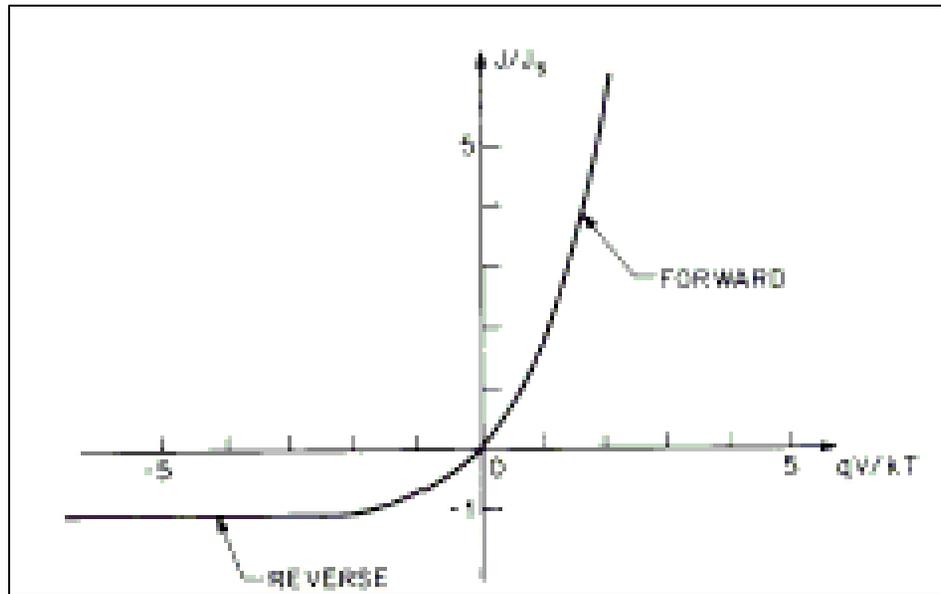




Reverse biased p-n junction ($I_{leakage}$)

Thermally generated minority carriers contribute to DC leakage current.

- Could be dominated by breakdown phenomena (induced by defects)
- Used as a macroscopic parameter for QA
- Strongly dependent on the temperature

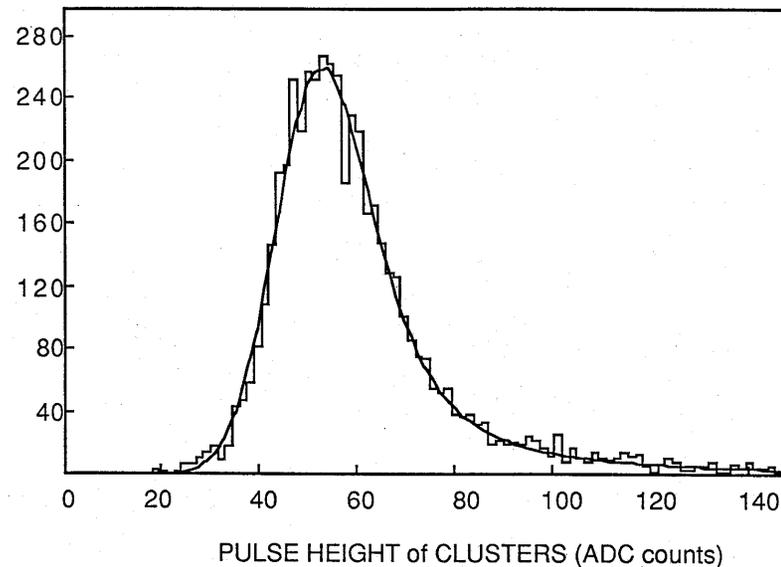


$$\frac{I_{leak}(T_1)}{I_{leak}(T_2)} = \frac{T_1^2}{T_2^2} e^{\left[\frac{E}{2k} \left(\frac{T_1 - T_2}{T_1 \cdot T_2} \right) \right]}$$



Reverse biased p-n junction (mip signal)

- mip release $390 \text{ eV}/\mu\text{m}$ & $\mathcal{E}_{\text{ionization}}=3.6 \text{ eV}$ \longrightarrow signal $\sim 4 \text{ fC}$
- Signal is proportional to the thickness of the depleted region
- $\rho=4 \text{ K}\Omega\text{cm}$ & $d=300 \mu\text{m}$ \longrightarrow $V_{\text{depl}} \sim 40\text{-}50 \text{ V}$
- Charge is available at the electrodes in time scales of 10-30 nsec





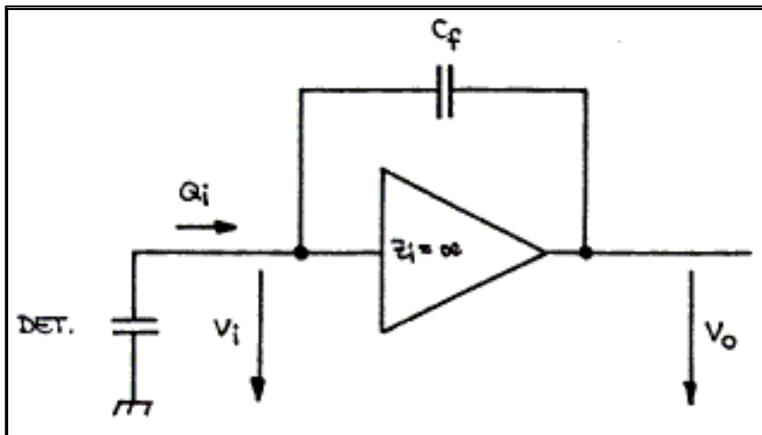
Charge sensitive amplifier (Ideal)

- Inverting voltage amplifier
- Voltage gain

$$dV_o/dV_i = -A \Rightarrow v_o = -Av_i$$

$$v_f = (A + 1)v_i$$

$$Q_f = C_f v_f = C_f(A + 1)v_i$$



$$Q_i = Q_f \quad (\text{since } Z_i = \infty)$$

$$C_i = Q_i/v_i = C_f(A + 1)$$

$$A_Q = \frac{dV_o}{dQ_i} = \frac{-A \cdot v_i}{C_i \cdot v_i} = \frac{-A}{C_i} = \frac{-A}{A+1} \cdot \frac{1}{C_f}$$

- Out of Q_t signal only Q_i is measured

$$\frac{Q_i}{Q_t} = \frac{C_i}{C_t} \cdot v_i = \frac{C_i}{C_t} \cdot \frac{Q_t}{C_i + C_{det}} = \frac{1}{1 + \frac{C_{det}}{C_i}} \approx 1 \quad (\text{if } C_i \gg C_{det})$$

$$A_Q \approx \frac{1}{C_f} \quad \text{if } (A \gg 1)$$



How is it read out ?



EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH

CERN-EP/85-148
C.R. - 511-562-85
September 25th, 1985

FIRST RESULTS FROM A SILICON-STRIP DETECTOR WITH VLSI READOUT

Giuseppina Anzivano, Roland Horisberger, Leonardus Hubbeling, and Bernard Hyams
CERN, Geneva, Switzerland

Sherwood Parker and Alan Breskione
University of Hawaii, Honolulu, Hawaii

Alan M. Lisse
University of California at Santa Cruz, Santa Cruz, California

James T. Walker
Stanford University, Stanford, California

Nils Bingsjö
University of Uppsala, Sweden

ABSTRACT

A 256-strip silicon detector with 25 micron strip pitch, connected to two 128 channel NMOS VLSI chips (Microplex), has been tested using straight through tracks from a Ruthenium beta source. The readout channels have a pitch of 47.5 microns. A single multiplexed output provides voltages proportional to the integrated charge from each strip. The most probable signal height from the beta traversals is approximately 14 times the rms noise in any single channel.

(Submitted to Nuclear Instruments and Methods)

- MICROPLEX amplifier in use by MARKII (SLC) and DELPHI (LEP)

- CDF note 475 (May 1986) evaluate the MICROPLEX for use in SVX

➤ Tevatron implies:

- Longer interaction region (30 cm)
 - Longer strips = more capacitive load
 - S/N too low
- Shorter time between collision (3.5 μsec)
 - Not possible to run with “pulsed” power

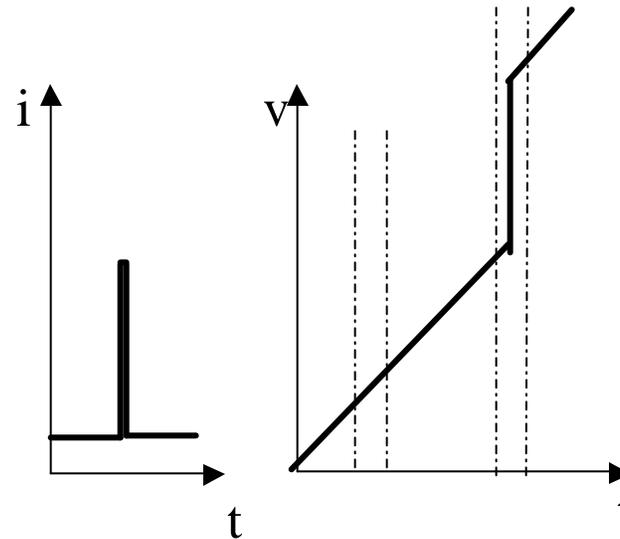
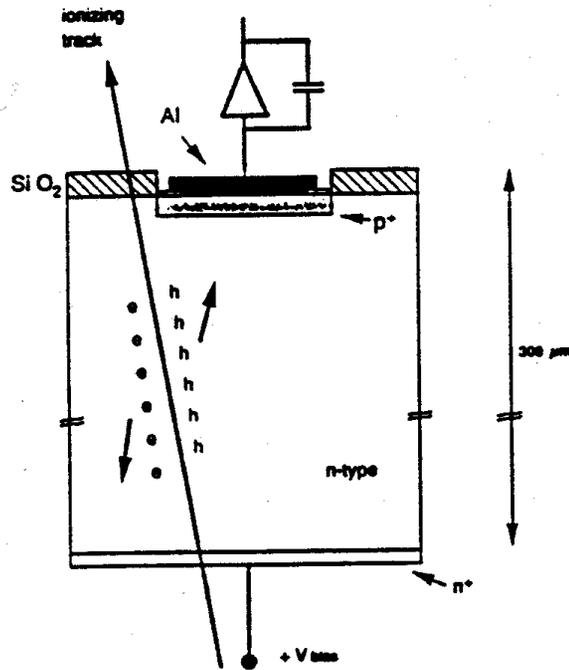
➤ It is necessary to develop a readout chip dedicated to the Tevatron constraints

➤ Beginning of the SVX saga (SVXC, SVXD, SVXH, SVX2, SVX3.....SVX4?)

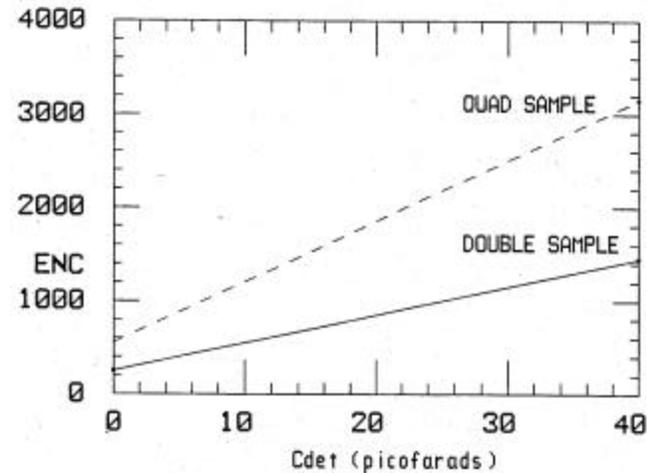


SVX, DC coupled sensor and SVXD chip

Leakage current is integrated with the signal and has to be subtracted

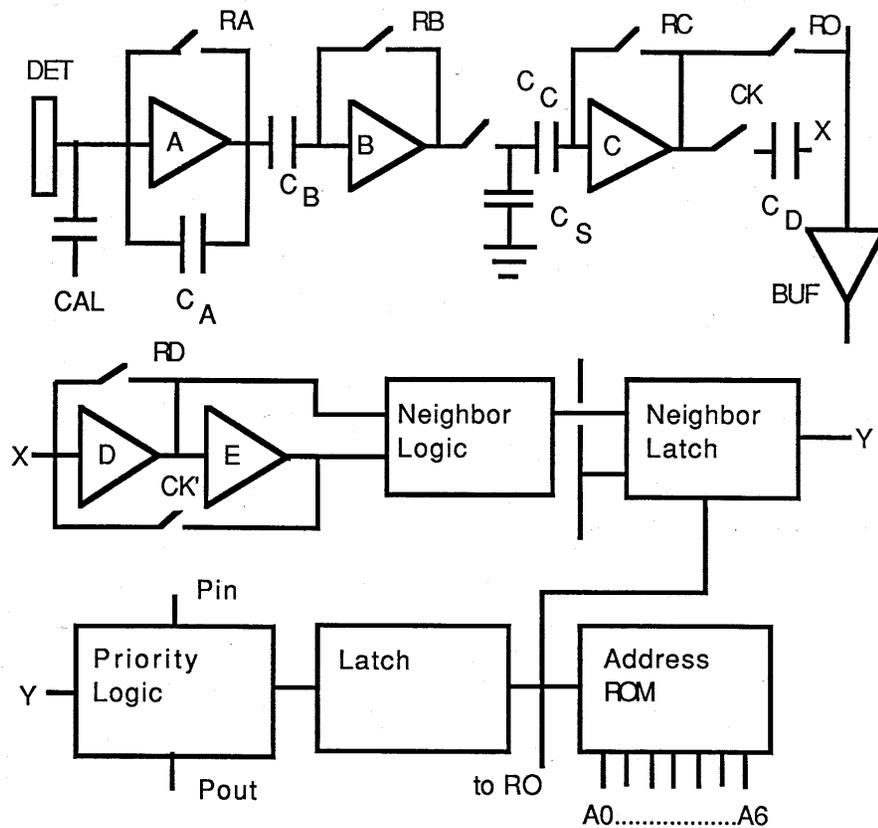


quadruple correlated sample





SVXD readout chip



- S/N >10 with 30 pF load.
- P < 2.5mW/ch
- Total readout time < 1 msec
 - CMOS 3 mm
 - 128 channels
 - Good charge collection
 - C_f=0.3pF and an open loop gain 2000 implies C_i=600 pF >>C_{det}
 - Sample and hold stage
 - Sparse logic
 - Comparator and latch
 - 1st Sample and hold stored on CC (leakage+threshold)
 - 1st Sample and hold stored on CS (leakage+signal)
 - Difference set the latch
 - **Readout time is set by occupancy not by number of channels**



Noise components

Total Noise $ENC = \sqrt{N_C^2 + N_{shot}^2 + N_R^2}$

“Capacitance” noise

$$N_C = A + kC$$

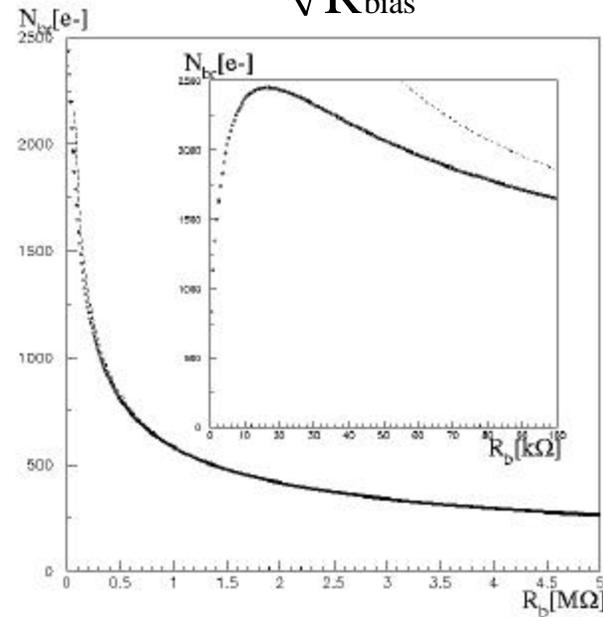
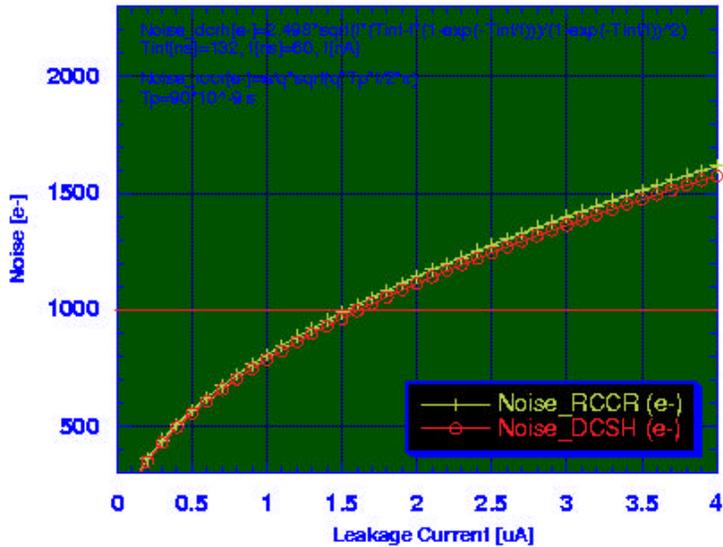
Shot noise

$$N_{shot} \propto \sqrt{I_{leak}}$$

Thermal noise

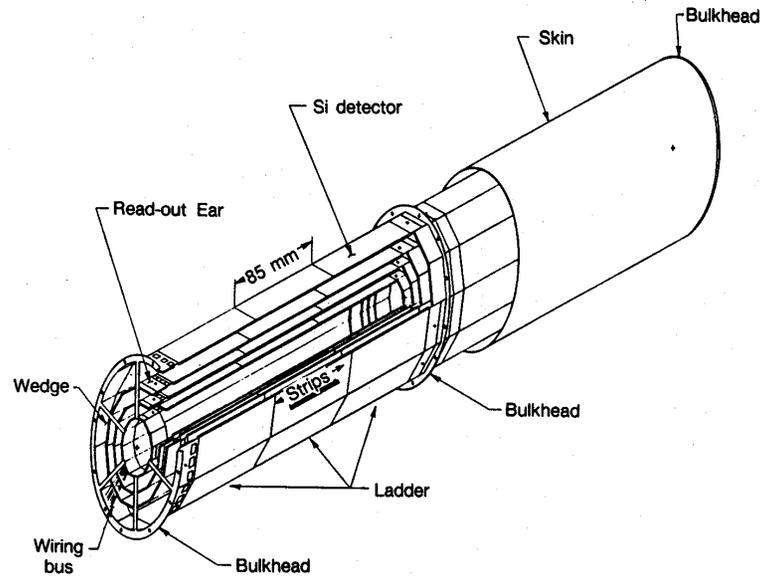
$$N_R \propto \frac{1}{\sqrt{R_{bias}}}$$

Noise vs leakage current

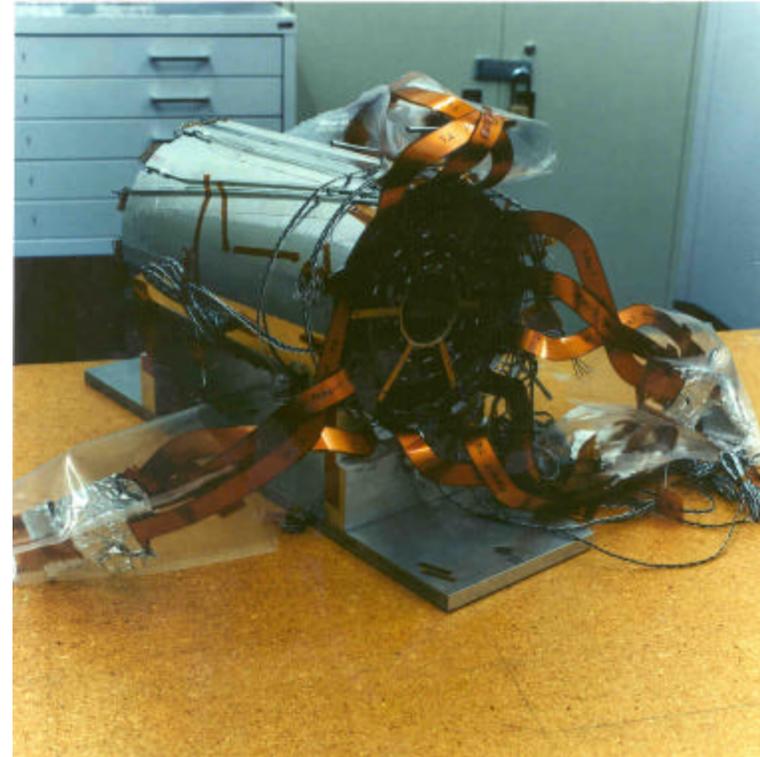




SVX was built and did its job



XBL 888-9722



- Very different from initial proposal, took 30 pb⁻¹ data (1192-1993)
- L0 S/N decreased from 9:1 to 6.5:1 but still good over Run 1a
- Run 1b target luminosity ~100 pb⁻¹ (SVX has to be replaced)



“Proposal For an Upgraded CDF detector”

Was published on October 9, 1990. Here are the last few sentences of the SVX chapter:

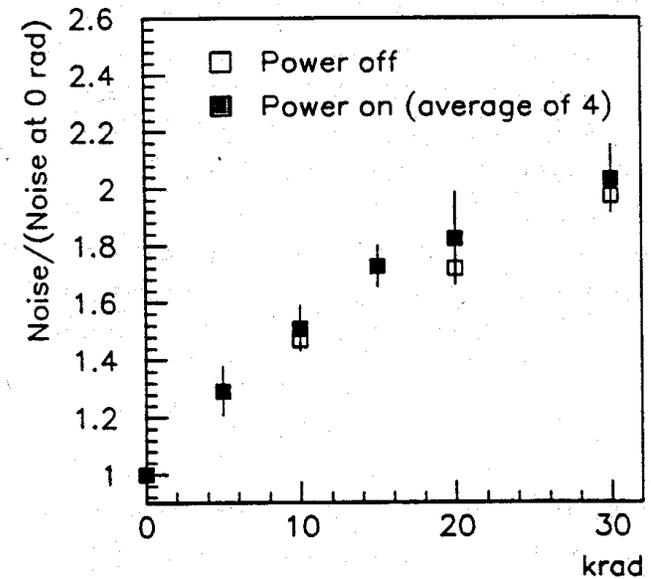
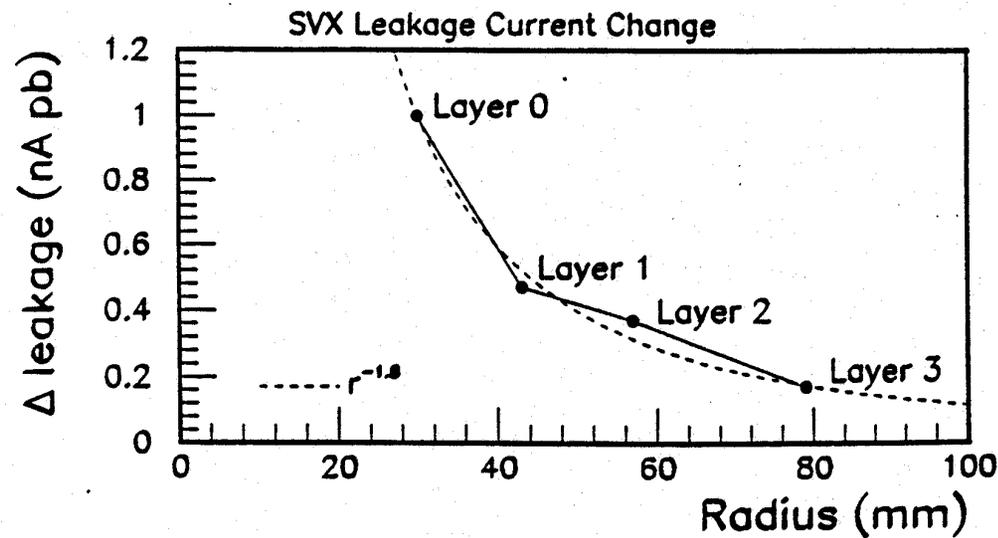
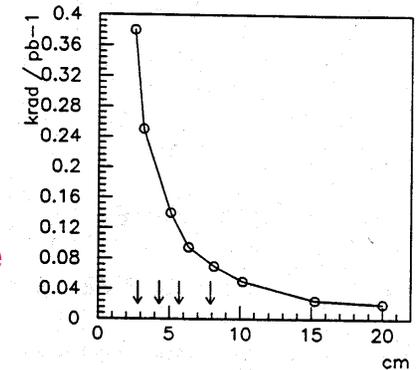
..... a program of high sensitivity B physics would be greatly enhanced by the addition of a secondary vertex trigger Promising schemes with associative memories are under development and we anticipate employing one for the 1993 run

Vertexing can be significantly improved by an inner layer close to the interaction point. Simulation studies show a 30 % increase in B tagging efficiency for an inner layer at a radius of 0.5 inches.



SVX to SVX' transition

- CDF note 1391: "... the "high" level of radiation ... the associated increase of leakage current would bring the preamplifiers out of range"
 - DC to AC coupled sensors
- CDF note 1741: "We conclude it will be necessary to replace the first two layers of the silicon vertex detector at CDF due to radiation damage after an accumulated dose of 30 krad"
 - SVX D to SVX H readout chip (rad hard)

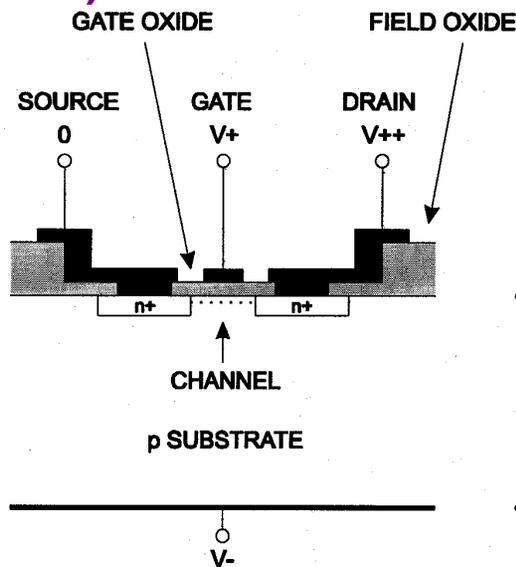
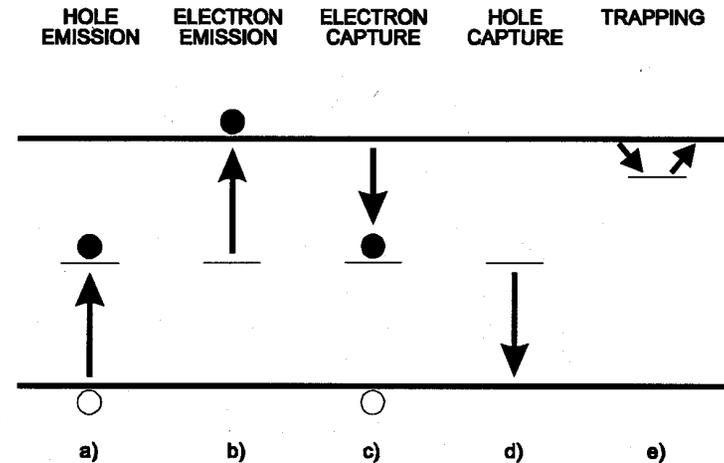




Radiation damage (2 mechanisms)

● Displacement damage

- Leakage current increase linearly with the absorbed dose
- Change in effective doping concentration (changes in V_{dep})
- Charge trapping (signal loss)

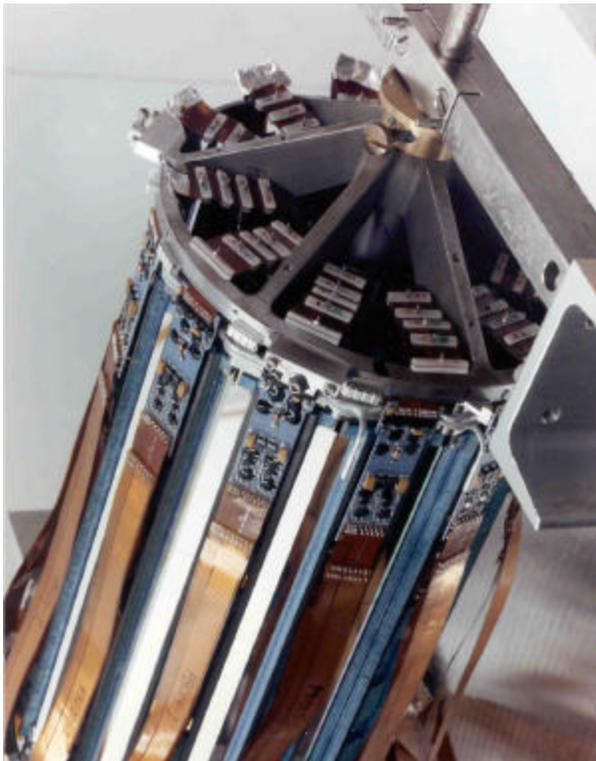


● Ionization damage

- Threshold shift
- Noise and gain deterioration
- Decrease surface mobility

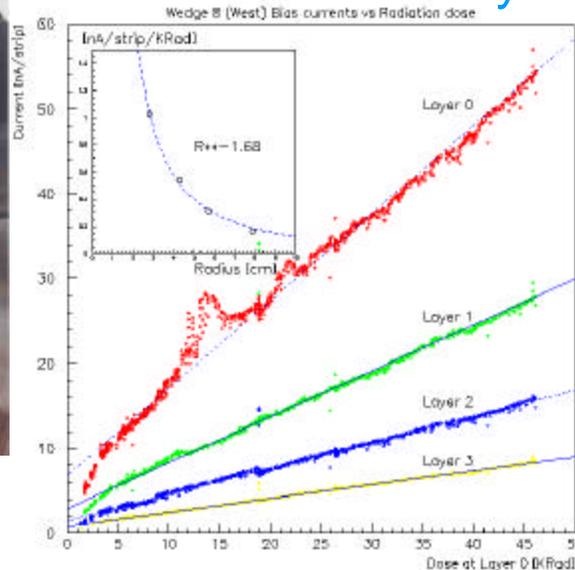


SVX' done!

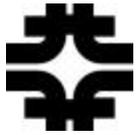


Features	SVX	SVX'
Silicon	DC-coupled	AC-coupled (FOXFET BIASED)
R-O chip	R.S. SVXD	R.H. SVXH
Sampling_i	Quadruple	Double
Noise	2200 ENC	1300 ENC
Radiation limit	15-20 krad	1 Mrad (chip)

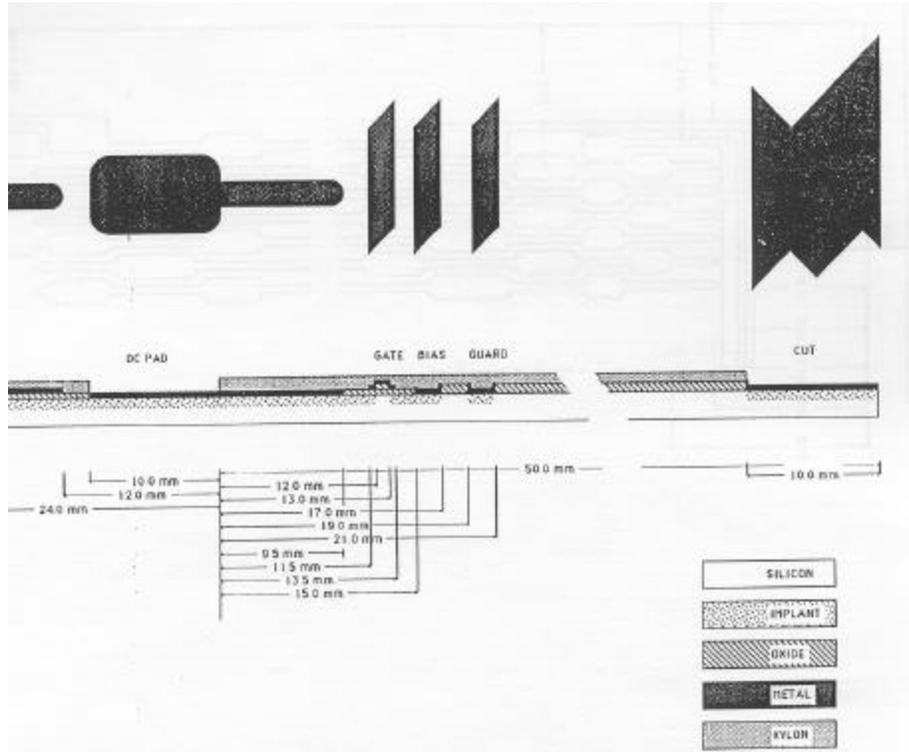
Mechanically almost the same!



Supposed to die of
shot noise when
 $I_{leak}/strip \sim 1\mu A$.
This should have
been way bigger than
the expected $100 pb^{-1}$

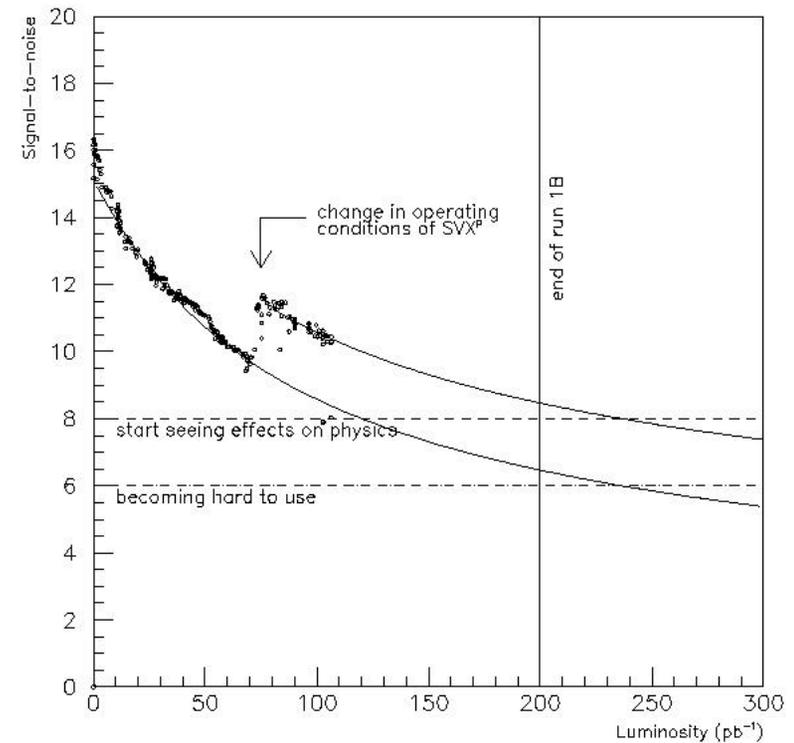


Excess noise



Mechanism not fully understood but clearly due to the FOXFET biasing structure. Future polysilicon resistors.

The FOXFET ruined the party.
Unexpected noise contribution.
Still SVX' made it to the end of RUN1b





SVX' to SVXII big step!

- Increase acceptance and coverage of luminous region along beam
 - Previous CDF vertex detectors covered interactions within $|z| < 0.27$ m, New silicon detectors designed to cover $|z| < 0.43$ m
 - Interaction region expected to be more concentrated in z in Run II
 - Increase silicon angular acceptance to cover approximately $\eta \approx 2$.
 - Overall effect should be approximately a factor of 2 increase in acceptance for particles with good tracking and vertexing
- Improve top tagging for high- p_T physics:

	Single tag eff. (%)	Double tag eff. (%)
SVX' + CTC (Run I)	37.6 ± 1.0	6.8 ± 0.5
SVXII + COT	46.7 ± 1.1	8.7 ± 0.6
SVXII + ISL + COT	60.1 ± 1.0	15.1 ± 0.8

- Improve B physics capability of the experiment



SVX' to SVXII big step!

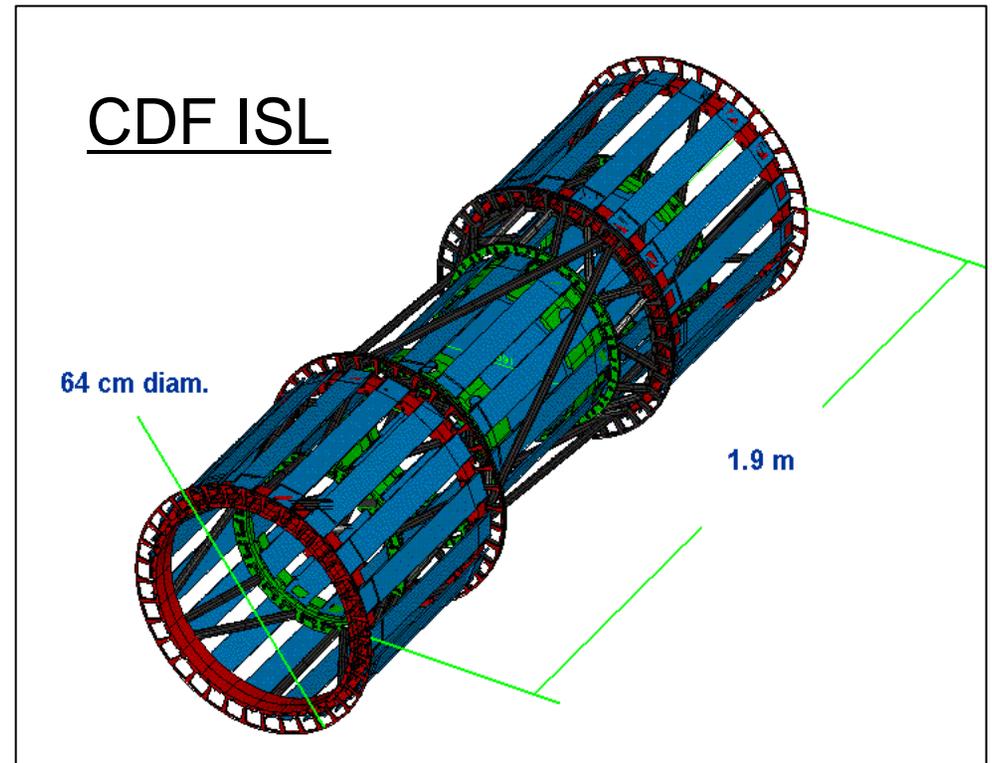
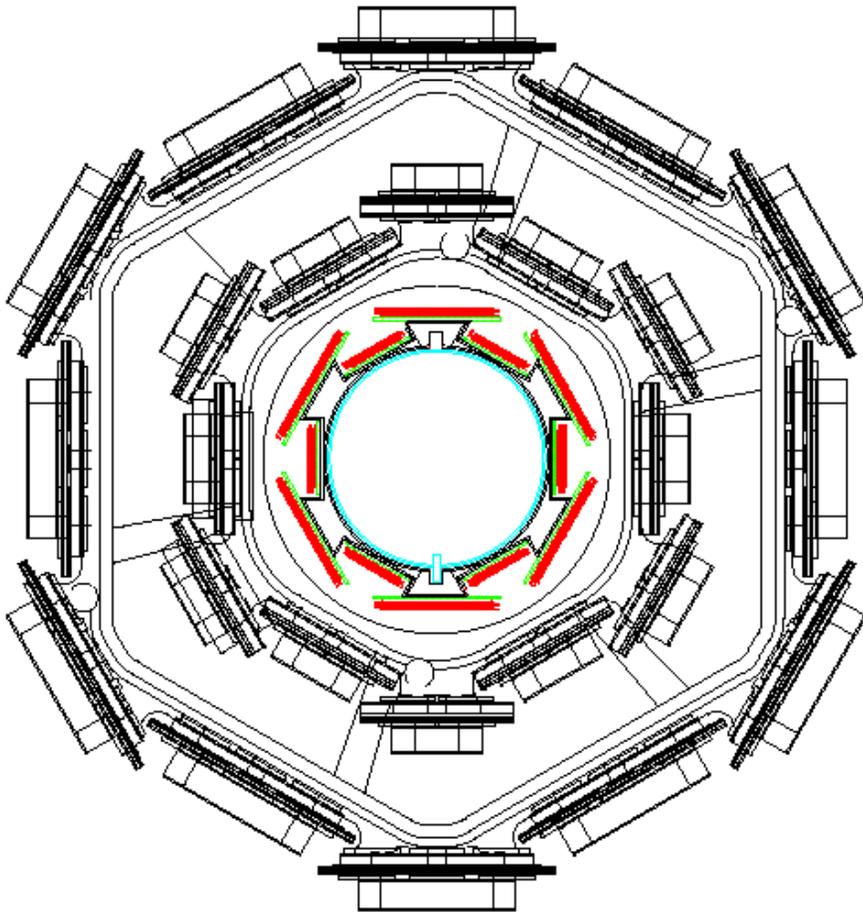
Goals and Features:

- Deal with new Tevatron parameters:
 - **132 nsec between bxngs**
 - **Much higher luminosity and radiation damage**
- Precise 3D track impact parameters
 - **B tagging: top, SUSY, Higgs**
 - **B Physics**
- Improved forward coverage
- Level II displaced-track trigger (SVT)

	SVX'	SVX II
Readout Coord.	r-φ	r-φ,z
# of Barrels	2	3
# of layers / barrel	4	5
# of wedges / barrel	12	12
Ladder length	25.5 cm	29.0 cm
Barrel length	51 cm	87 cm
Layer geometry	3° tilt	staggered radii
Radius inner layer	3.0 cm	2.44 cm
Radius outer layer	7.8 cm	10.6 cm
r-φ readout pitch	60,60,60,55 μm	60,62,60,60,65 μm
r-z readout pitch	absent	141;125.5;60;141;65 μm
Length readout channel (r-φ)	25.5 cm	14.5 cm
r-φ chips / ladder	2;3;4;6	4;6;10;12;14
r-z chips /ladder	absent	4;6;10;8;14
r-φ channels	46,080	211,968
r-z channels	absent	190,500
Total channels	46,080	405,504
Total chips	360	3168
Total detectors	288	720
Total Ladders	96	180



More inside and more outside!





Double sided silicon

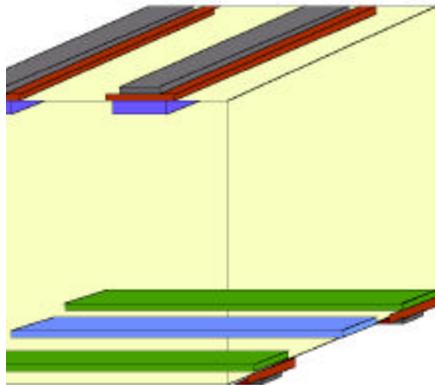
Both sides of the silicon wafers are segmented.

A combination of 90° and small stereo angle

Double metal layer necessary to readout the 90°

Capacitance Minimization

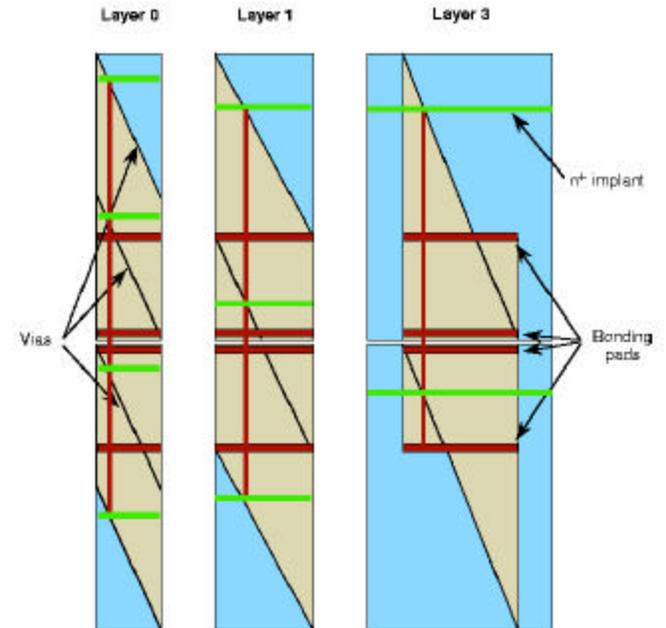
N-side 90 Deg. Stereo Sensors



Chip needs to be able to read both electrons and holes.

Number of channel per volume unit goes to the roof

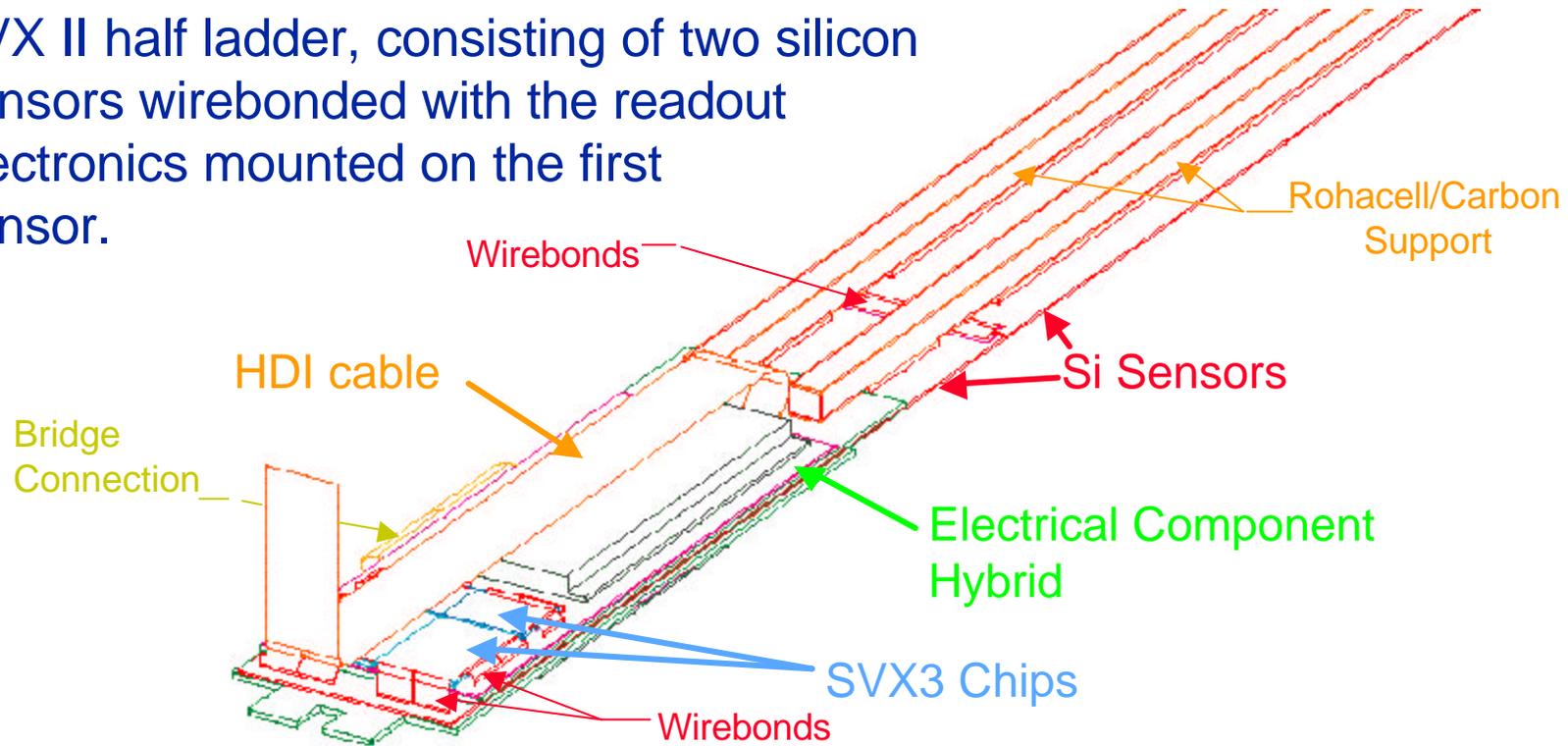
It allows 3D tracking





Very complicated modules

SVX II half ladder, consisting of two silicon sensors wirebonded with the readout electronics mounted on the first sensor.



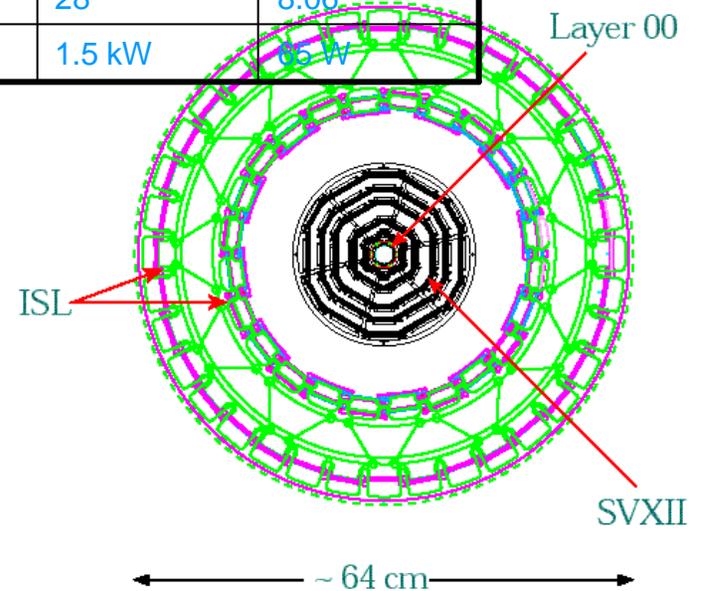
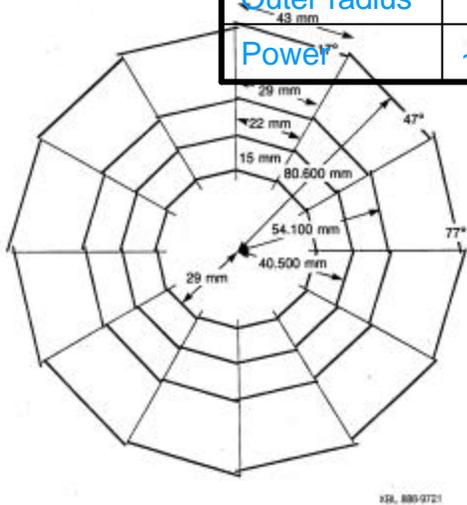
Gino Bolla, Purdue University

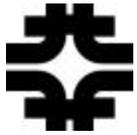
Evolution of Silicon Detector in CDF



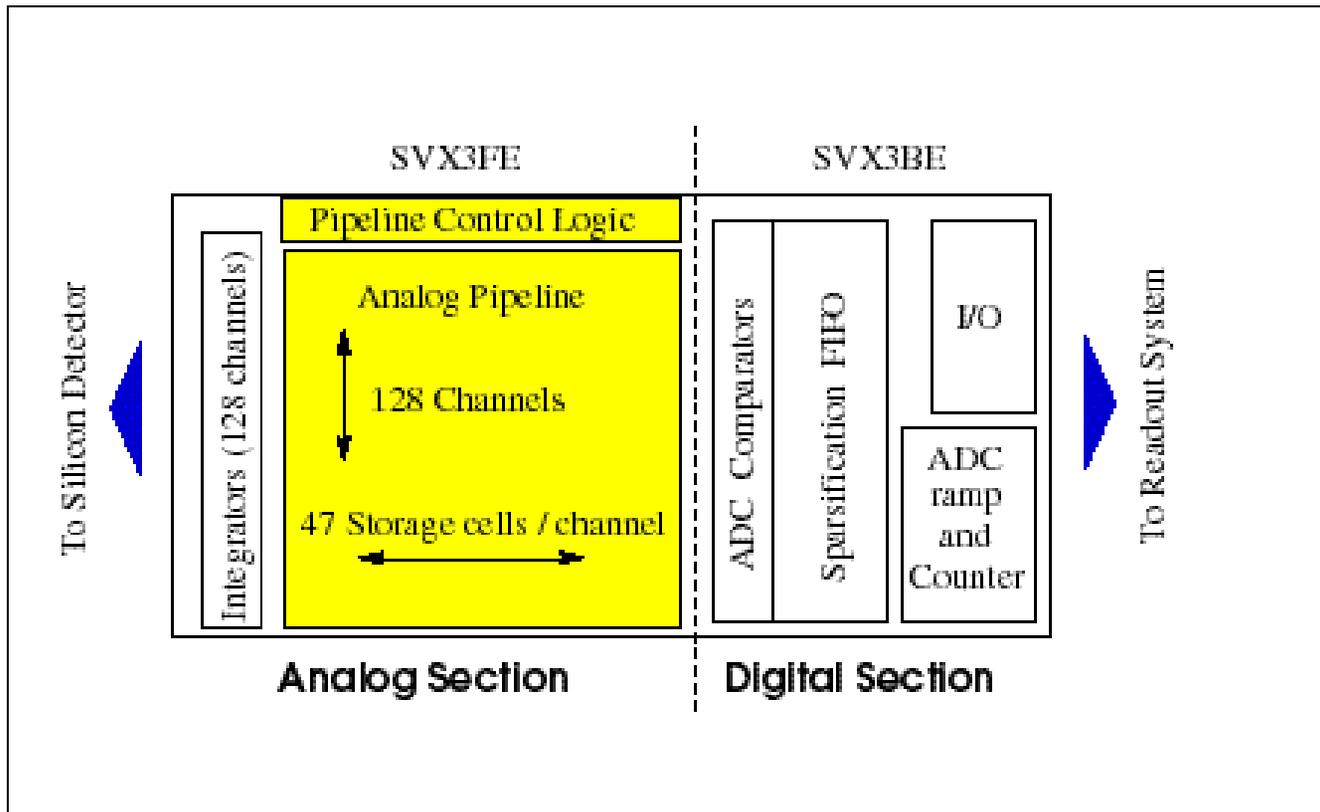
More inside and more outside!

	Layer 00	SVXII	ISL	Total Run 2b	SVX'
Layers	1	5	2	8	4
Length	0.9 m	0.9 m	1.9 m	1.9	0.6
Channels	13824	405504	303104	722432	48080
Modules	48 SS	360 DS	296 DS	704	96
Readout Length	14.8	14.5	21.5		30
Inner radius	1.35	2.5	20	1.35	2.86
Outer radius	1.65	10.6	28	28	8.06
Power	~100 W	1.4 kW	1.0 kW	1.5 kW	~60 W





A brand new readout chip



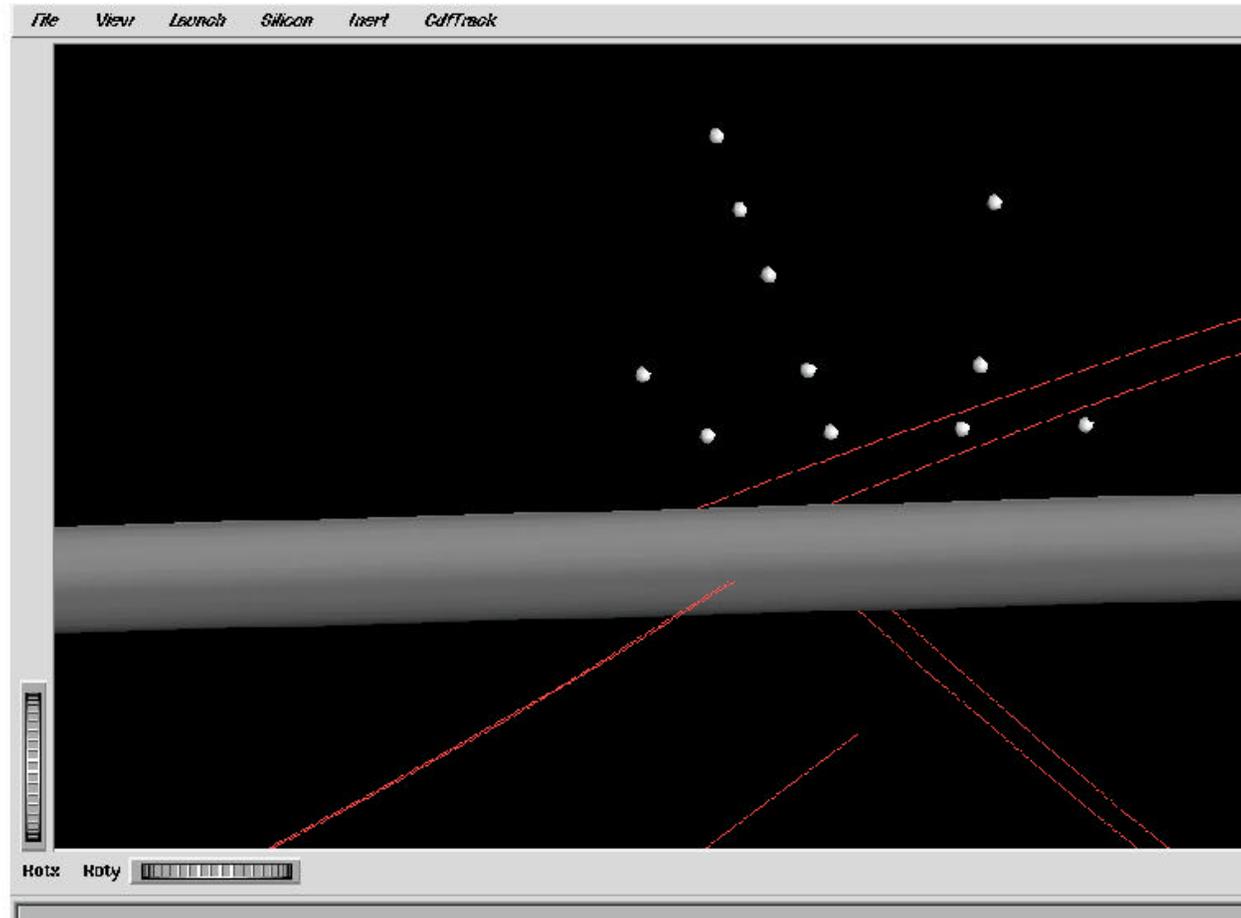
- Rad-hard 0.8 um Honeywell CMOS
- Tested to ~ 4 MRad
- Deadtimeless
- Dynamic pedestal subtraction
- Common to all Run II CDF silicon projects



Last week 1x8 collisions

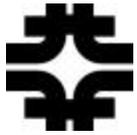
Graphic

Page 1 of 2



<http://www-h0.fnal.gov/8000/cgi-bin/det-system-align.pl?nb=silicon&action=view&npage=18&button=ves>

4/11/01



- Run 2b is going to be reality!
- Promised at least 15 fb^{-1} .
- SVXII was designed for 2 fb^{-1} but will probably last 5 (best estimate).
- Will have to be replaced with radiation harder device.

A simpler device would be desirable.

New SVX4 chip

Only single sided silicon (back to back)

Simple modules (hopefully hybrids outside of tracking volume L00 style).

Minimal number of subdesigns



Already a conceptual design ??????????

- It might look like a step back in technology but the scale of the project drives toward the minimum risk.
- The time scale to build it is very tight compared to the time spent to build SVXII.
- It will be one more challenge

