

The Silicon Vertex Trigger of CDF

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- **What is it ?**
- **How does it work ?**

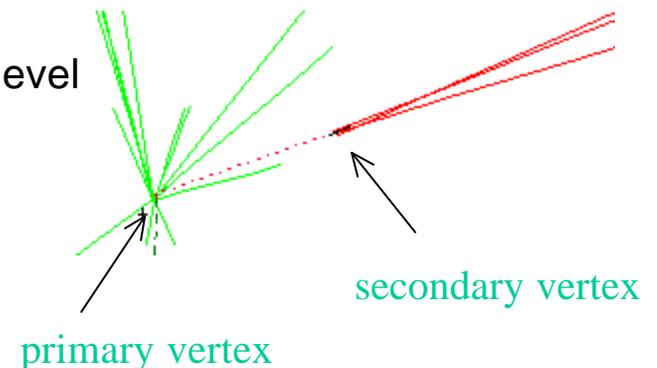
The Silicon Vertex Trigger was designed and built for the CDF collaboration by people from the following institutions:

- INFN – Pisa
- INFN – Trieste
- University of Chicago
- Université de Genève

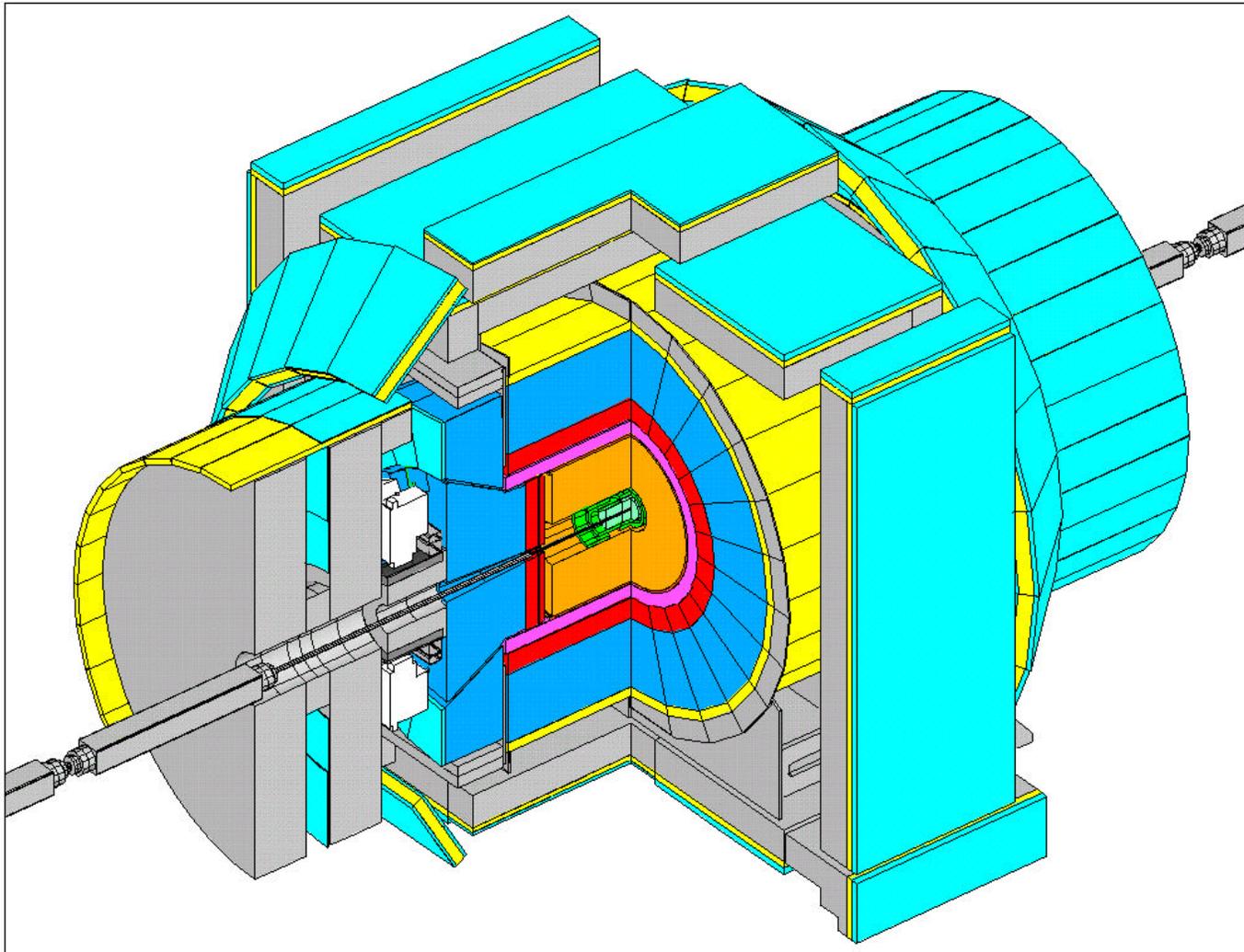
Physics Motivation

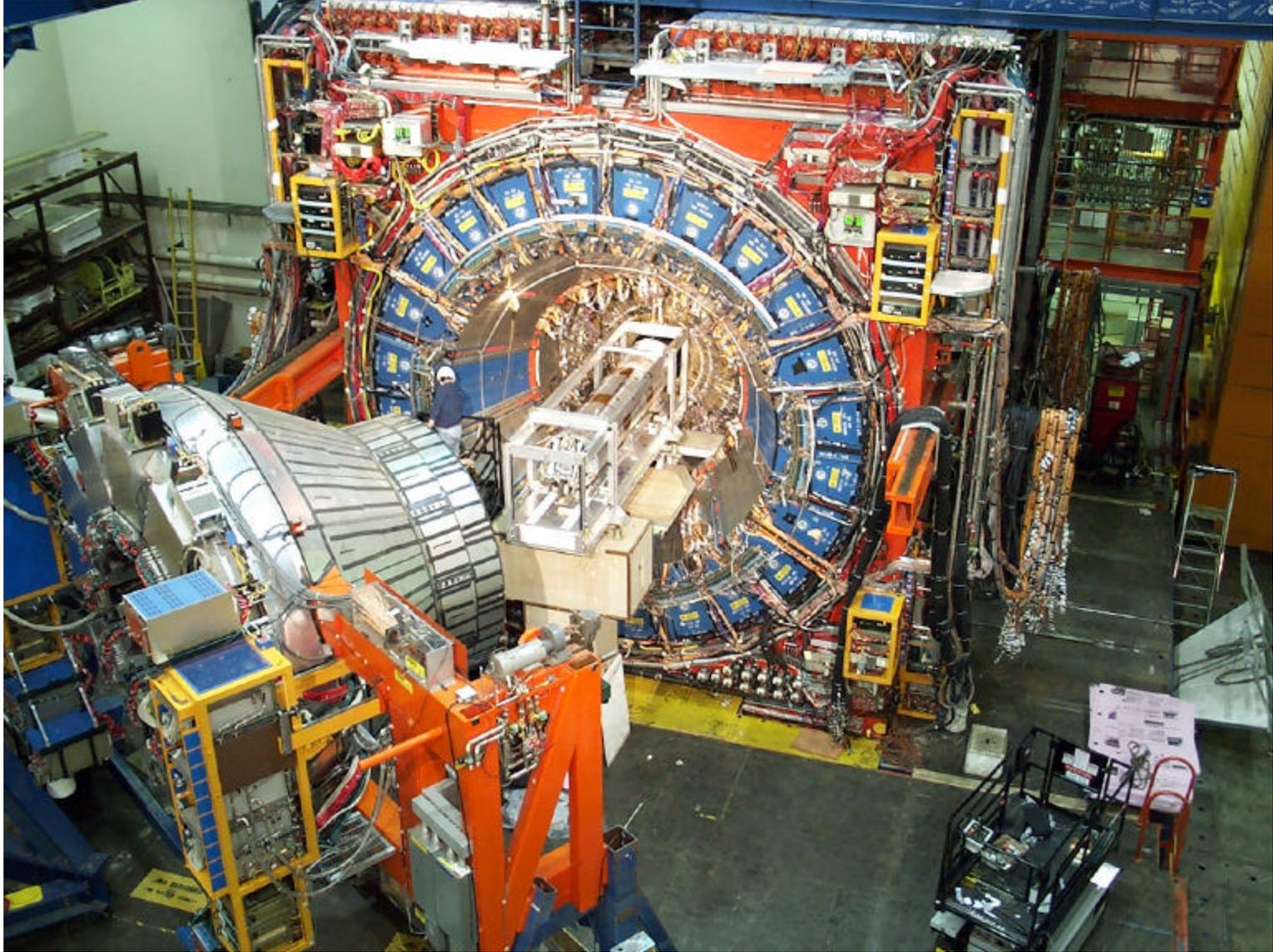
- With the great success of Silicon micro-strip detectors at high energy physics, its applications in triggering has been one of the major goals in instrumentation development
- An important application is to trigger on B hadrons inclusively, for
 - B physics studies, eg. CP violation in B decays, B_s mixing
 - new particle searches, eg. Higgs, Supersymmetry
- principle: detect large impact parameter tracks or secondary vertex from B hadron decays using the fact that $\tau(B) \approx 1.5$ ps
- A b-trigger is particularly important at hadron colliders
 - large B production cross section for B physics
 - high energy available to produce new particles decaying to b quarks
 - overwhelming QCD background
 - necessary to suppress background at trigger level

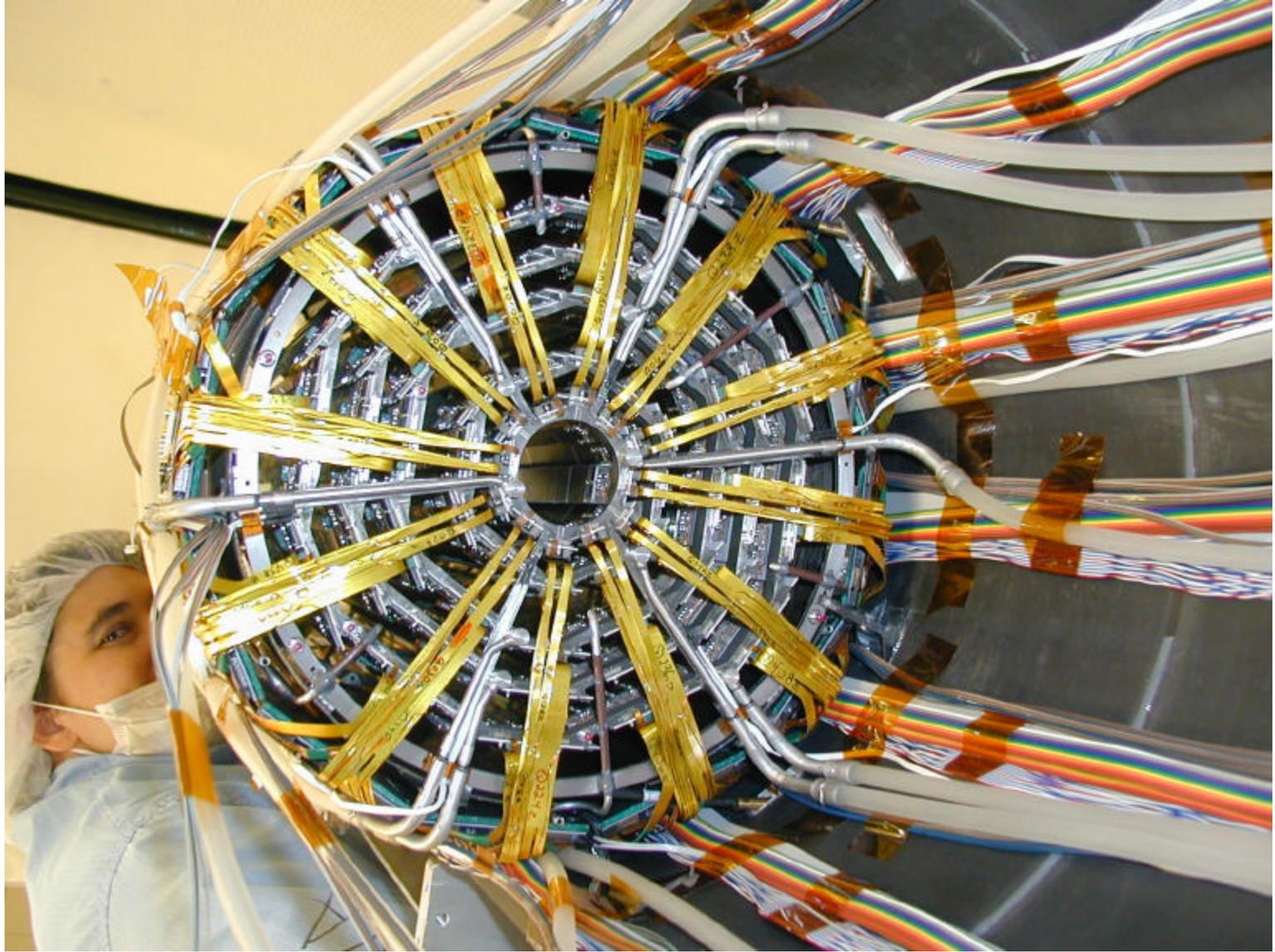
Big technical challenge!



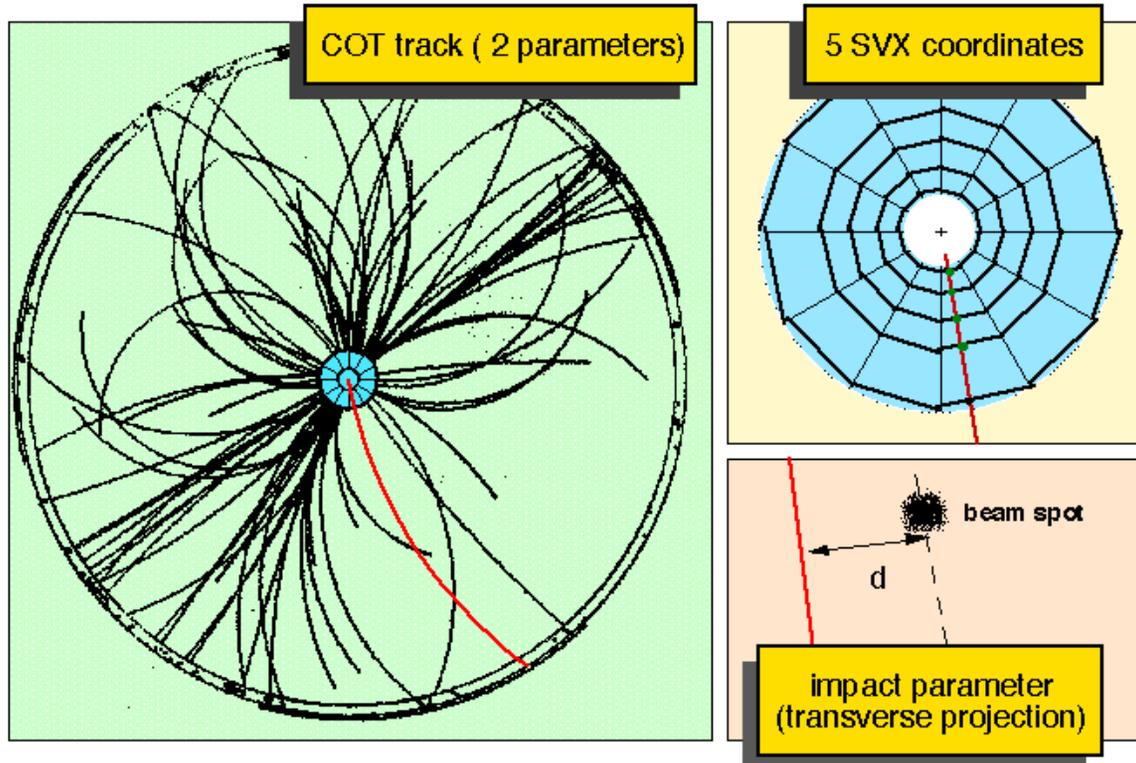
CDF DETECTOR







SVT: Silicon Vertex Trigger



Inputs:

- L1 tracks from XFT (f, p_T)
- digitized pulse heights from SVX II

Functionalities:

- hit cluster finding
- pattern recognition
- track fitting

Outputs:

- reconstructed tracks (d, f, p_T)

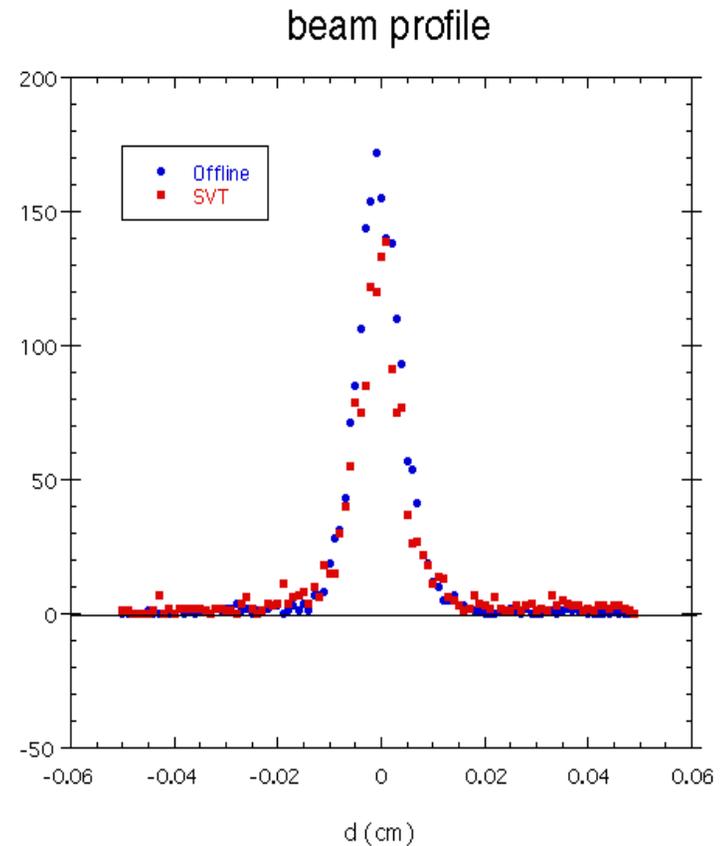
SVT performance

Tracking performance tested on CDF data using bit-level SVT simulation

$\sigma_d = 35 \mu\text{m}$ (at $p_T = 2 \text{ GeV}/c$)
 $\sigma_\phi = 1 \text{ mrad}$
 $\sigma_{p_T} = 0.003 p_T$ (p_T in GeV/c)
 $\varepsilon \sim 97 \%$ (for 4 hits tracks)

almost offline quality!

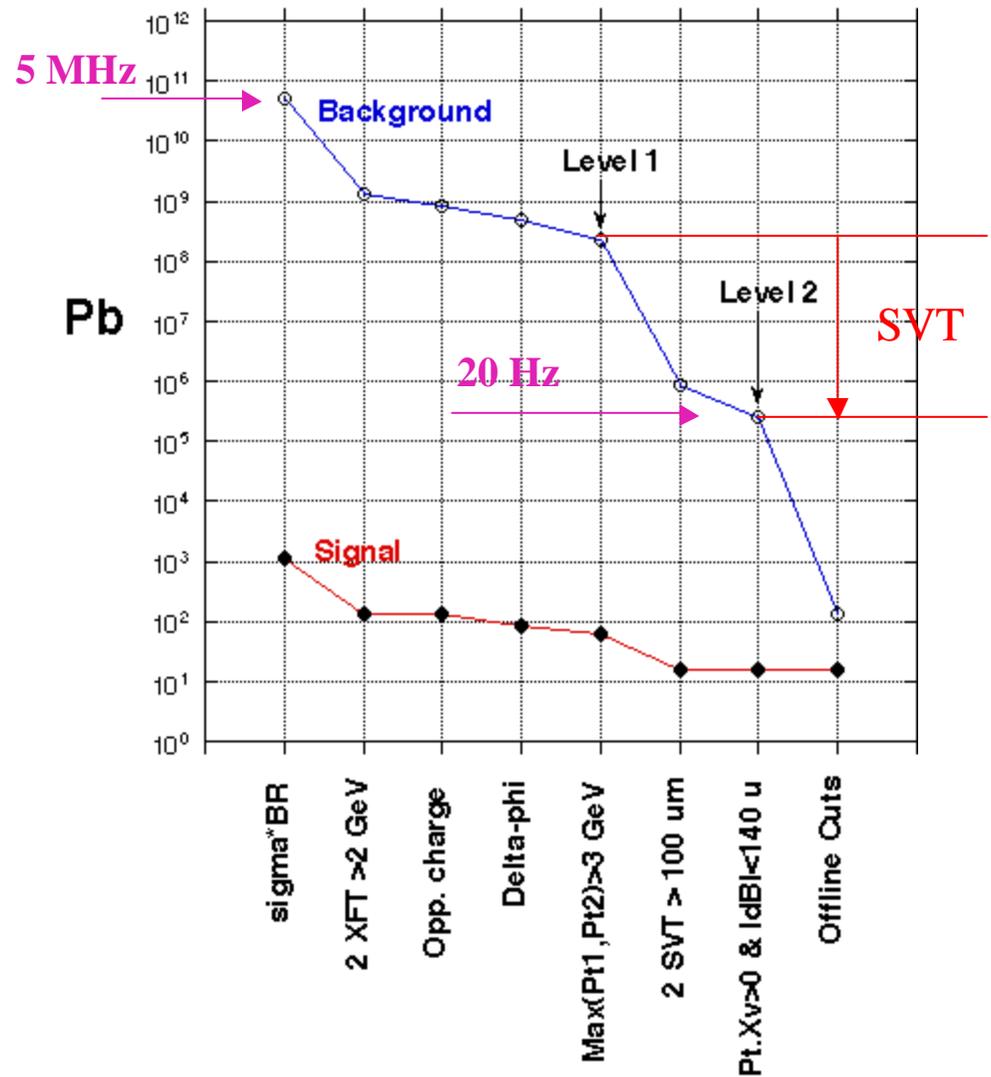
Execution time $\sim 10 \mu\text{s}$ / event



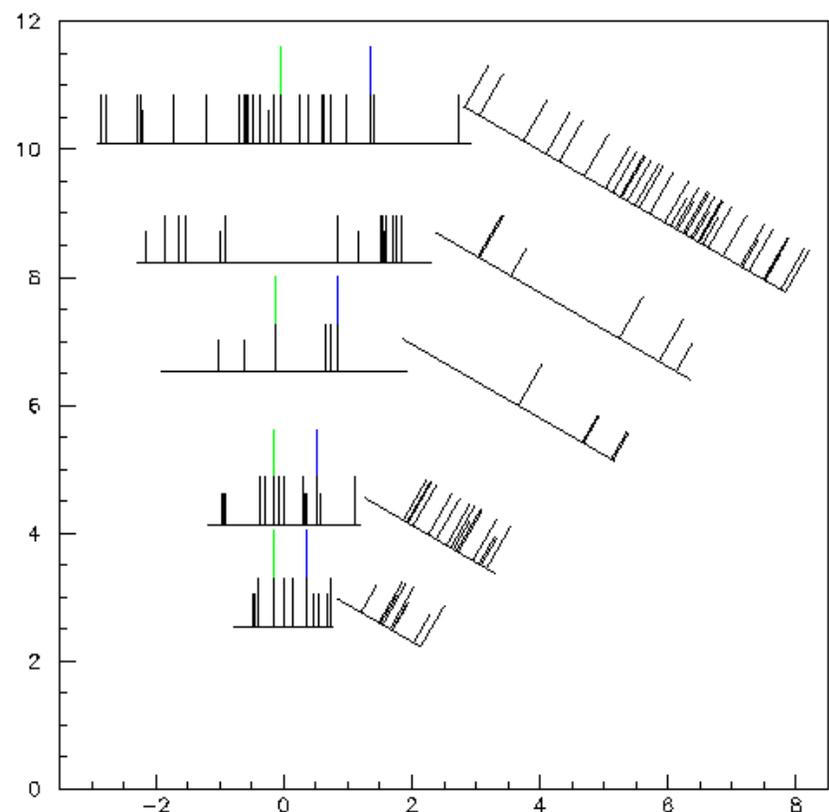
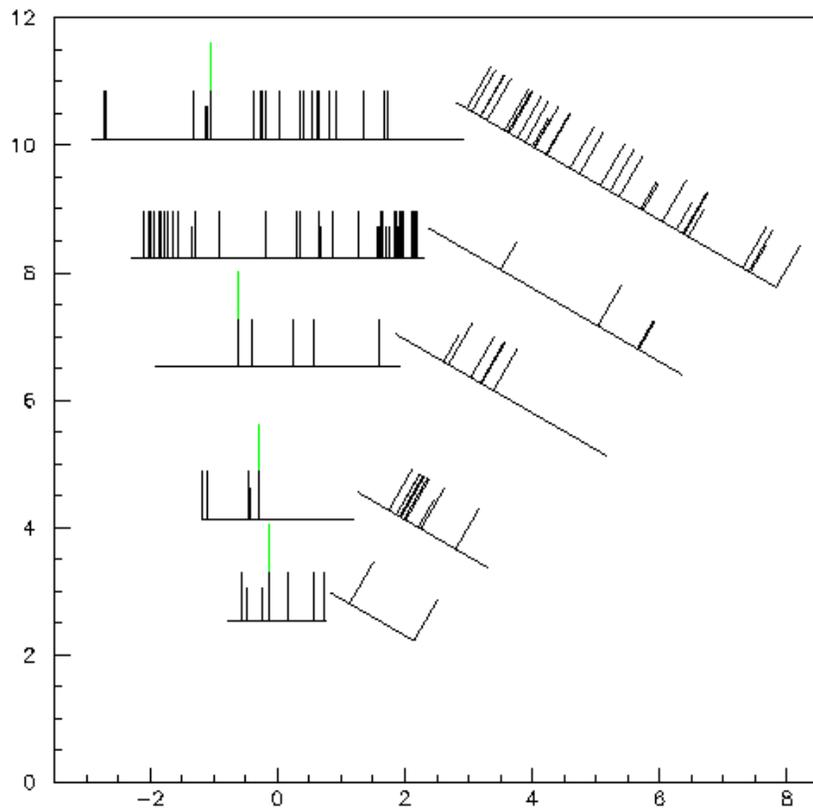
SVT for $B^0 \rightarrow \pi^+ \pi^-$

$B^0 \rightarrow \pi^+ \pi^-$ Trigger

- SVT reduces the background rate by a factor of 1000
 - data recording possible by DAQ
- CDF II (2 fb^{-1} , 2001-2003)
 - $\Delta(\sin 2\beta) \approx 0.08$
($\sim 10,000 B^0 \rightarrow J/\Psi K_S^0$)
 - $\Delta(\sin 2\alpha) \approx 0.1$
($\sim 10,000 B^0 \rightarrow \pi^+ \pi^-$)
 - B_s^0 mixing up to $X_s \sim 60$
($\sim 10,000 B_s^0 \rightarrow D_s \pi$)



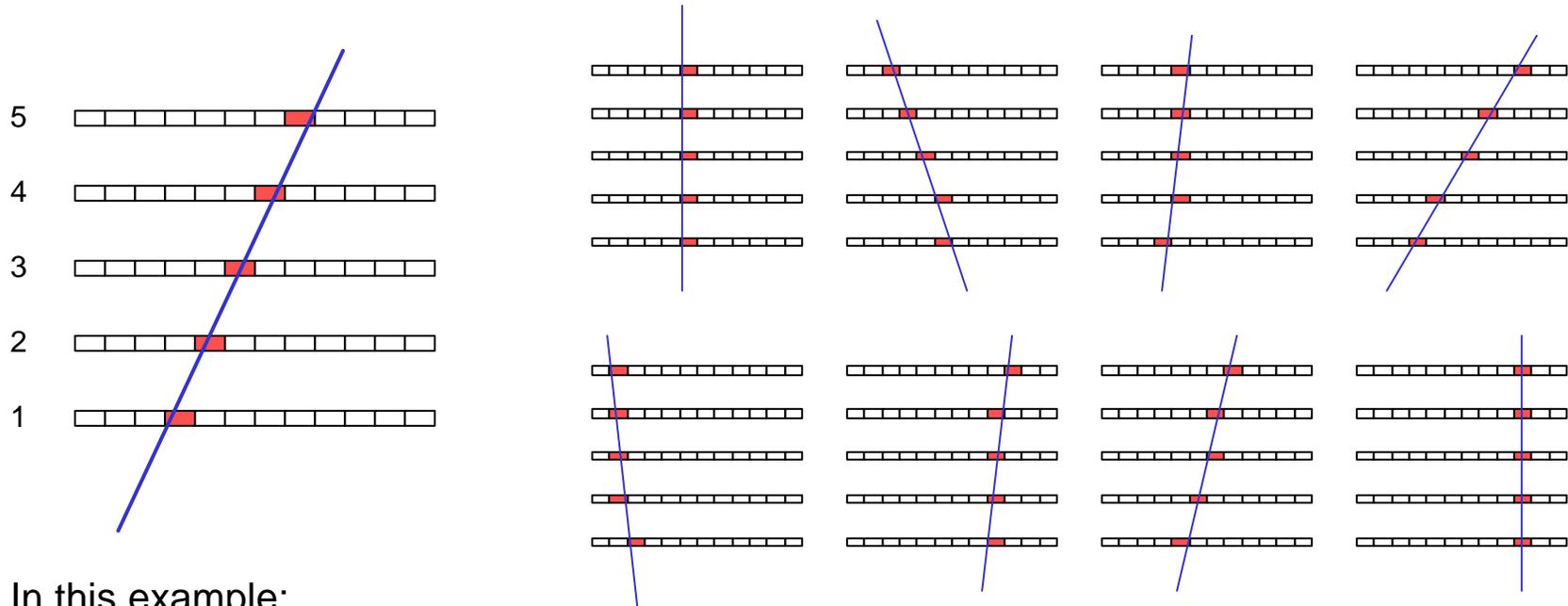
FINDING TRACKS IN THE SILICON



Building the “Pattern Bank”

Instead of looking for hit combinations such that $f(x_1, x_2, x_3, \dots) = 0$

1. Build a database with all patterns corresponding to “good” tracks
2. Compare hits in each event with all patterns to find track candidates



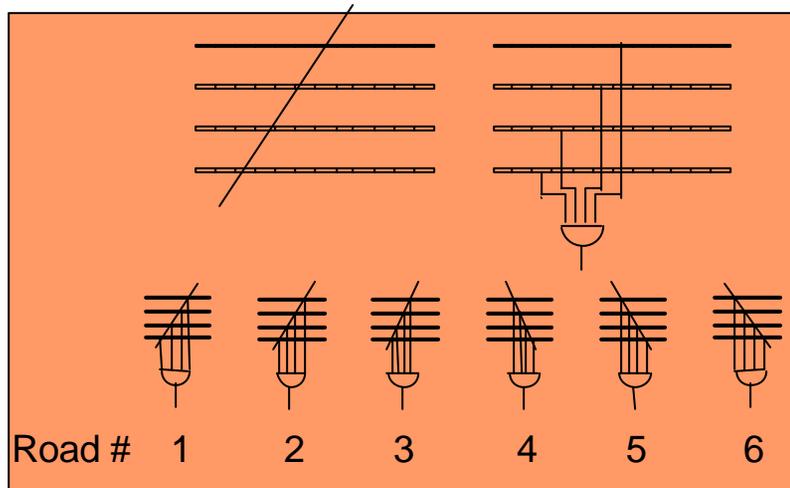
In this example:

Straight lines, 5 layers, 12 bins/layer

⇒ Total number of patterns $\sim (12)^2 \cdot (5-1) = 576$

Associative Memory working principle

A set of patterns is stored in the Associative Memory. Each pattern (ROAD) contains the coordinates of hit at each detector layer of a possible track.

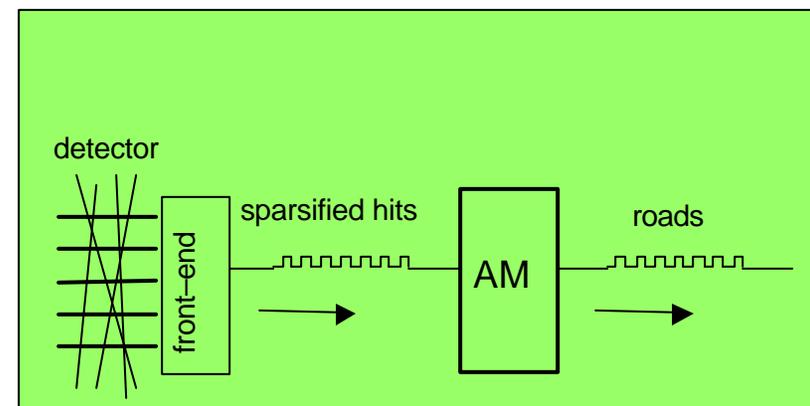


Pattern recognition is complete as soon as the last hit is read.

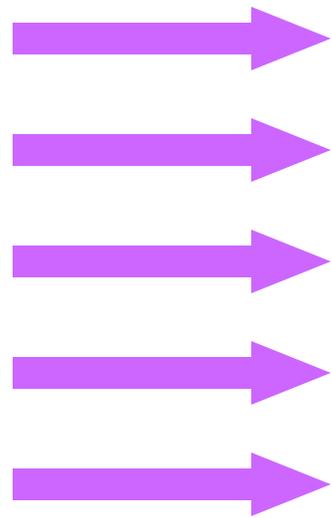
Roads found by the AM are output sequentially.

Hit coordinates are read into the AM sequentially.

Each coordinate is compared with all the patterns in parallel.

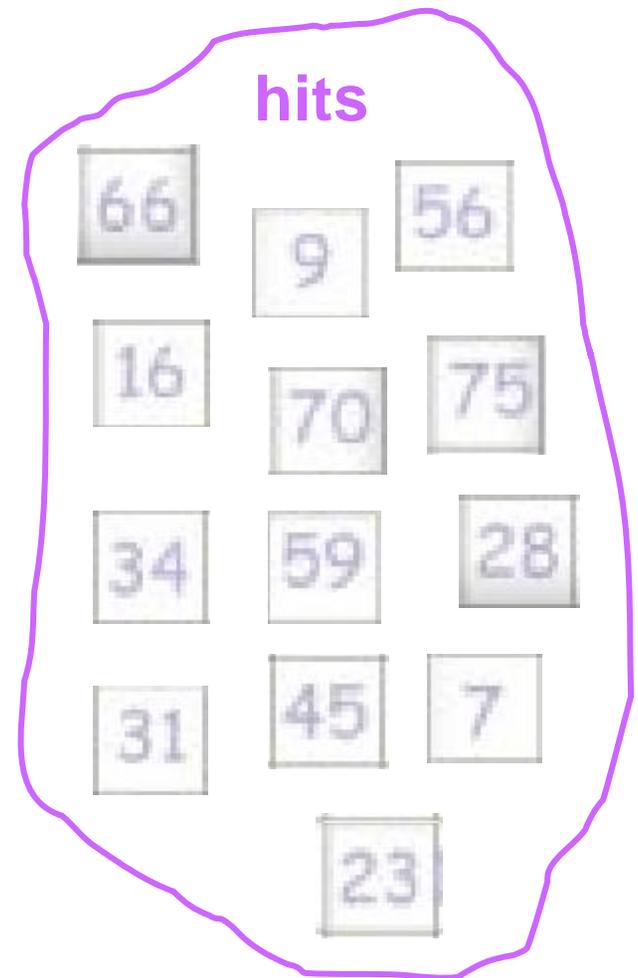


Let's play Bingo!

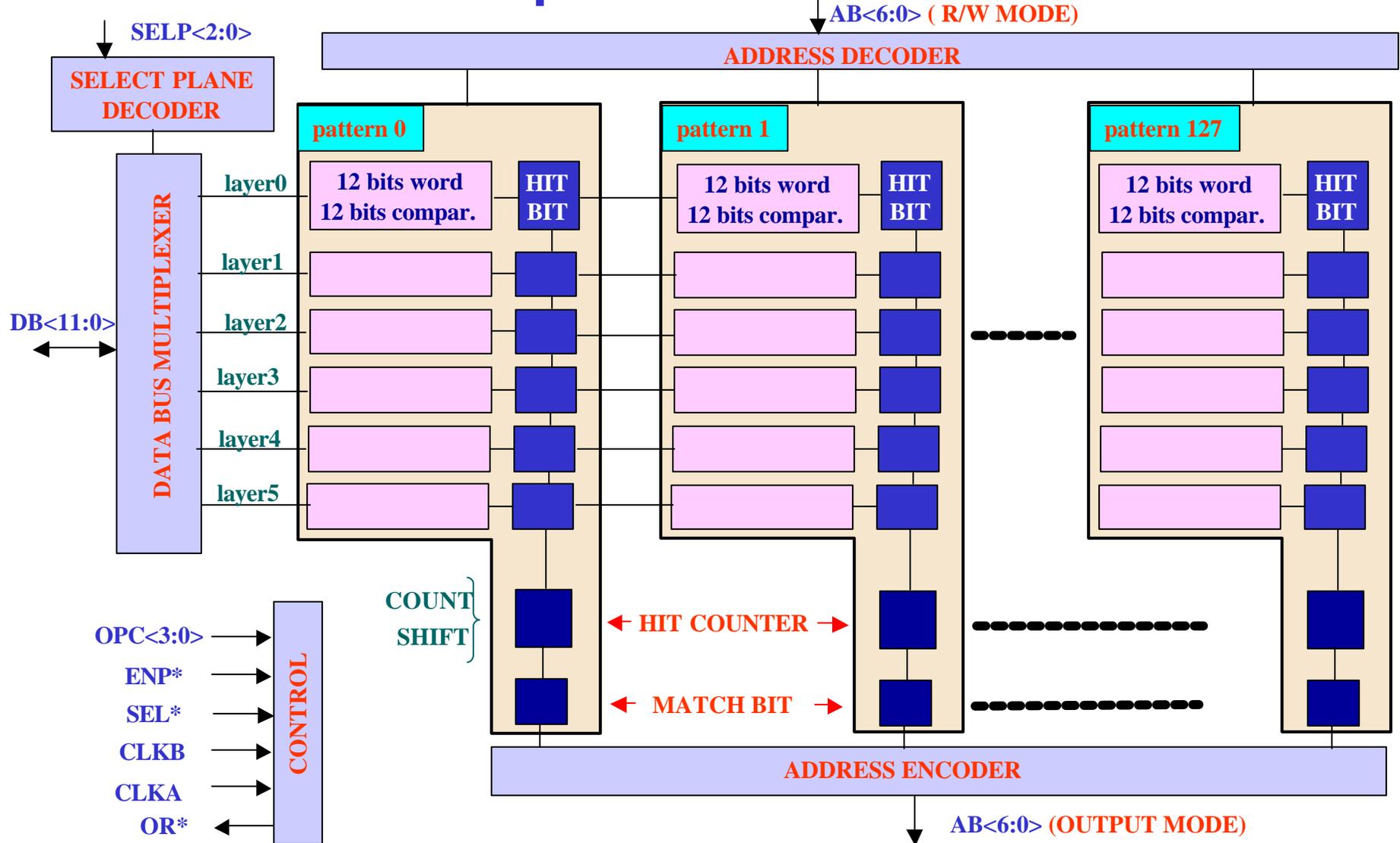


B I N G O				
9	22	31	59	65
7	16	45	56	70
1	23	FREE	48	75
13	17	34	47	69
15	28	43	53	66

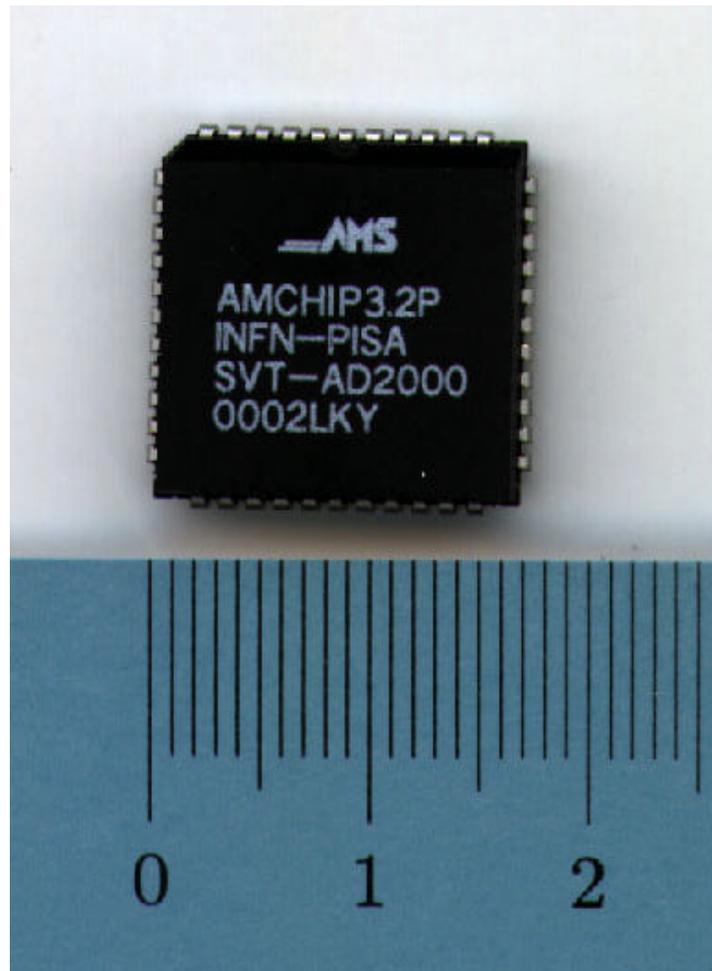
one row of numbers = one pattern



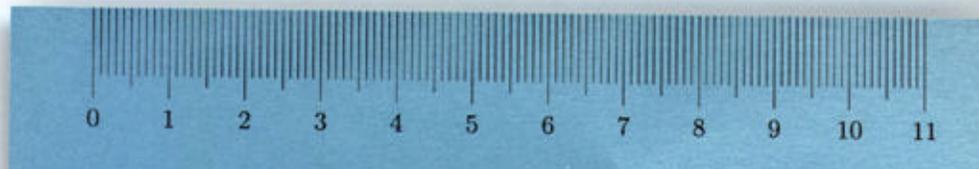
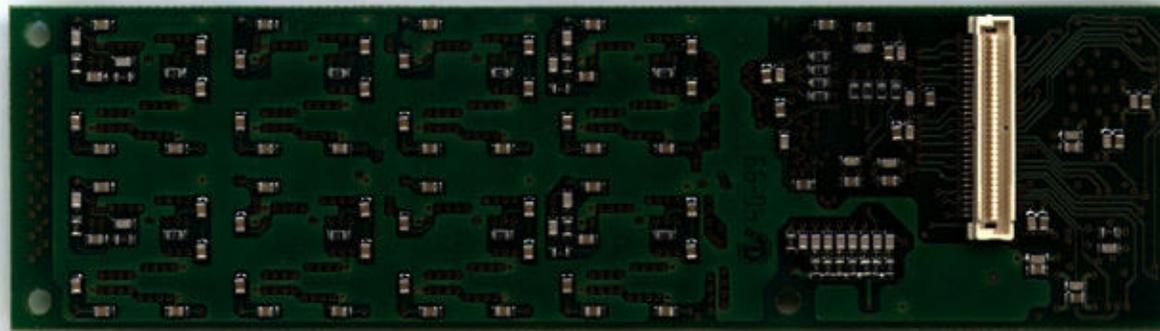
AM chip internal structure



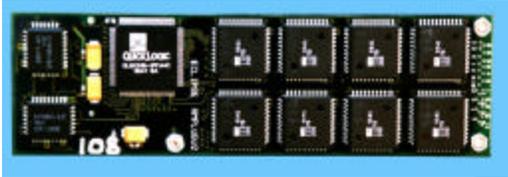
AMchip



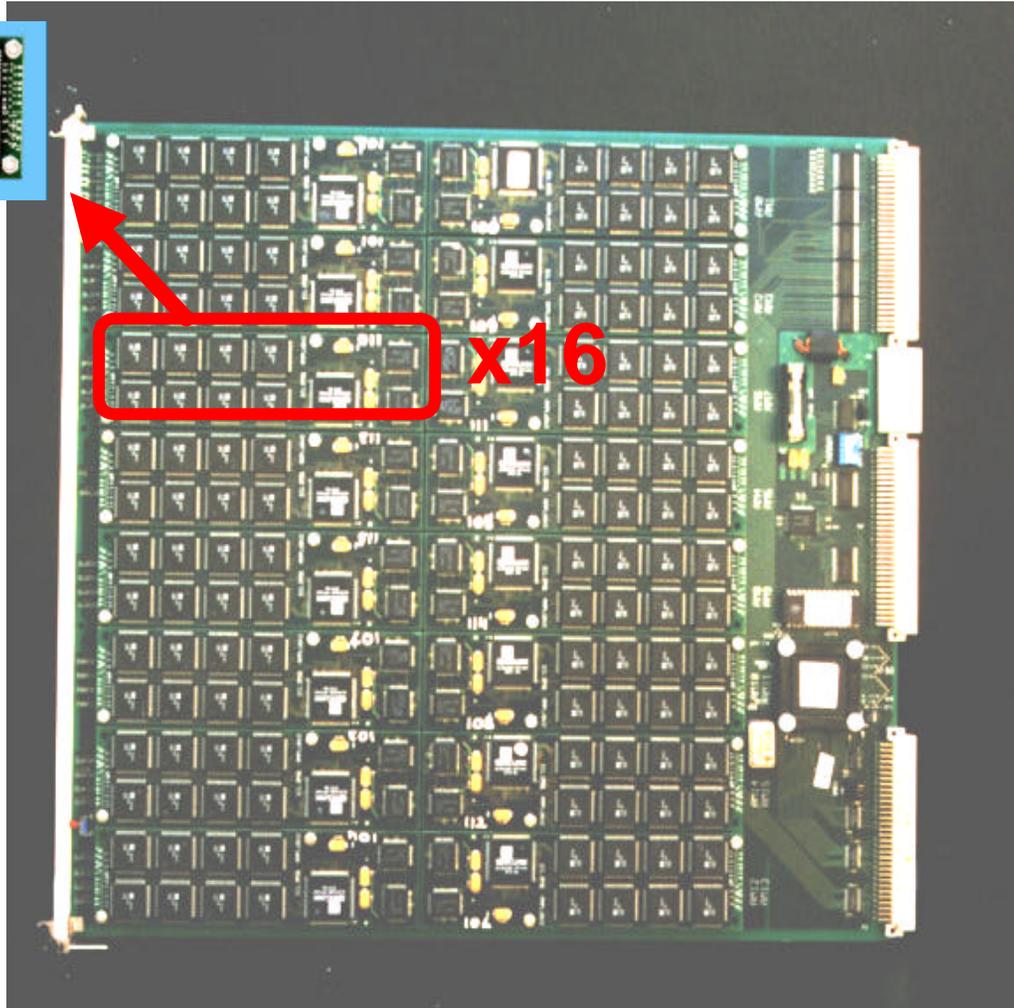
Amplug: mezzanine board



AM Board



**128 Amchips
x 128 patterns
each
= 16K pattern
board**



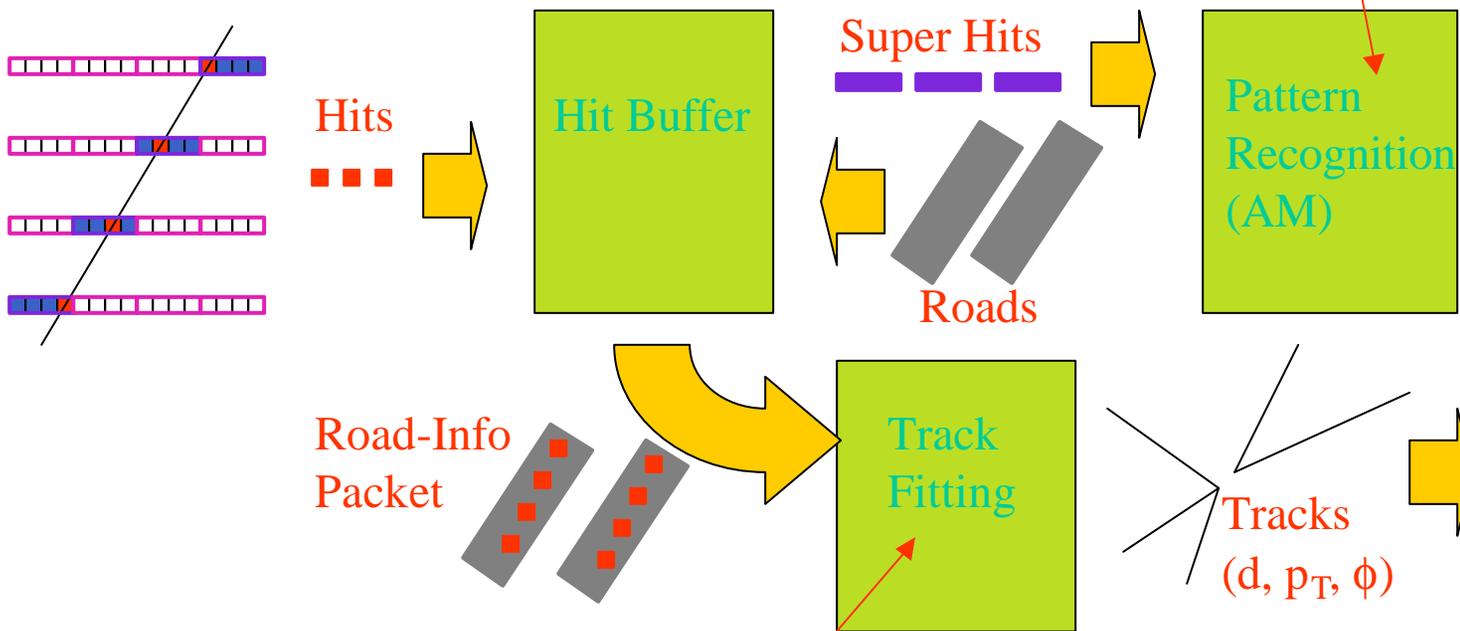
VME
↔

AMbus
↔

SVT basic architecture

- Pattern recognition and track fitting done separately and pipelined

Pattern recognition with Associative Memory (AM)
highly parallel algorithm
using coarser resolution to reduce memory size

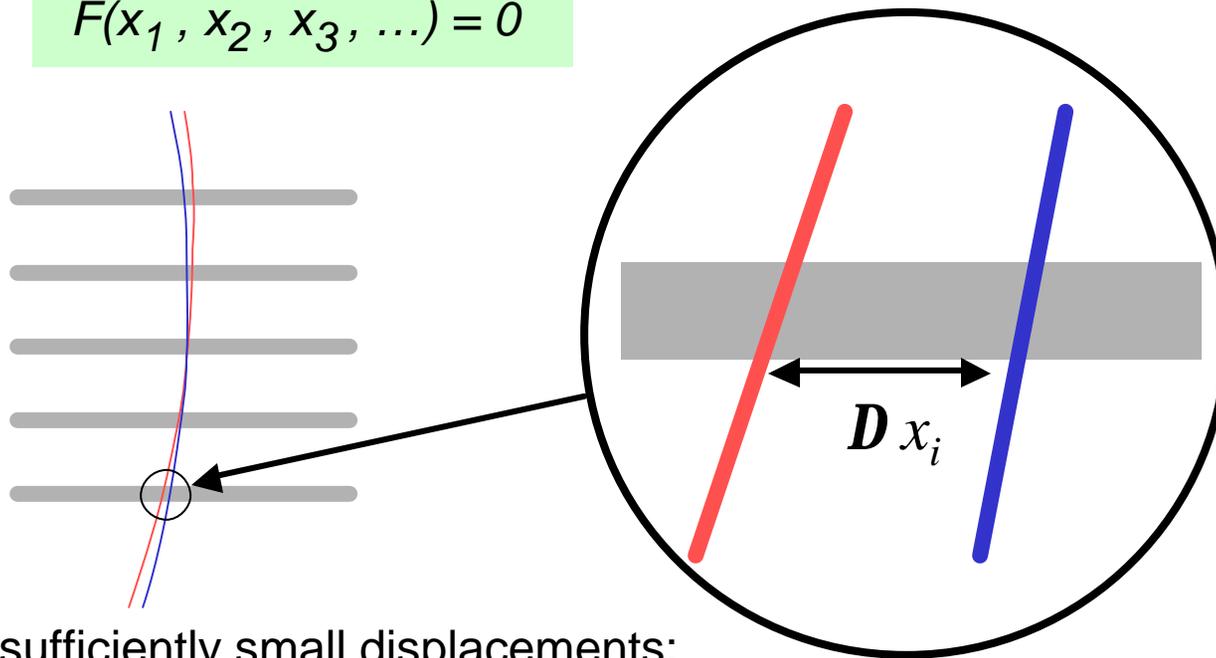


Fast track fitting with linear approximation
using full resolution of the silicon vertex detector

From non-linear to linear constraints

Non-linear geometrical constraint for a circle:

$$F(x_1, x_2, x_3, \dots) = 0$$



But for sufficiently small displacements:

$$F(x_1, x_2, x_3, \dots) \sim a_0 + a_1 \mathbf{D}x_1 + a_2 \mathbf{D}x_2 + a_3 \mathbf{D}x_3 + \dots = 0$$

with constant a_i

(first order expansion of F)

6 coordinates: $x_1, x_2, x_3, x_4, x_5 (P_T), x_6 (\phi)$

3 parameters to fit: P_T, ϕ, d

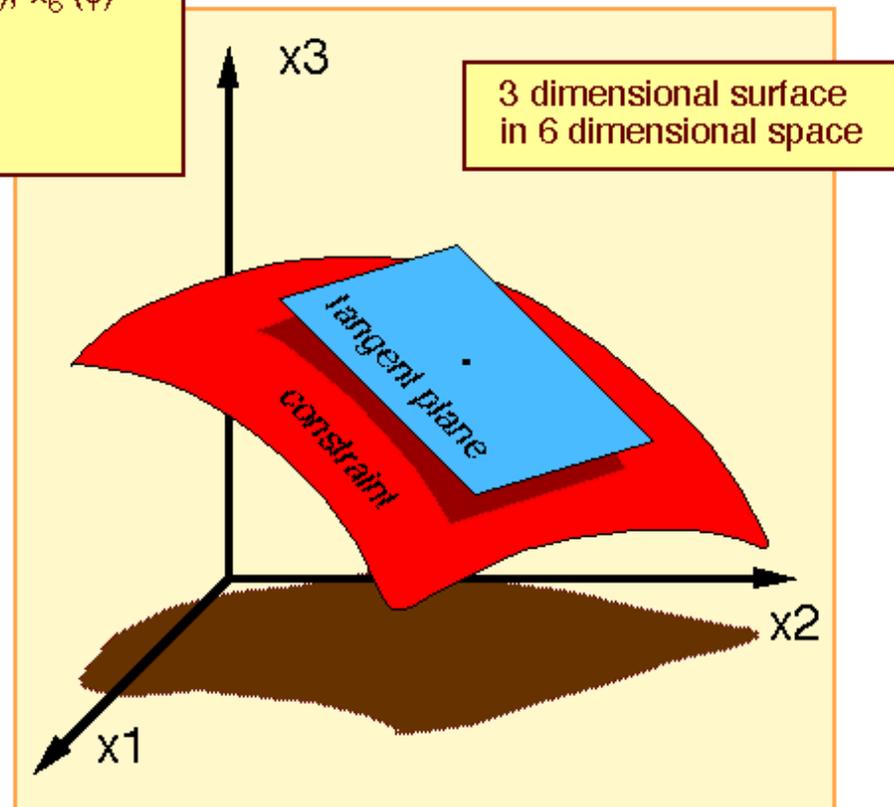
3 constraints

tangent plane:

$$\sum_1^6 a_i x_i = b$$

track parameters:

$$d \approx c_0 + \sum_1^6 c_i x_i$$



Linear approximation is so good that a single set of constants is sufficient for a whole detector wedge (30° in ϕ)

Constraints vs ChiSquare

Constraints:

$$F_k(x_1, x_2, x_3, \dots) = 0$$

$$K = 1 \dots N$$

$$N = (\text{number of points}) - (\text{number of parameters})$$

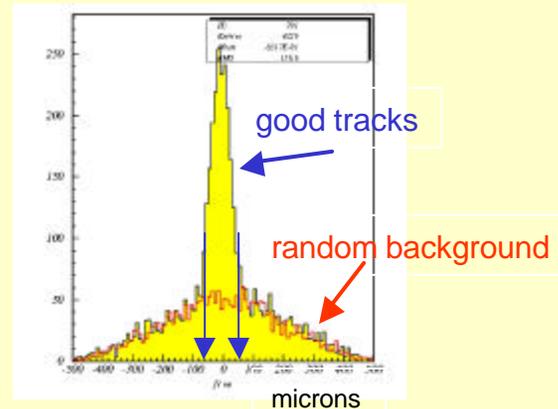
= "number of degrees of freedom of fit"

$$\chi^2 = \sum F_k^2$$

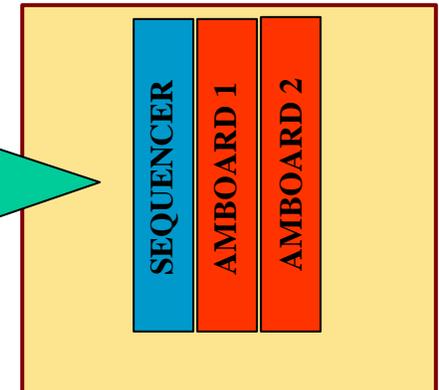
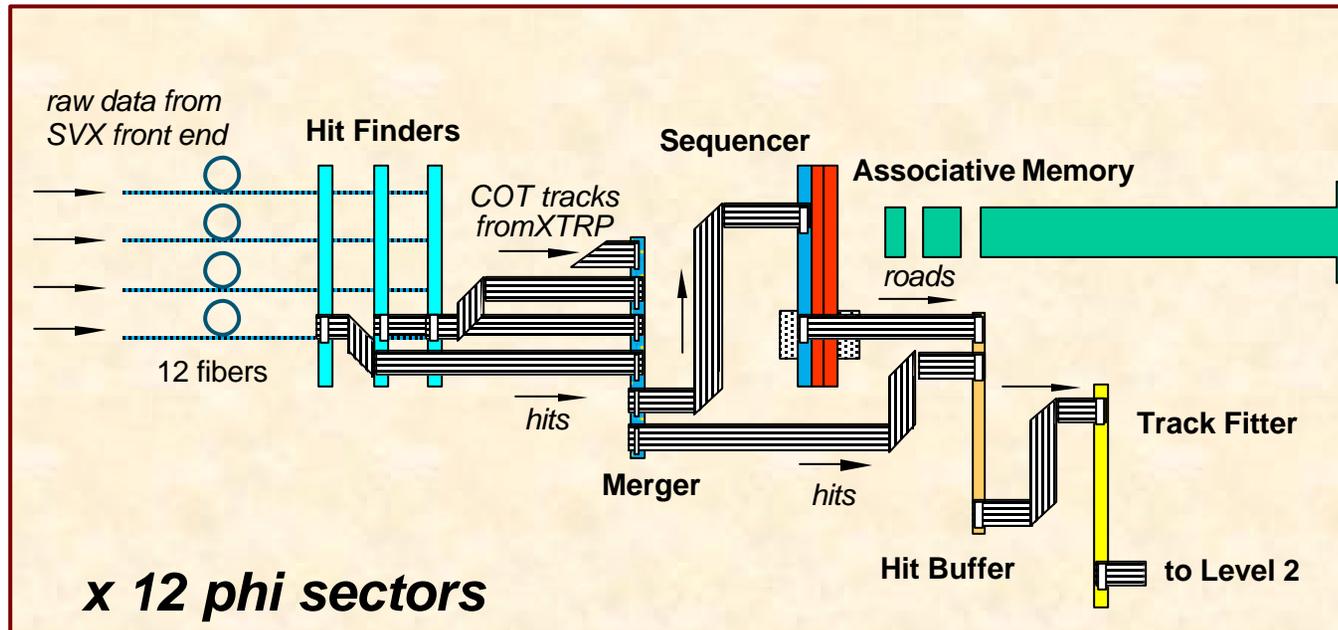
provided the F_k are normalized correctly

Why use F_k instead of χ^2 ???

Since F_k are linear functions of coordinates (at least to first order) a small detector misalignment will just cause a *shift* of the peak with no appreciable increase of the *width*.



SVT system architecture



**Pattern recognition:
1 AMS + 2 AMBOARD
for each 30° phi sector**

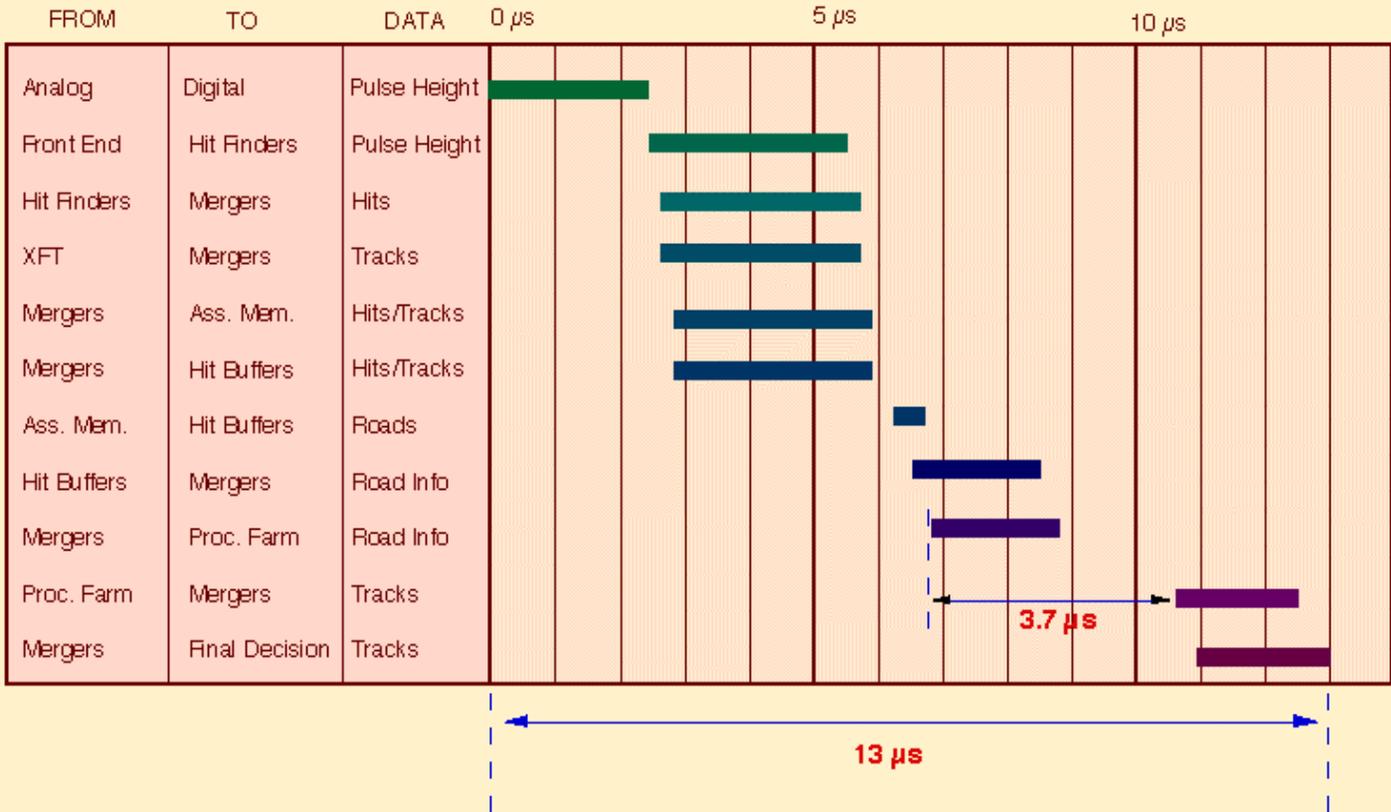
- Hit Finder:** finding silicon hit clusters
- Merger:** merging data at various stages
- AM Sequencer:** managing AM operation, gateway to AM chips
- AM Board:** housing AM chips for road finding
- Hit Buffer:** associating hits to roads found by AM
- Track fitter:** fitting full resolution tracks
- Spy Control:** managing spy buffers and error handling

All 9U VME boards

All data driven
(except AMS + AMB)

All with spy buffers
(except AMB)

SVT TIMING

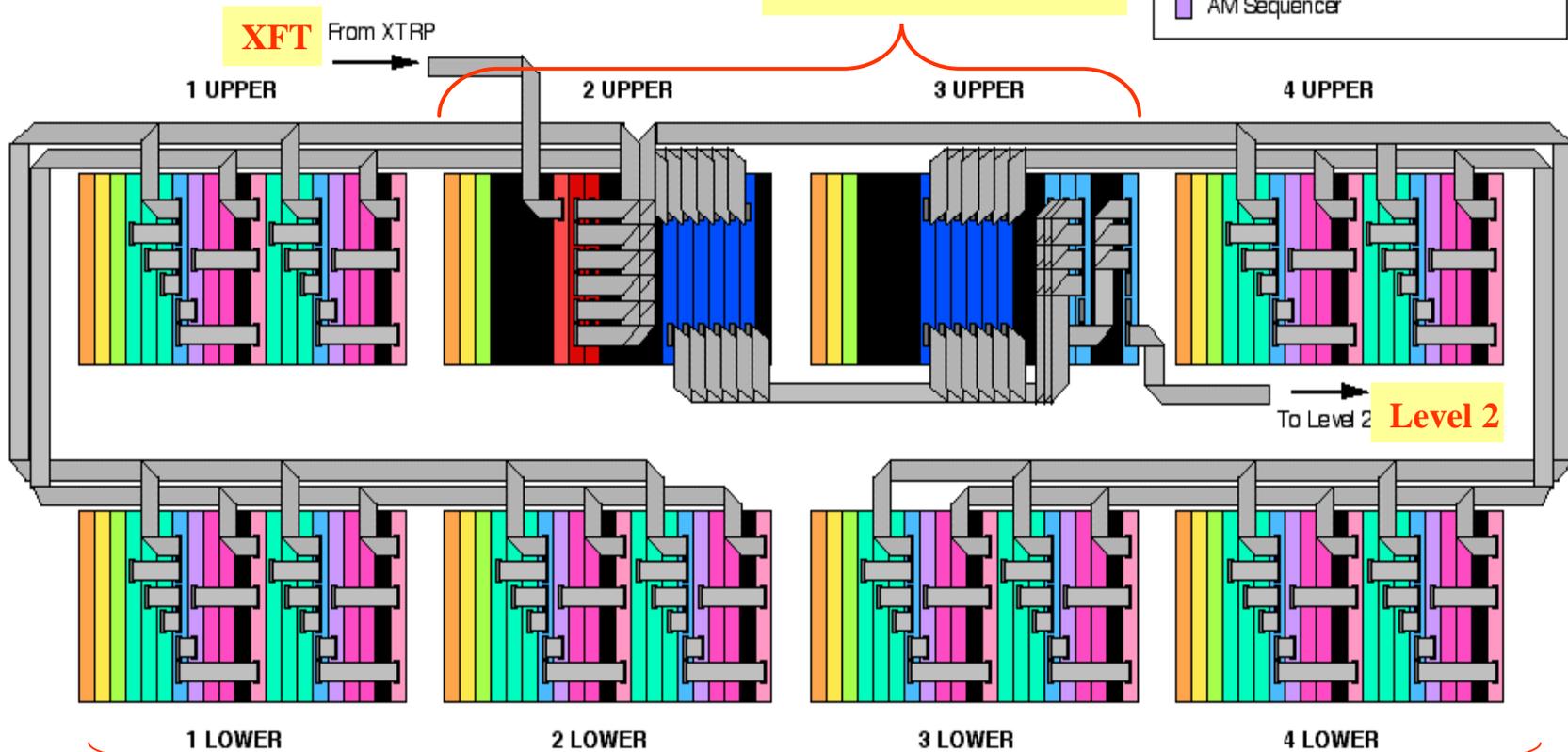


SVT Crate Layout

SVT BASELINE
BOARD AND CRATE LAYOUT

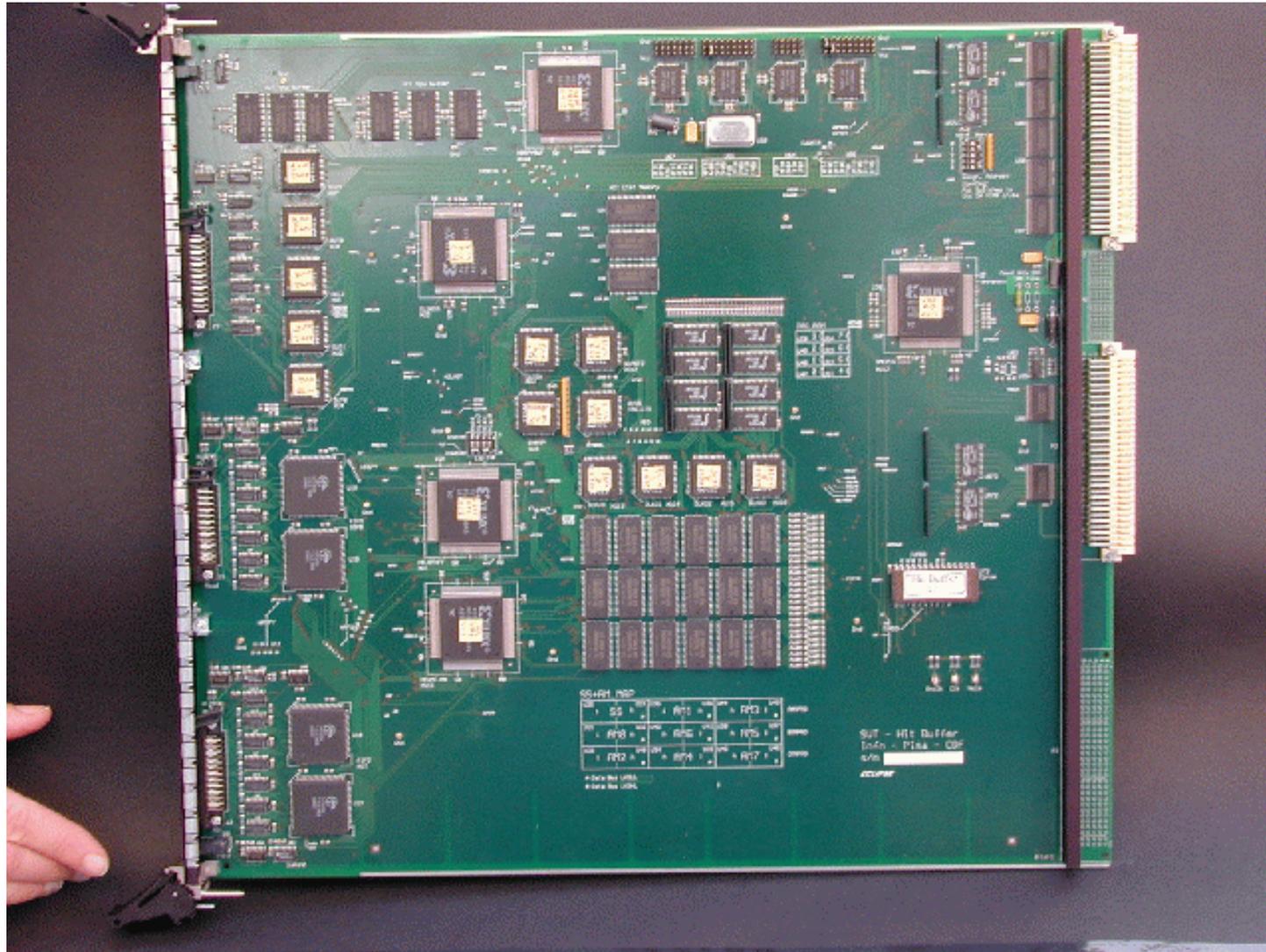
2 Fitter and
Fanout crates

CPU	AM Board
Tracer	Hit Buffer
Spy Control	Track Fitter
Hit Finder	XFT A
Merger	XFT B
AM Sequencer	

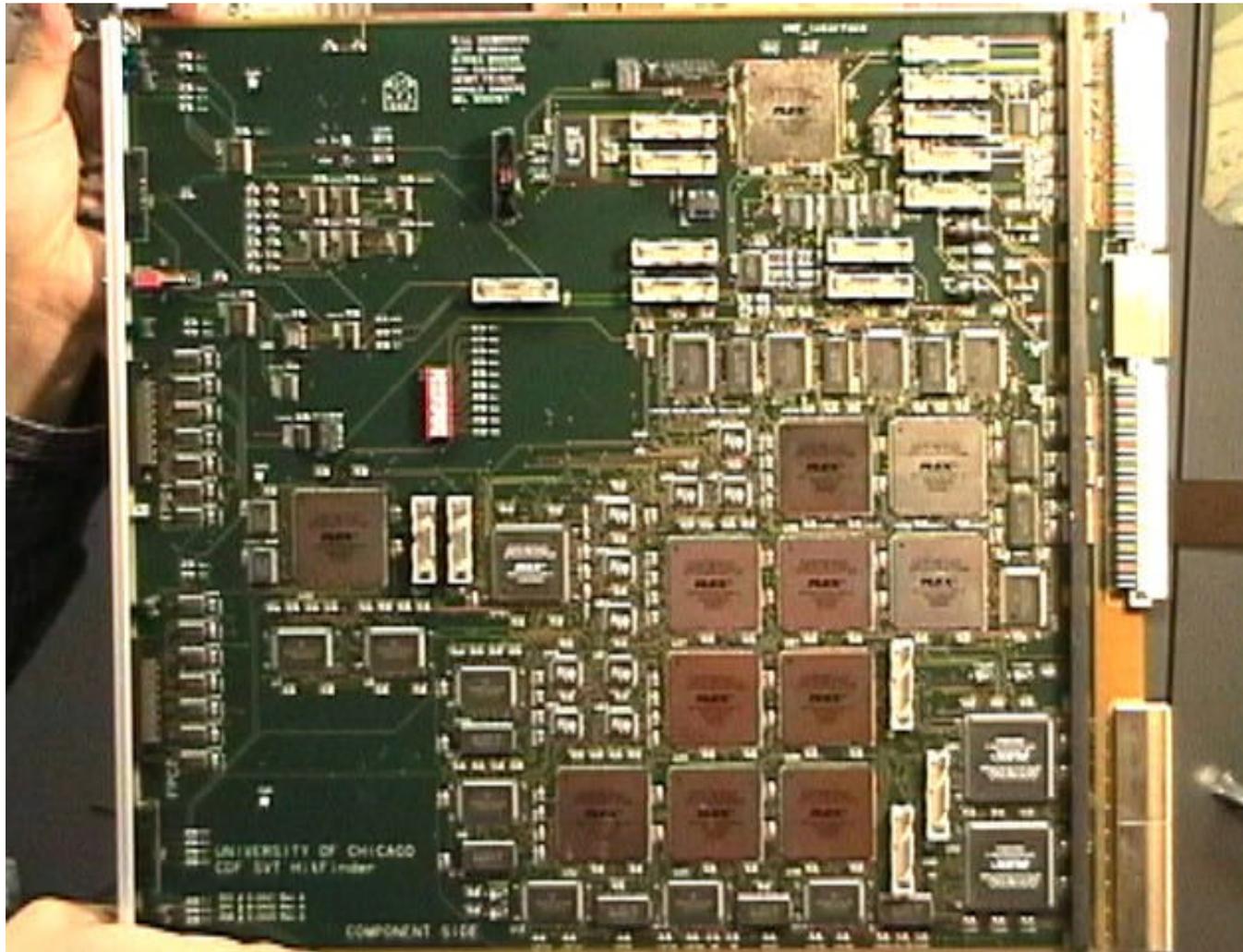


6 main crates

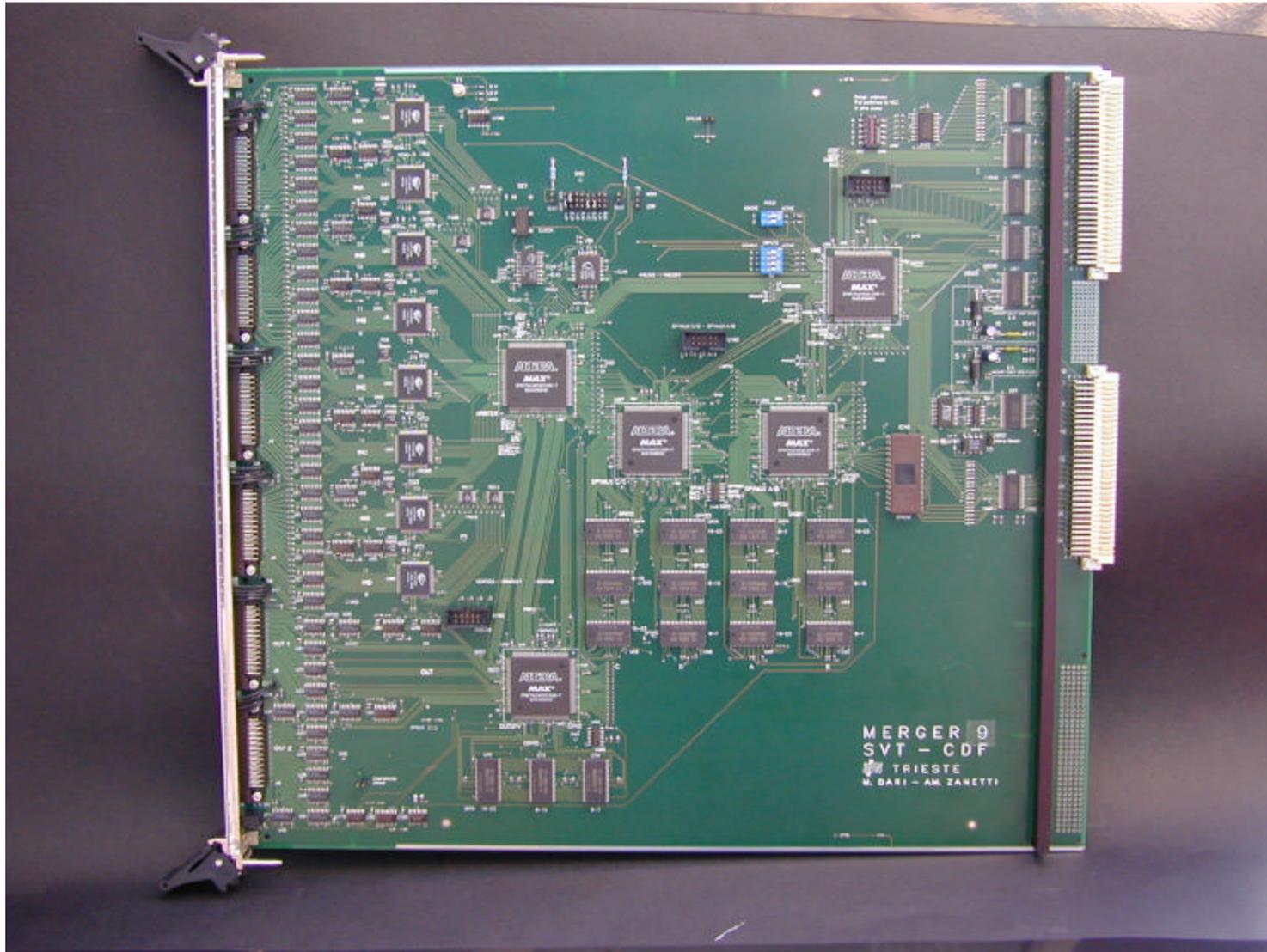
HIT BUFFER BOARD



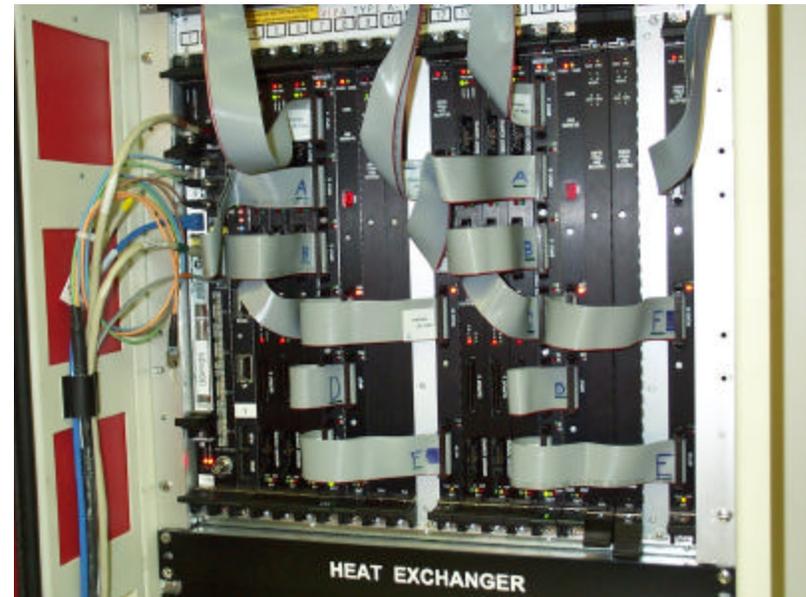
HIT FINDER BOARD



MERGER BOARD

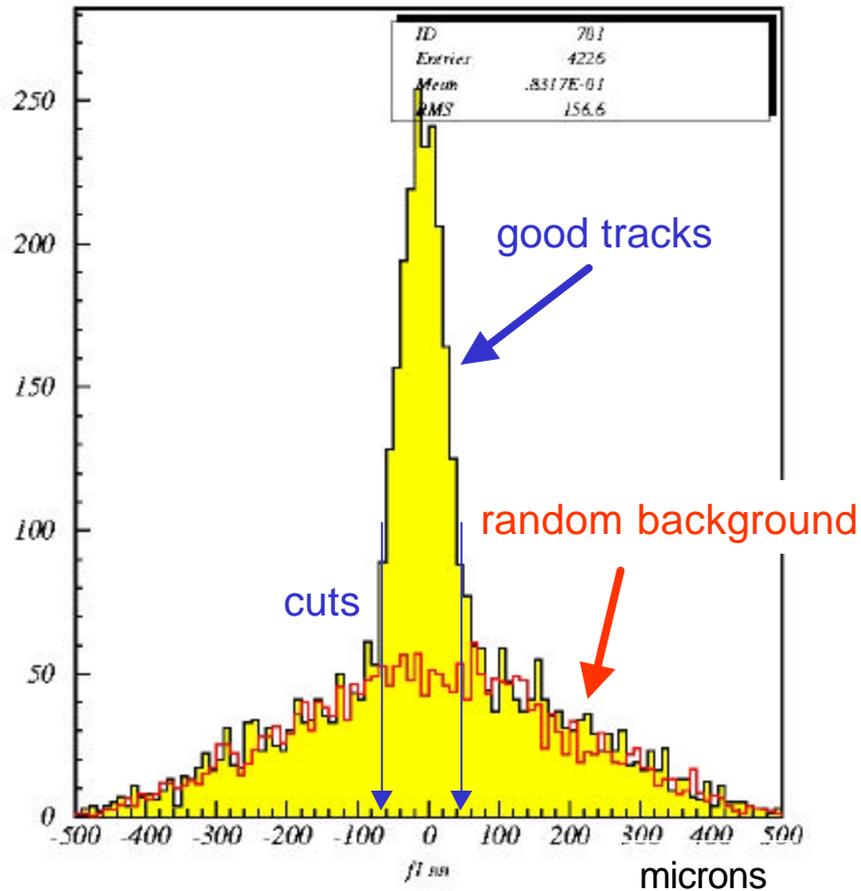


SVT crates installed in CDF counting room

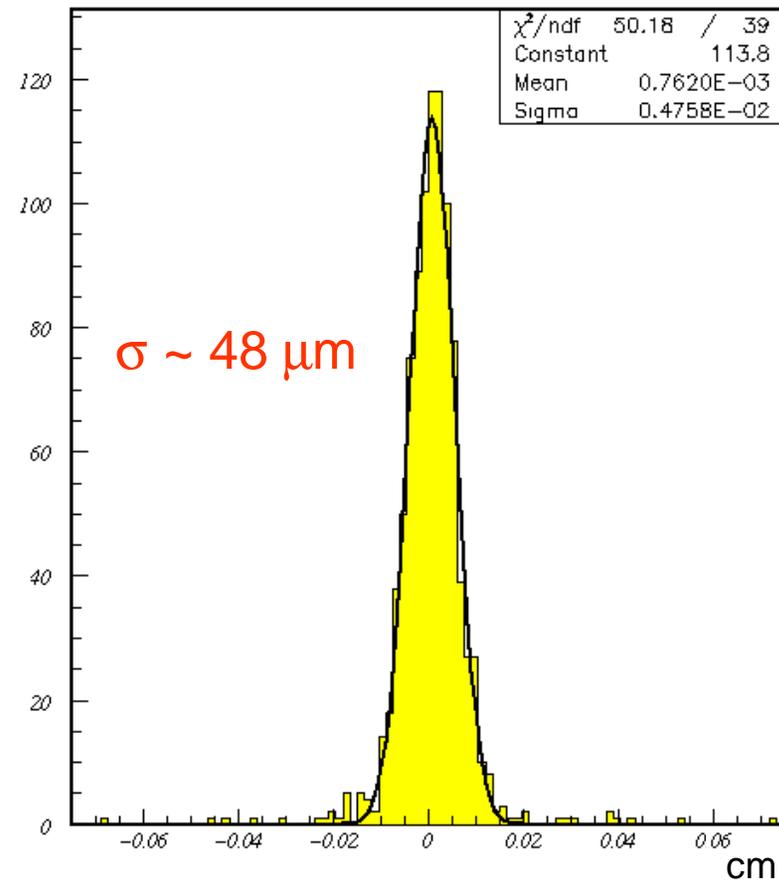


Preliminary results from CDF “commissioning run” Oct-Nov 2000

geometrical constraint



impact parameter distribution



SUMMARY

- The SVT project implied a significant step forward in the quality of fast track finding
- A massively parallel/pipelined architecture was used combined with some innovative techniques such as the **associative memory** and **linearized track fitting**
- Commissioning of SVT is well on track to allow CDF to start triggering on impact parameter soon after RunII of the Collider begins