

Cold Electronics for Very Large LAr TPCs

Veljko Radeka
BNL
for
“Cold Electronics Team”:

Gianluigi De Geronimo, Sergio Rescia, Hucheng Chen
BNL
Grzegorz Deptuch, Ray Yarema
FNAL

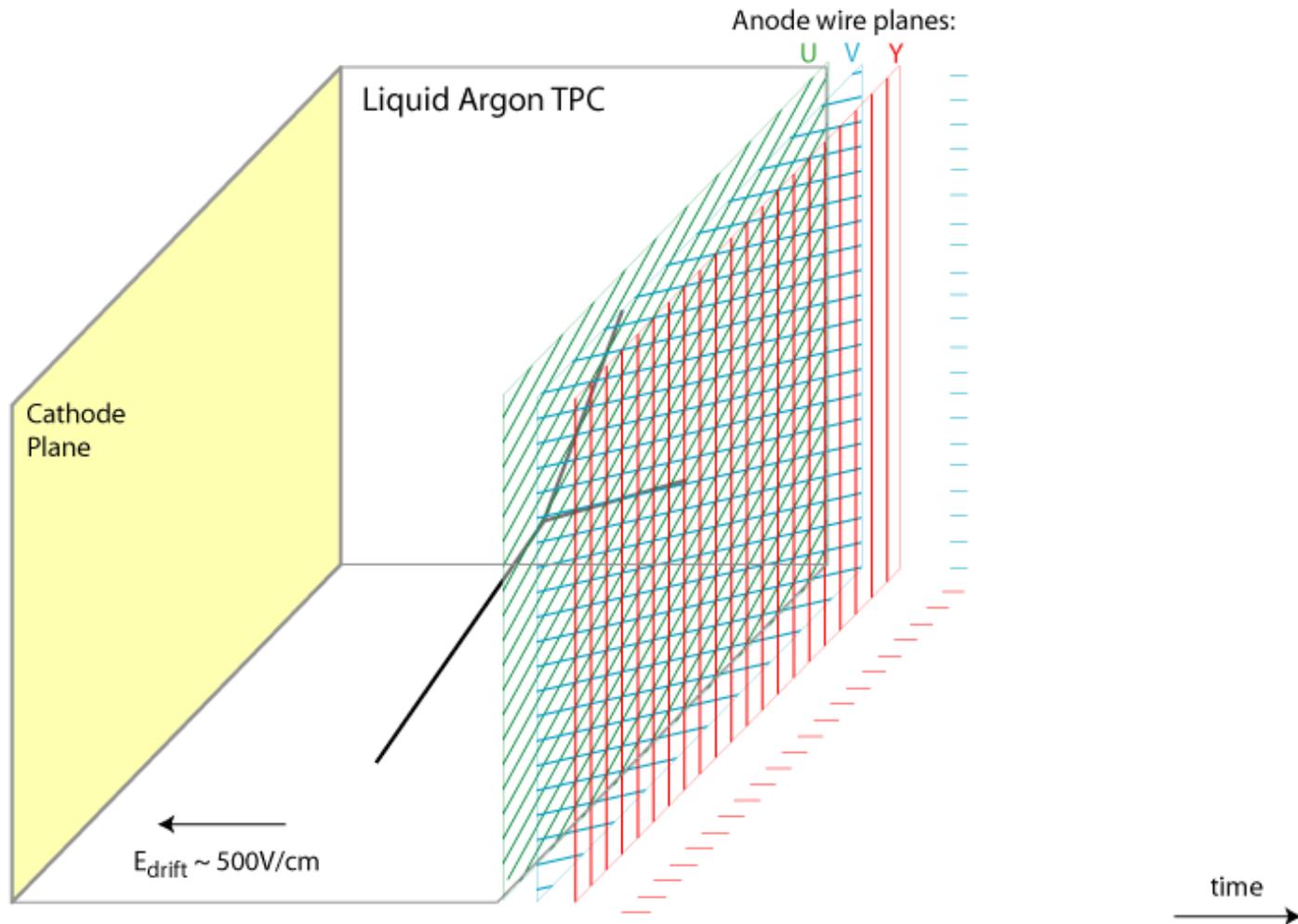
LAr20 Review, Nov 23, 2009

Outline:

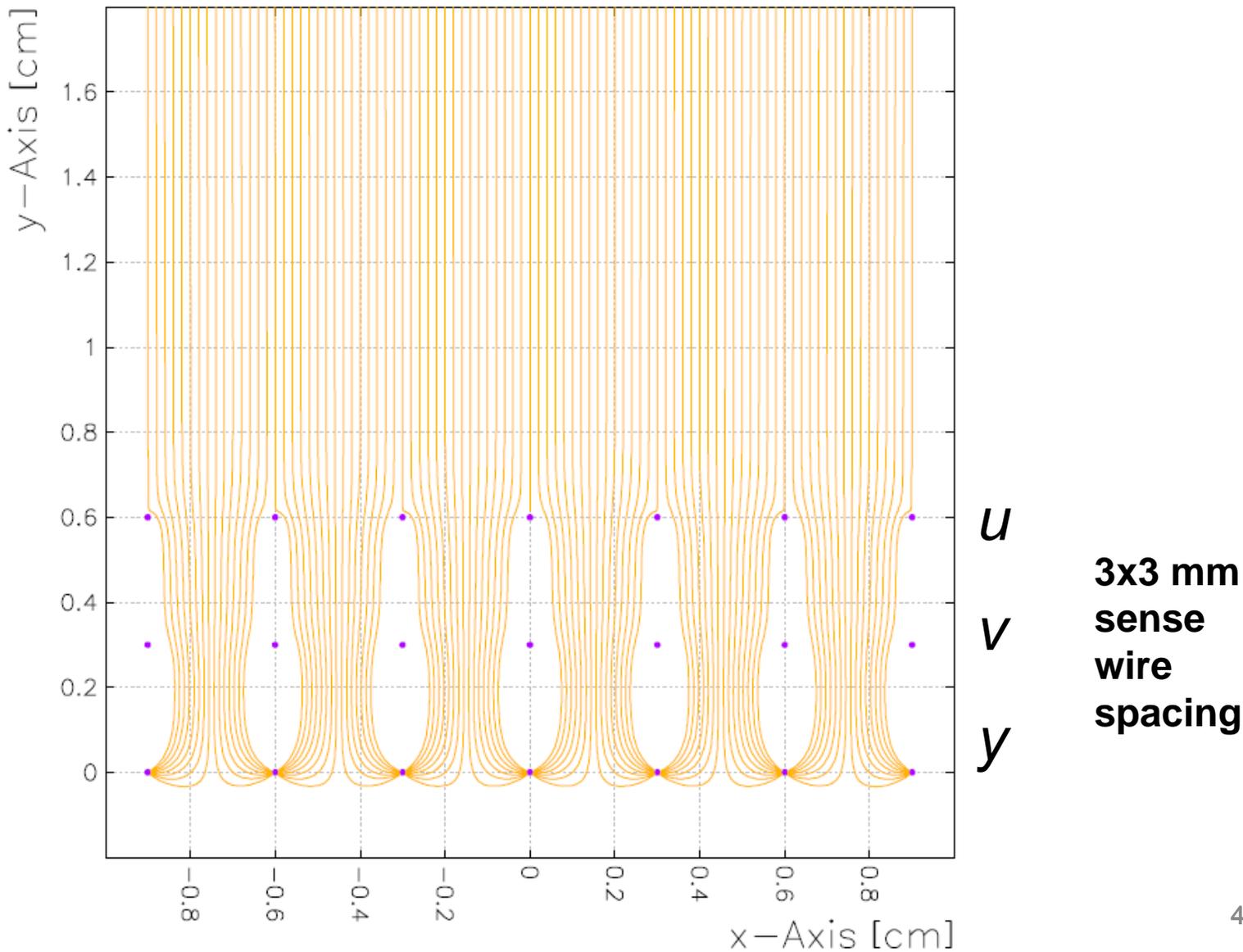
	<u>Slides:</u>
•TPC Signals:	3-6
•Noise:	7-9
•“Cold” vs “Warm” electronics:	10-12
•Readout chain concept:	13-17
•Reliability of CMOS:	18-19
•R&D plan	20-21

Large Volume LAr TPC

- 3 Wire plane readout with excellent space and energy resolution
- 3D-imaging: full event topology reconstruction
- Higher sensitivity to n physics and for some of the proton decay channels (e.g. $p \rightarrow K n$)



Using Garfield (2D) to Simulate Signal Waveform from the Wires

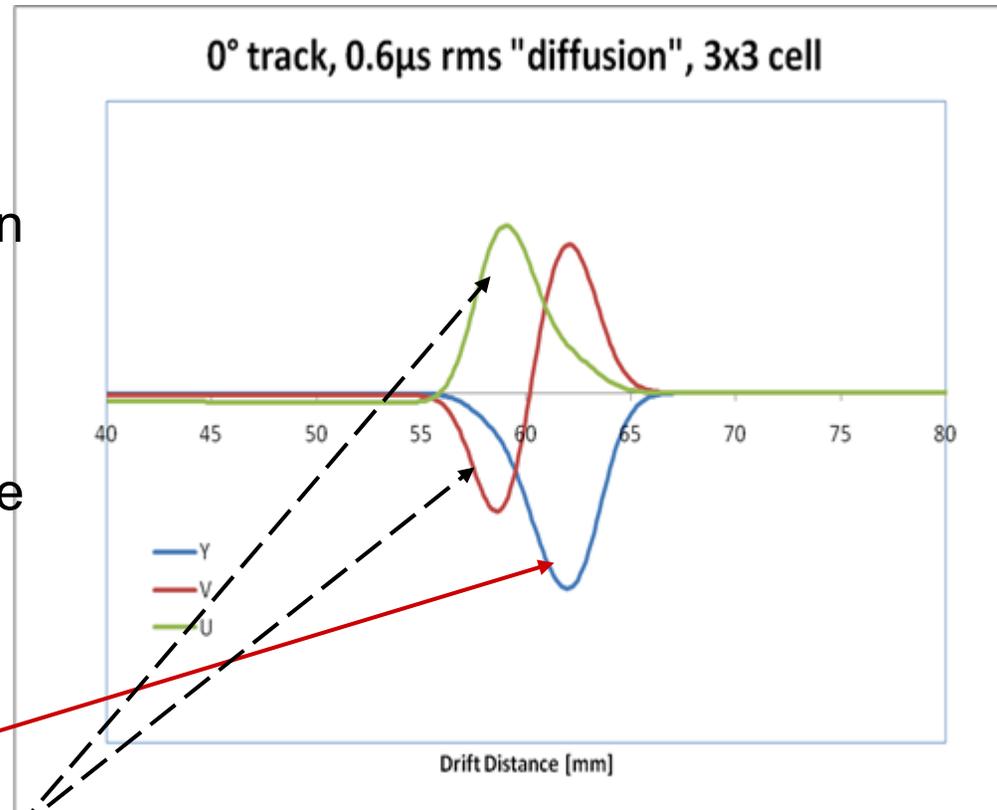


Signals in LAr TPC

Charge signal:

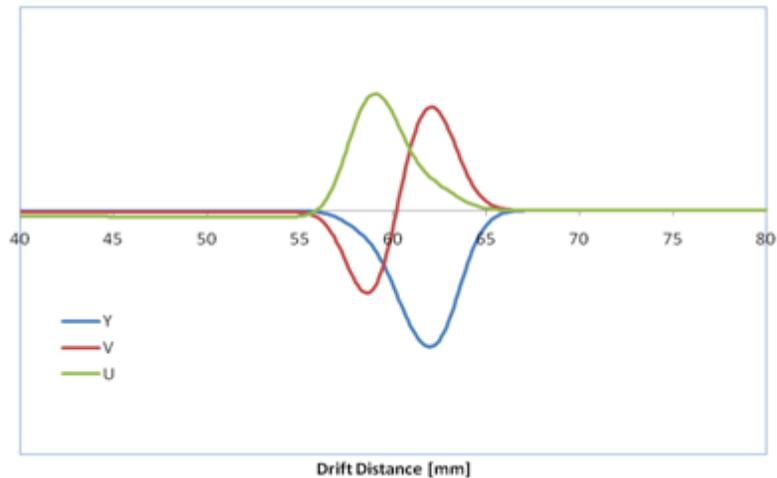
- A 3mm MIP track should create $210\text{keV/mm} \times 3\text{mm} / 23.6\text{eV/e} = 4.3\text{fC}$.
- After a 1/3 initial recombination loss: $\sim 2.8\text{fC}$
- It is expected that the TPC design will maximize the drift path to equal or exceed the charge life time, thereby reducing the signal to $1/e \approx 0.368$.
- The expected signal for **3mm** wire spacing is then $\approx 1\text{fC} = 6250$ **electrons**,
... and for **5mm**, $\approx 10^4$ **electrons**,
for **the collection signal**.
- The induction signals are smaller

Induced Current Waveforms on 3 Sense Wire Planes:

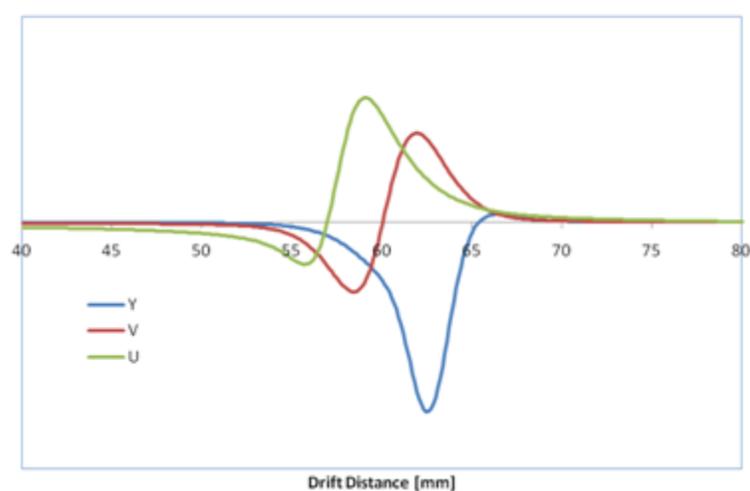


Relative Induced Current Waveforms on 3 Sense Wire Planes vs Wire Spacing and MIP Angle

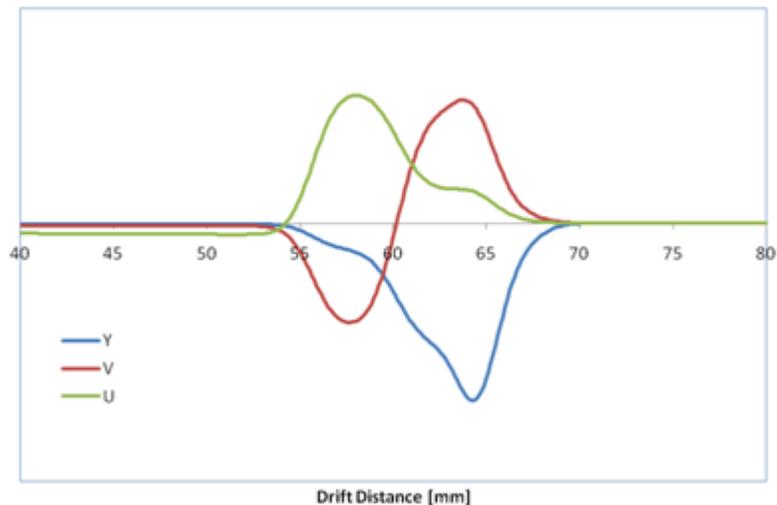
0° track, 0.6 μ s rms "diffusion", 3x3 cell



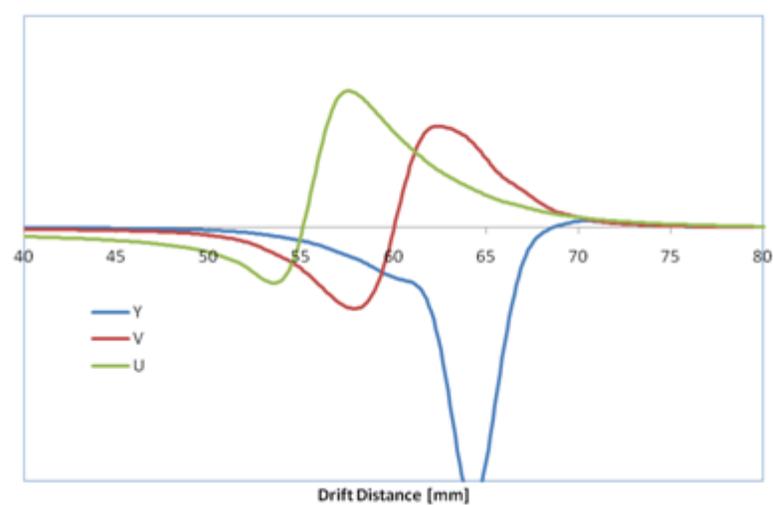
30° track, 0.6 μ s rms "diffusion", 3x3 cell



0° track, 0.6 μ s rms "diffusion", 5x5 cell

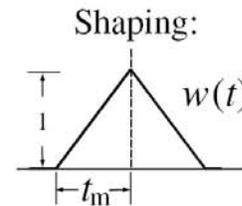
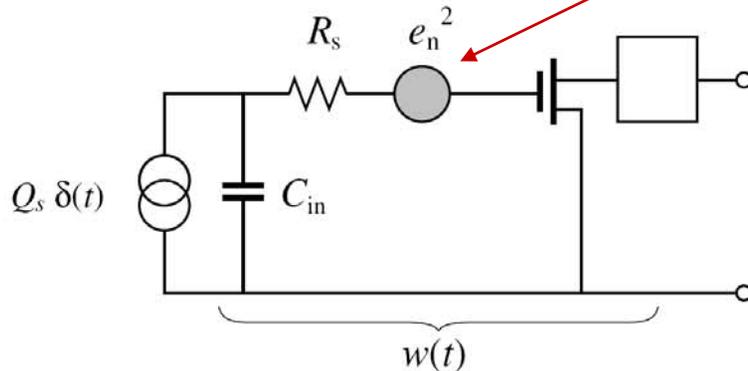


30° track, 0.6 μ s rms "diffusion", 5x5 cell



Simple ENC Calculation for *Series* White Noise

$$ENC_s^2 = \frac{1}{2} 4kTR_s C_{in} \cdot I_1$$



$$I_1 = \int_{-\infty}^{\infty} w'^2(t) dt = 2/t_m$$

(for 5th order semi-gaussian $I_1 = 2.2$)

$$ENC_s = e_n C_{in} / t_m^{1/2}$$

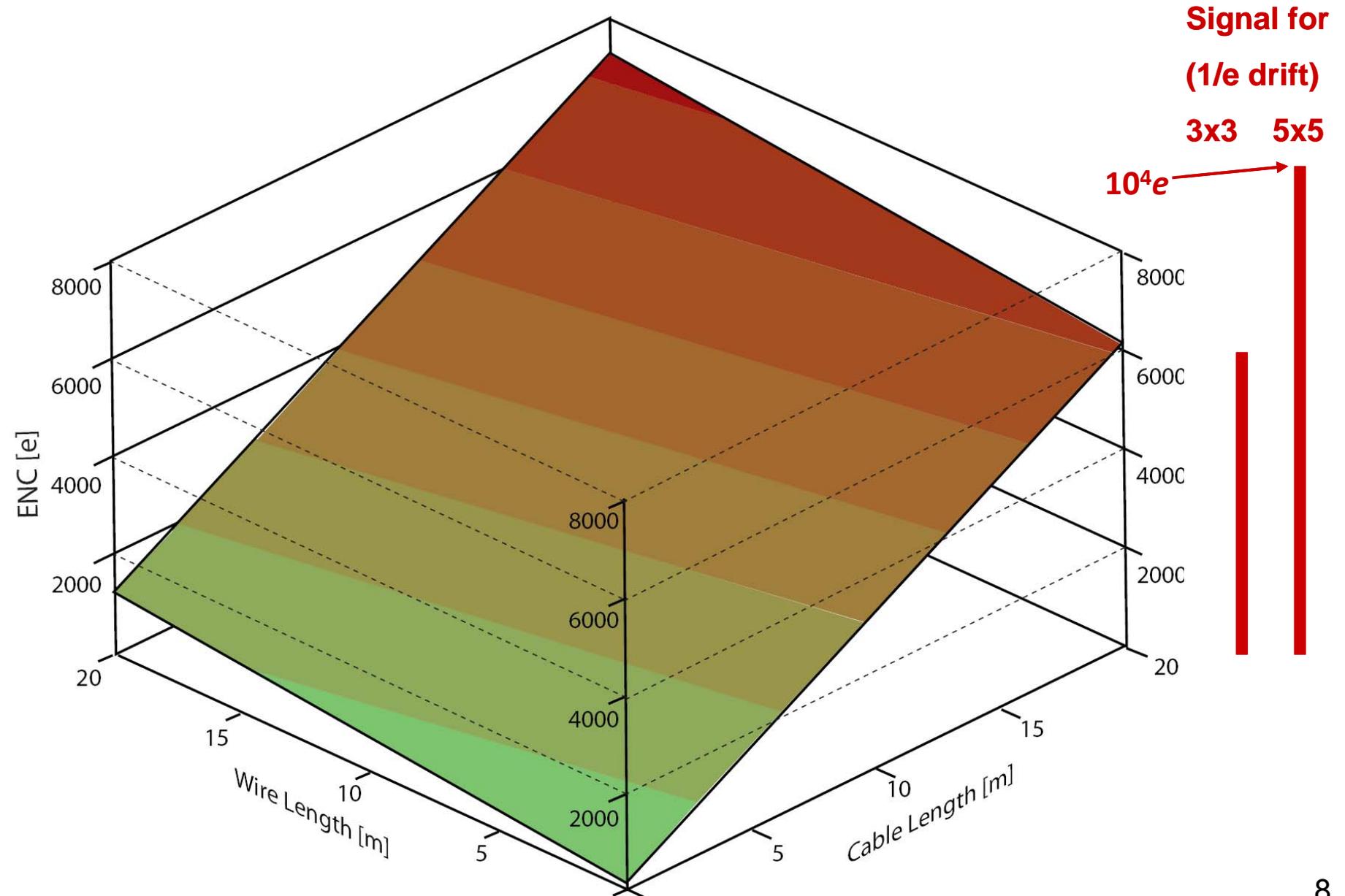
Lowest practical values for spectral density: $e_n \sim 0.5 \text{ nV/Hz}^{1/2}$
 resulting in $\Delta ENC / \Delta C \sim 3 \text{ rms e/pF}$ at $t_m = 1 \mu\text{s}$

$$\begin{aligned} e_n &= 1 \text{ nV/Hz}^{1/2} \\ C_{in} &= 1 \text{ pF} \\ t_m &= 1 \mu\text{s} \end{aligned}$$

$$\rightarrow ENC_s \approx 6 \text{ rms e} \rightarrow \Delta ENC_s / \Delta C_{in}$$

e_n = series noise (**voltage**) spectral density [V/Hz^{1/2}]
 $e_n C_{in}$ = series noise (**charge**) spectral density [e/Hz^{1/2}]

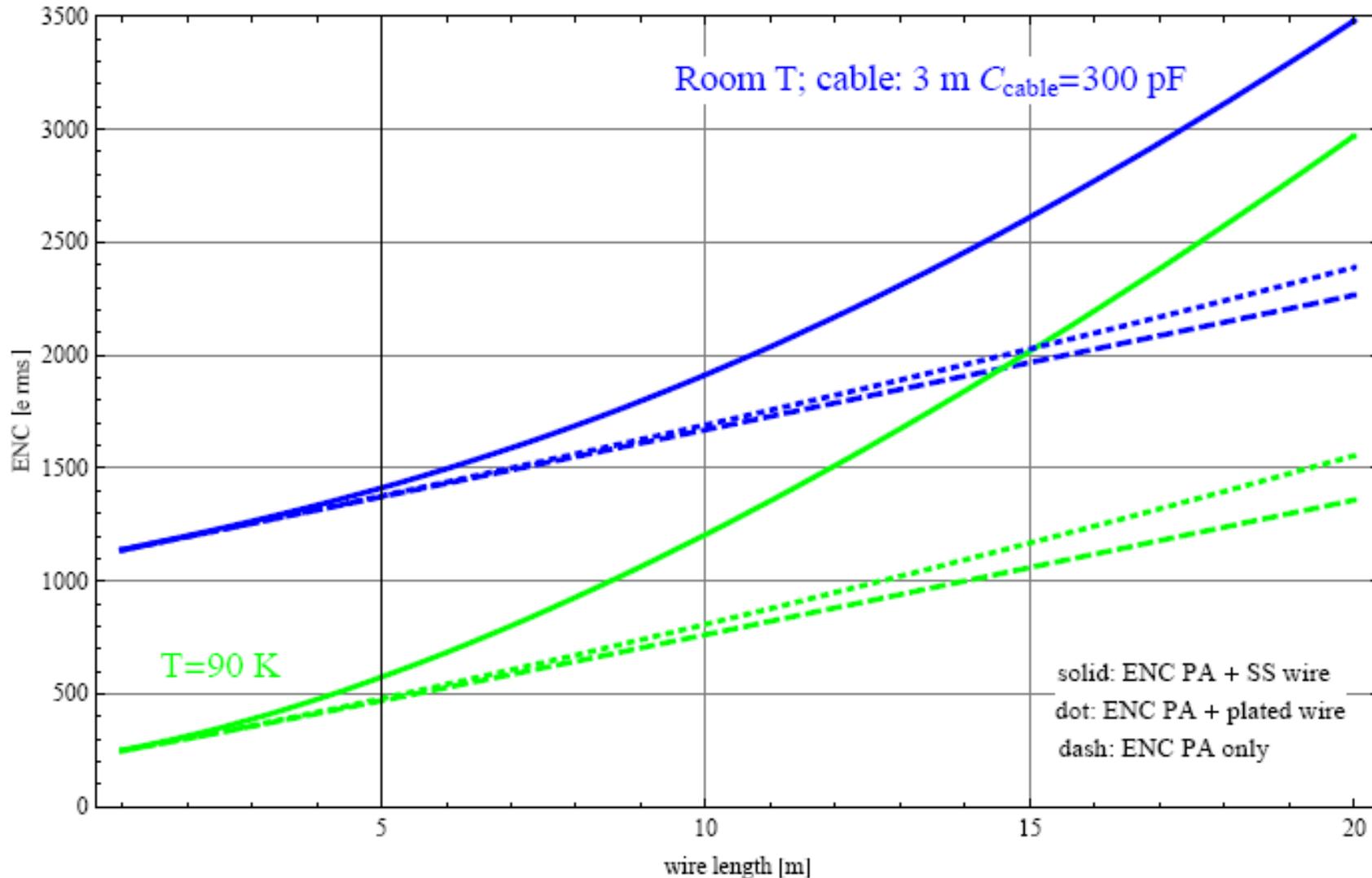
Noise vs Sense Wire and Cable Length



ENC vs Sense Wire resistance

SS sense wire 150 μ m (36ohm/m) and Cu+Au plated SS wire (3 ohm/m)

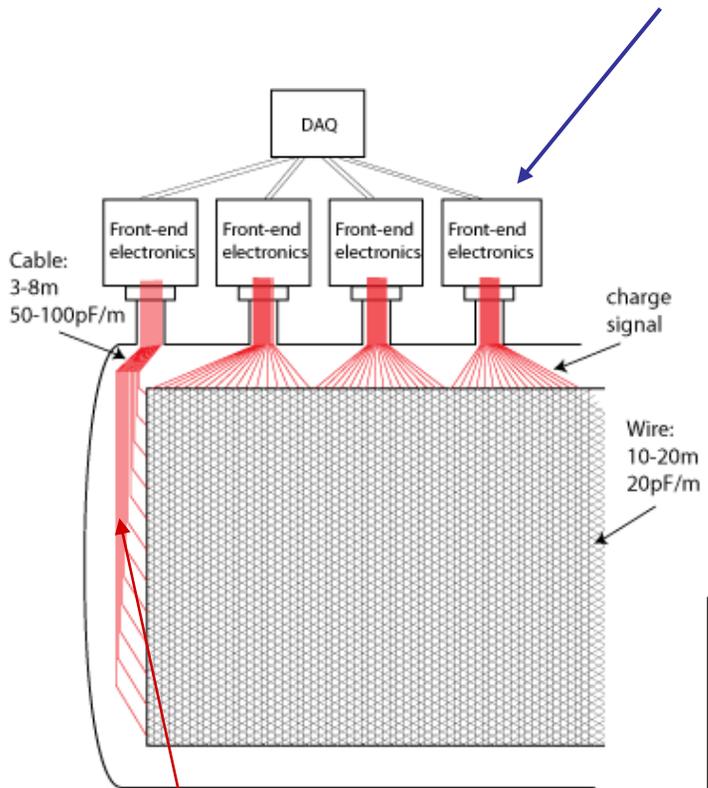
Stainless steel 150 μ m wire (36 Ω /m) and Cu/Au plated wire (3 Ω /m)



Number of Wires (signal channels) in Large TPC Detectors – an illustration:

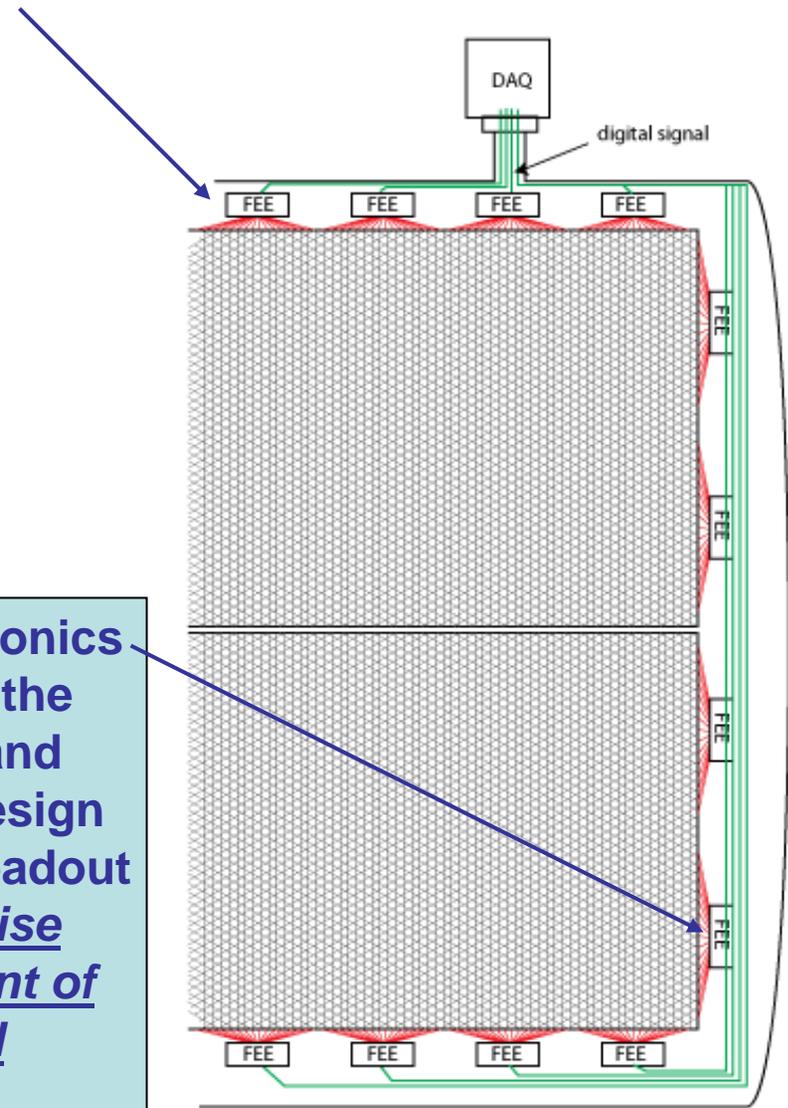
- **A lower limit**: If we assume the sense wire length of **10 meters**, the electron drift distance of **2.5 meters** and the sense wire spacing **5mm x 5 mm**, the number of sense wires (and readout channels) for a 3-coordinate readout will be **~18/ton** in a large module.
- **An upper limit**: Sense wire length = **5 meters**, electron drift distance = 2.5 meters, sense wire spacing, **3mm x 3 mm**, the number of sense wires (and readout channels) for a 3-coordinate readout will be **~60/ton** in a large module.
- A possible **intermediate case**: Sense wire length = **5 meters**, electron drift distance = 2.5 meters, sense wire spacing, **5mm x 5mm**, the number of sense wires (and readout channels) for a 3-coordinate readout will be **~36/ton** in a large module.

Cryostat Design: “Warm” vs “Cold” Electronics



Signal cable lengths increasing to >10-20 meters for detector fiducial volume > 1kton resulting in high capacitance and high noise.

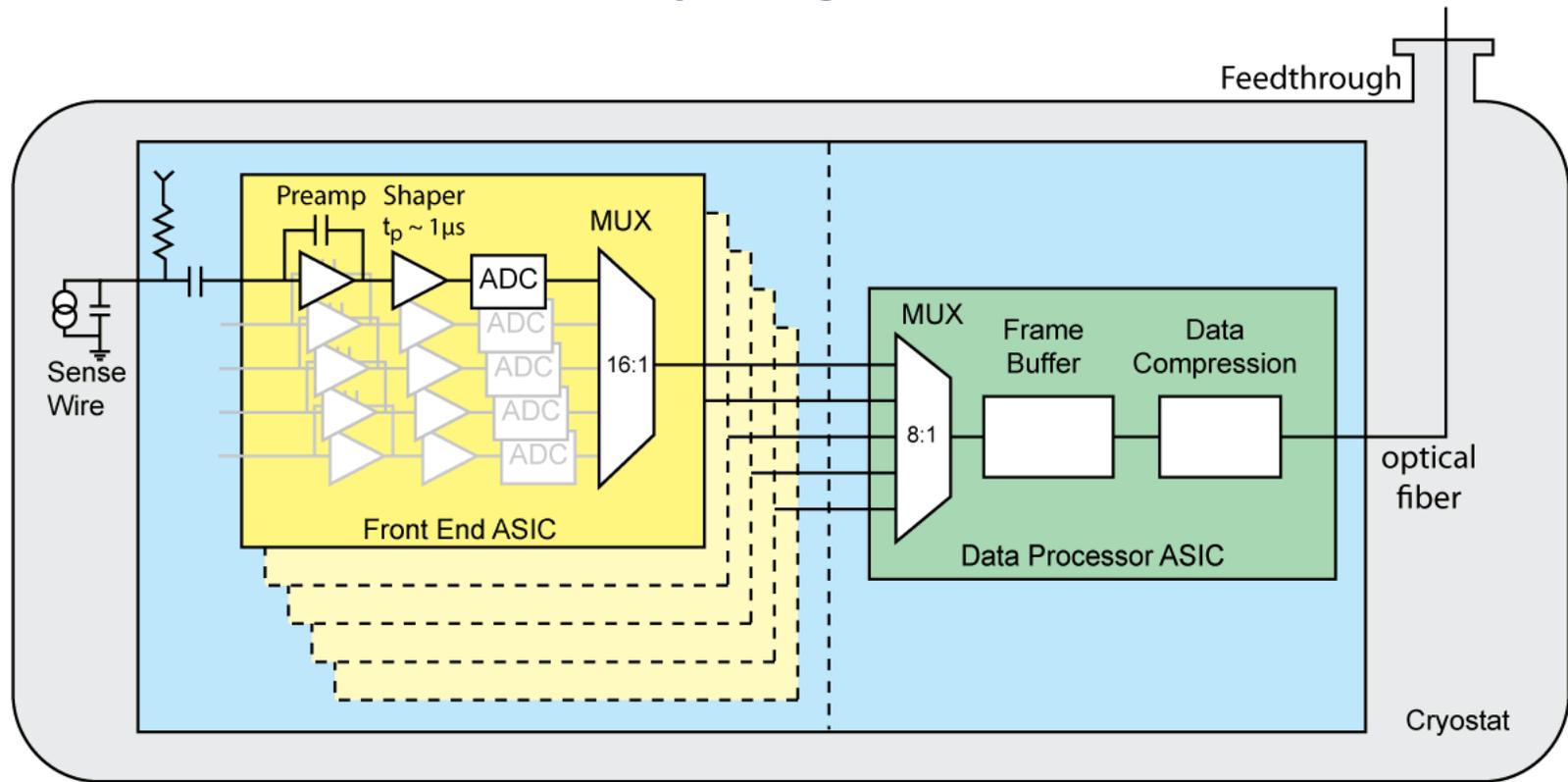
Cold electronics decouples the electrode and cryostat design from the readout design: noise independent of the fiducial volume.



“Cold” vs “Warm” Summary:

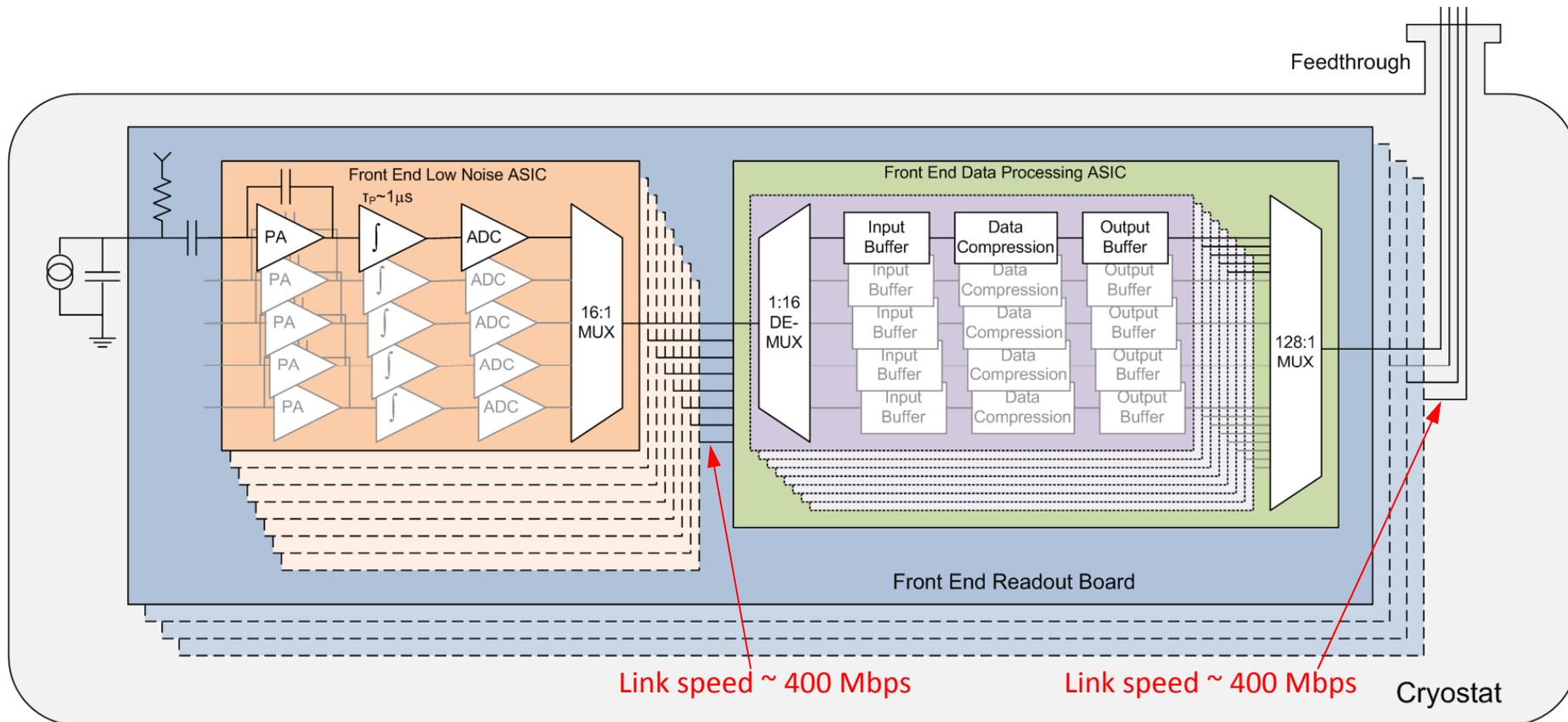
- For detector fiducial volume > 1 kton signal cable lengths of >10 - 20 meters will be required due to the cryostat size to bring the signals from the sense wires to the feedthroughs (and *external warm electronics*) resulting in high capacitance and high noise. (The feedthroughs will have to be located on top of the cryostat to minimize the heat input and to simplify the construction of the cryostat.)
- *Cold electronics* will make possible to decouple the electrode and cryostat design from the readout design (no limit on the cable length within the cryostat after the signals are amplified and digitized at the sense wires, so that *the noise will be independent of the fiducial volume and much lower than with the warm electronics*).
- Signal multiplexing within the cryostat will result in a large reduction in the quantity of cables (less outgassing) and the number of feedthroughs/penetrations (lower cost and probability of leaks).

A Functional Outline of a Multiplexed Readout Chain for Very Large LAr TPCs



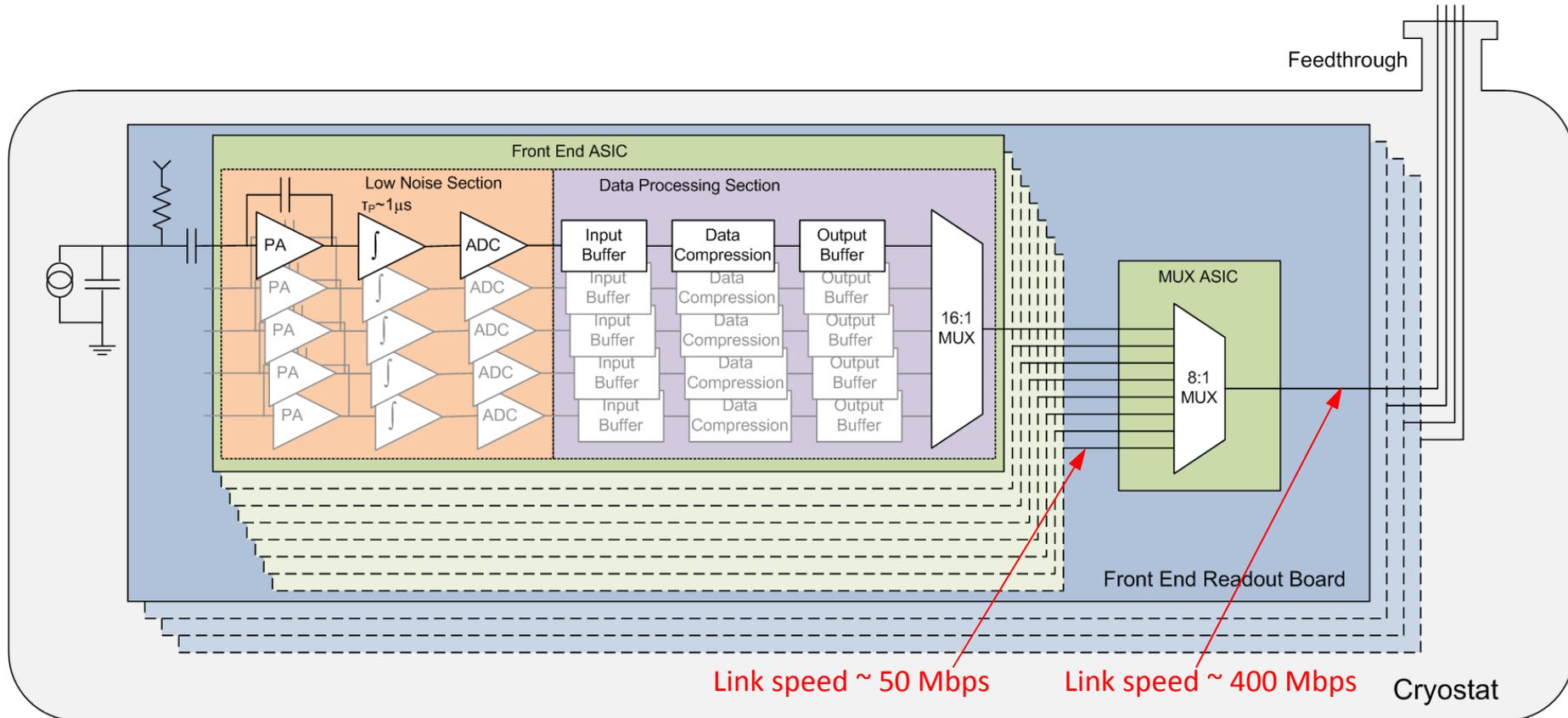
A Functional Outline of a Multiplexed Readout Chain for Very Large LAr TPCs. Multiplexing will be performed in two steps at appropriate locations within the cryostat. A CMOS, or a BiCMOS technology with circuit design and operating conditions for long term operation in LAr will be used. A preliminary goal is **multiplexing in two steps by $16 \times 8=128$** . Power dissipation has been estimated to be $\leq 10\text{mW/signal wire}$.

LAr20 Front End Electronics



- Option 1: **Two separate front end ASICs**
- Low noise ASIC and data processing ASIC could be developed and tested independently, higher yield
- Two ASICs could adopt different technologies with different voltages if necessary

LAr20 Front End Electronics (con't)

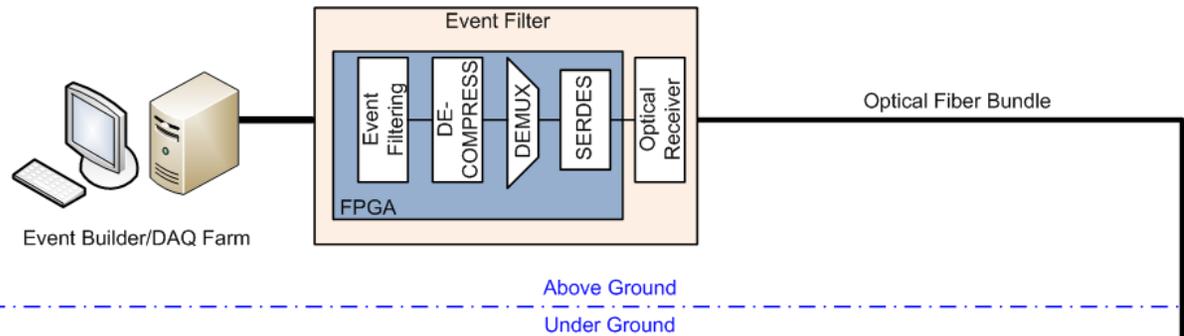


- Option 2: **One front end ASIC** with one MUX ASIC
- Eliminate multiplex and de-multiplex blocks
- Complex mixed signal ASIC design, layout of the front end ASIC has to be considered carefully to eliminate any potential impact on noise performance; lower yield

LAr20 Readout Requirements

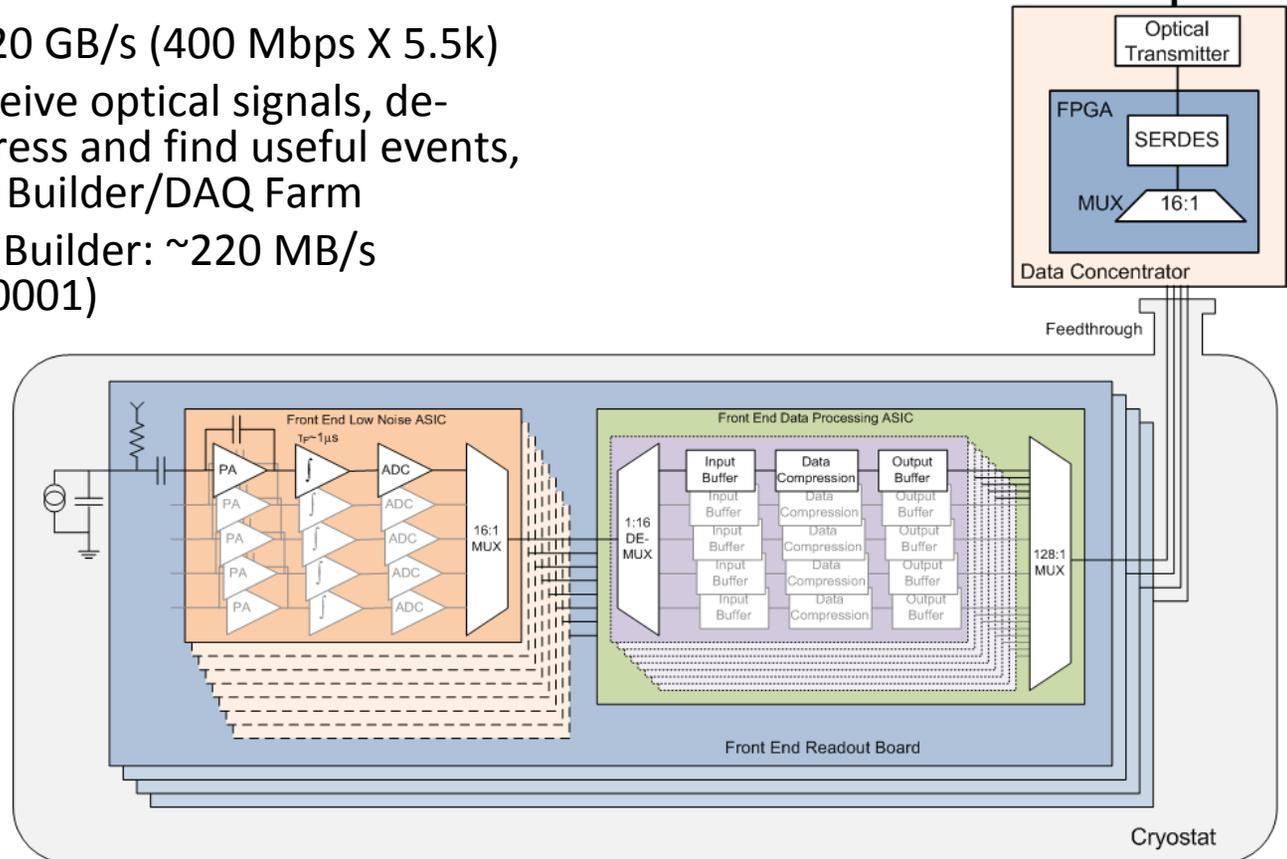
- Number of Detector Wires: ~700k
 - Detector volume is ~**20** kton
 - ~**35/ton** for 2.5 m drift distance, 5 m wire length, 5 mm wire pitch
- Number of Readout Links: ~5.5k
 - With multiplex factor of 128 implemented in ASIC to transmit data out of the cryostat
 - Link speed is ~400 Mbps with 2 MSPS 12 bit ADC
- Number of Fiber Optical Links: ~350
 - With multiplex factor of 16 implemented in FPGA on Data Concentrator board to transmit data to DAQ farm through optical link
 - Fiber optical link speed is ~**6.4** Gbps

LAr20 Readout Scheme



- Event Filter

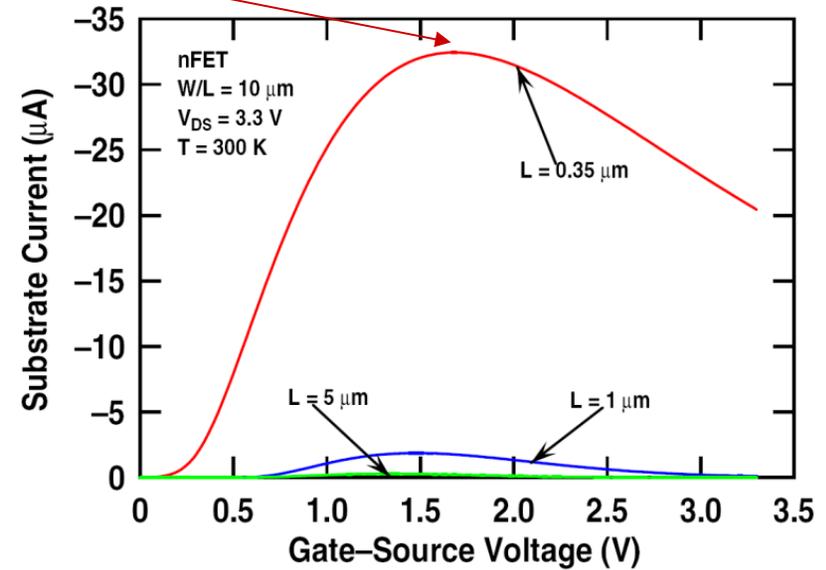
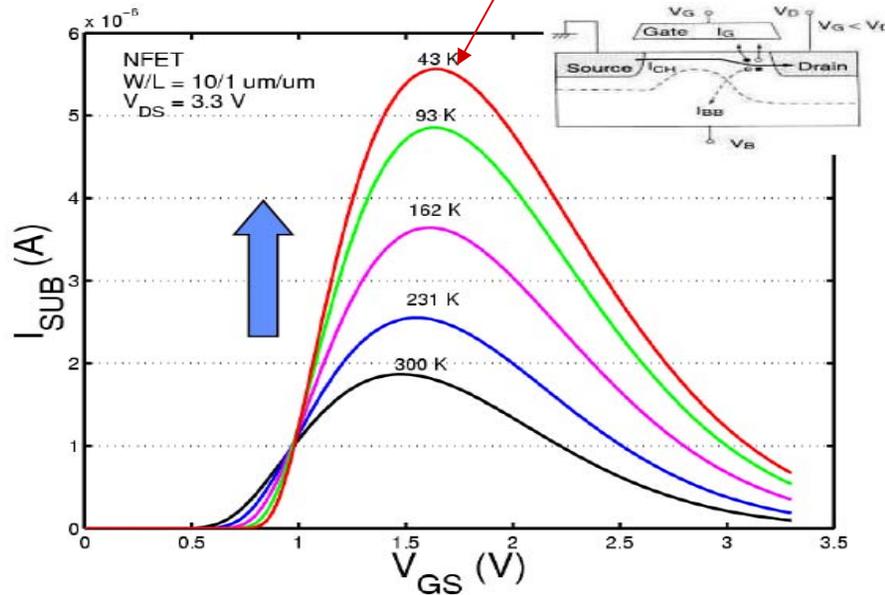
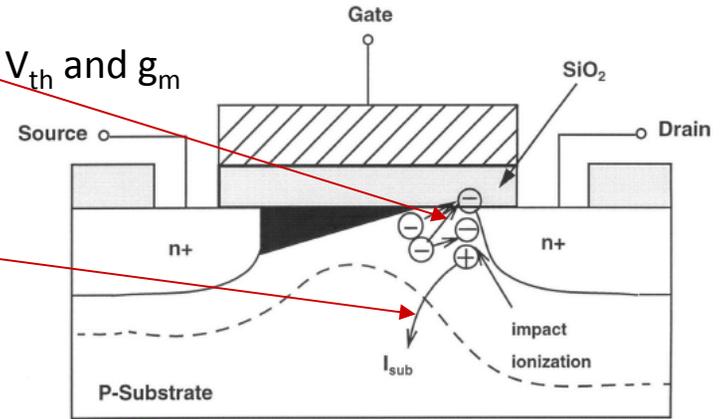
- Raw Data Rate: $\sim 220 \text{ GB/s}$ ($400 \text{ Mbps} \times 5.5\text{k}$)
- Event Filter will receive optical signals, de-multiplex, decompress and find useful events, then send to Event Builder/DAQ Farm
- Data Rate to Event Builder: $\sim 220 \text{ MB/s}$ ($200\text{GB/s} \times 10 \times 0.0001$)



CMOS Reliability at Cryogenic Temperatures – Basic Mechanism

- **Degradation** is due to **impact ionization**
 - charge trap in oxide, interface generation → shift in V_{th} and g_m
- **Substrate current** is a **monitor of impact ionization**

- increases with drain voltage
- is higher in short channel devices
- has a maximum at $V_{gs} \approx V_{ds}/2$
- increases as the temperature decreases



- Commercial technologies are rated 10 years lifetime (10% shift) in worst case continuous operation: $T = 220 \text{ K}$, $L = L_{min}$, $V_{ds} = \text{nominal } V_{dd}$, $V_{gs} \approx V_{ds}/2$

• **Accelerated tests at increased V_{ds} allow extrapolation of lifetime**

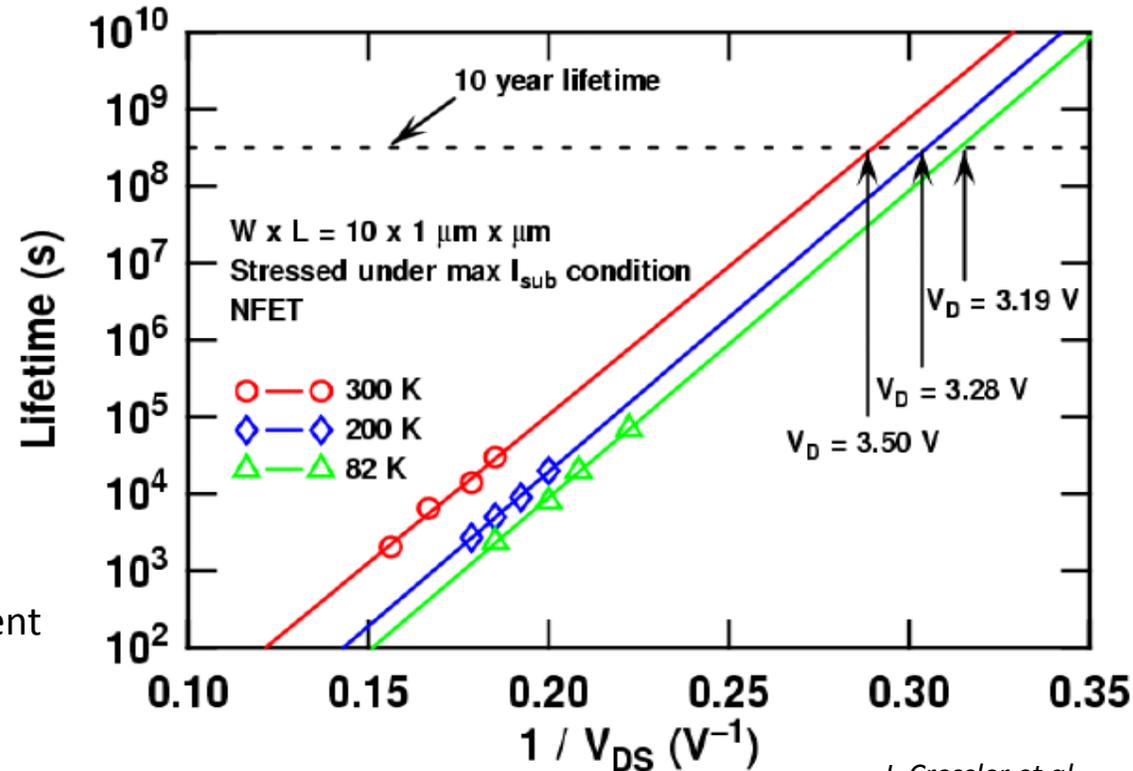
CMOS Reliability at Cryogenic Temperatures – Design Guidelines

- **Reliability at low temperature can be guaranteed by:**

1. decreasing V_{ds} (i.e. decreasing the supply voltage)
2. decreasing V_{gs} (i.e. decreasing the drain current density)
3. increasing L (i.e. non-minimum channel length devices)

- **Design guidelines:**

1. analog circuits
 - operate devices at low current density
 - use non-minimum L
1. digital circuits
 - operate devices at 2/3 of nom. V_{dd}
 - use non-minimum channel length



J. Cressler et al.

Accelerated tests will be performed to guarantee > 10-20 years lifetime at 90 K (operated at V_{dd} and max. current continuously)

Collaboration with Georgia Tech on Cryogenic Electronics

- **Strong group led by J. Cressler, with experience in “extreme environment” electronics (development for NASA of electronics for the Lunar Base Station project).**
- **Expertise in cryogenic CMOS and BiCMOS (SiGe HBJT), Cressler was a key person in developing SiGe process at IBM.**
- **Cressler has agreed to collaborate with BNL/FNAL in development of cryogenic electronics for LBNE.**
- **Topics:**

- 1. Process and device reliability qualifications**
- 2. Device testing at cryogenic temperature**
- 3. Device modeling at cryogenic temperature**
- 4. Development of circuit blocks needed in the system (e.g. bandgap reference, voltage regulator).**

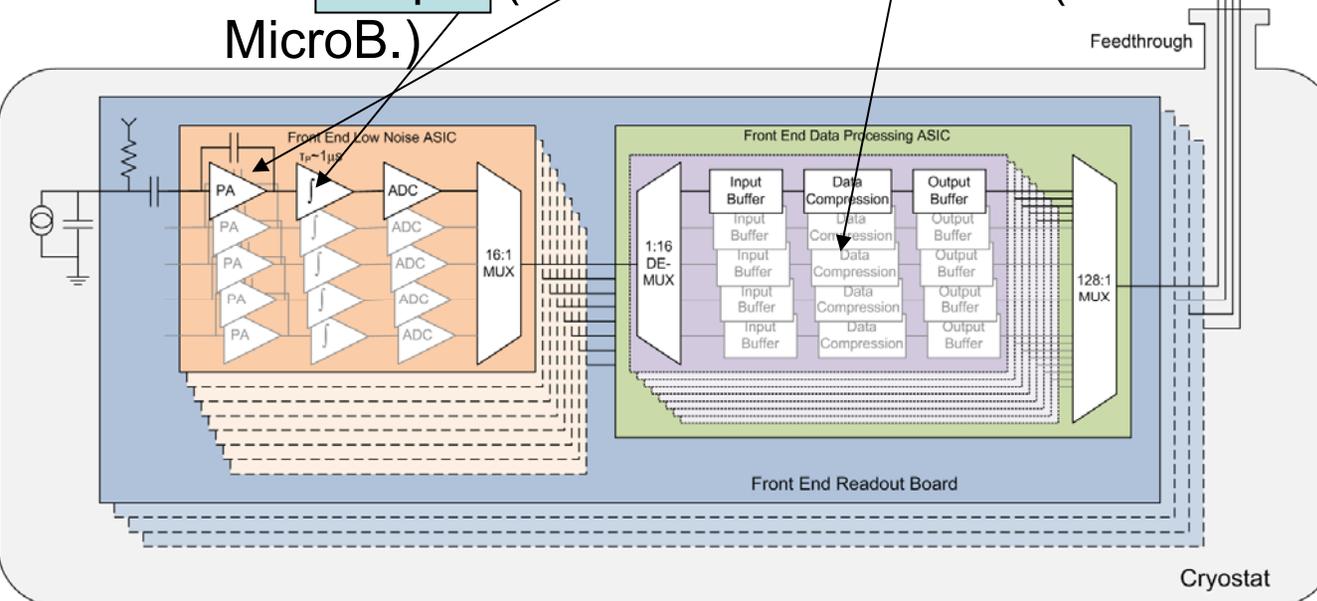
Outline of R&D Plan on ASICs for 90K

Fast Track (prior to CD1):

1. Test single device parameters (noise, etc.) from 3 suppliers (Chartered, IBM, TSMC);
2. Design, fabricate, test circuit blocks: preamp and shaper (later test in MicroB.)

R&D toward integration of the whole cold readout chain (next 2-3 years):

1. Investigate data compression schemes and proceed with digital circuits design.
2. Investigate transmission of data from the cryostat (electrical vs optical).



(Note: All devices and assemblies will be verified on thermal contraction issues: considerable positive experience on this exists from previous LAr, LKr projects.)