

R&D on Readout for Very Large Liquid Argon TPCs

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1. Introduction

Our R&D objective is to develop electronics technology suitable for readout of very large LAr TPCs, such as a progression of modules, 5+25+30+30 kton for DUSEL.

In such detectors, the key issue is ***feasibility of scaling in size*** before reaching the fundamental limits in terms of the signal-to-noise, and technological limits in terms of the readout and cryostat complexity. If most or all of the active electronic components are at ambient temperature outside the cryostat, the number of signal electrodes (sense wires) that can be read out is largely limited by the number of signal feedthroughs (cryostat penetrations) and complexity of the signal cables. This compels the designer of a very large TPC with external (“warm”) electronics toward a detector with ***long drift distances, long sense wires and long cables*** in an effort to avoid large numbers of signal channels exiting the cryostat. The ***signal-to-noise ratio*** (i.e., the detector sensitivity) suffers twofold, from the ***attenuation of the signal charge*** during a long drift and from the ***increased electronic noise*** due to the capacitance of very long sense wires and long cables. The long drift distance leads also to very high purity requirements for LAr. The combination of high purity, long sense wire and long signal cables makes for a difficult detector design. We propose an approach where these shortcomings of the conventional approach are alleviated.

Advances in microelectronics, and in particular in ***low-noise-low-power electronics*** for detectors, have led us to propose an approach where the readout electronics with a ***high degree of multiplexing*** (by ~100 or more) will be inside the cryostat. This will allow greater freedom in the choice of the electrode granularity (length and pitch of the sense wires) and in the choice of the drift distance. The length of the cables (or optical fibers) after multiplexing becomes much less critical than with external warm electronics and it allows more freedom in cryostat modules shape and configuration. In particular, cryostat designs with feedthroughs (“chimneys”) on other cryostat walls than the top become unnecessary. The cold electronics at the electrodes with moderate sense wire lengths and no cables between the sense wires and the amplifiers leads to a superior signal to noise ratio and detection sensitivity.

We outline here an estimate of the benefit in the signal to noise ratio for various combinations of the sense wire lengths and cable lengths, and propose a plan for development of CMOS and BiCMOS readout electronics to be operated immersed in liquid argon.

2. TPC Signals

The simplest electrode configuration which allows track reconstruction with dE/dx measurements consists of three planes of sense wires, arranged as illustrated in Fig.1.

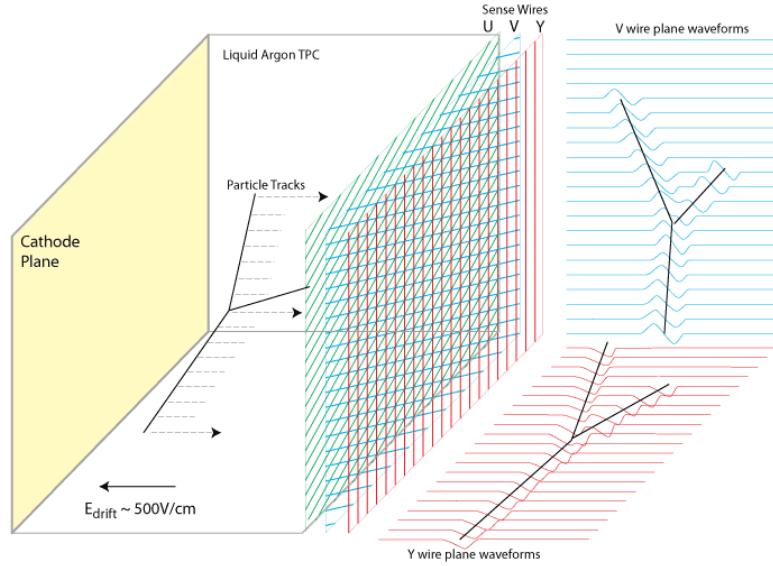


Fig. 1(a). An illustration of the TPC electrode configuration

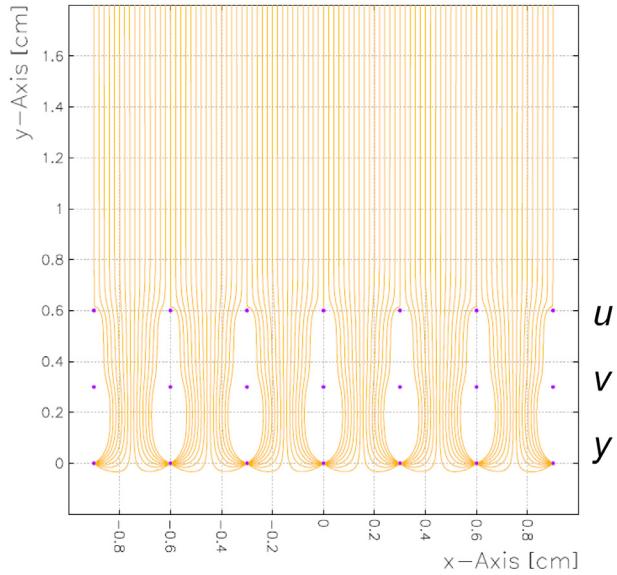


Fig. 1(b). A planar illustration of electric field lines (i.e., electron trajectories). The wires in the induction planes u and v are inclined at ± 60 degrees with respect to wires in the y plane.

This configuration is based on a square cell, where the sense wire pitch is equal to the spacing between the wire planes. Under a constraint that each wire is read out, variations in the ratio of these dimensions (i.e., departure from the square cell) offer no overall advantage. More ideal electrode configurations would all require either more wires (to form denser grids), or pad/pixel electrodes in great numbers, where the costs and mechanical construction requirements would become prohibitive.

Two sizes of the square cell have been used or are under consideration: 3mm x3mm and 5mm x 5mm, the former in ICARUS and MicroBOONE, and the latter in the studies for DUSEL. An estimate of the charge signal size on the collection wire plane for a track perpendicular to the sense wire and parallel to the wire plane is as follows:

- A 3mm MIP track should create $210\text{keV/mm} \times 3\text{mm} / 23.6\text{eV/e} = 4.3\text{fC}$.
- After a 1/3 initial recombination loss (at 500V/cm): $\sim 2.8\text{fC}$. This would be the maximum signal for tracks close to the wire planes.
- It is expected that the TPC design will maximize the drift path to equal or exceed the charge life time, thereby reducing the signal to $1/\text{e}\approx 0.368$.
- The expected signal for 3mm wire spacing is then $\approx 1\text{fC}=6250\text{ electrons}$.
- The expected signal for 5 mm wire spacing is $\approx 10^4\text{ electrons}$.
- The induction signals on the first and second wire plane are smaller as shown in Fig. 2.

These signal sizes are for a track perpendicular to the sense wire and parallel to the wire plane. For track inclinations α and β with respect to this orientation, the signal has to be multiplied by $1/(\cos\alpha \cdot \cos\beta)$.

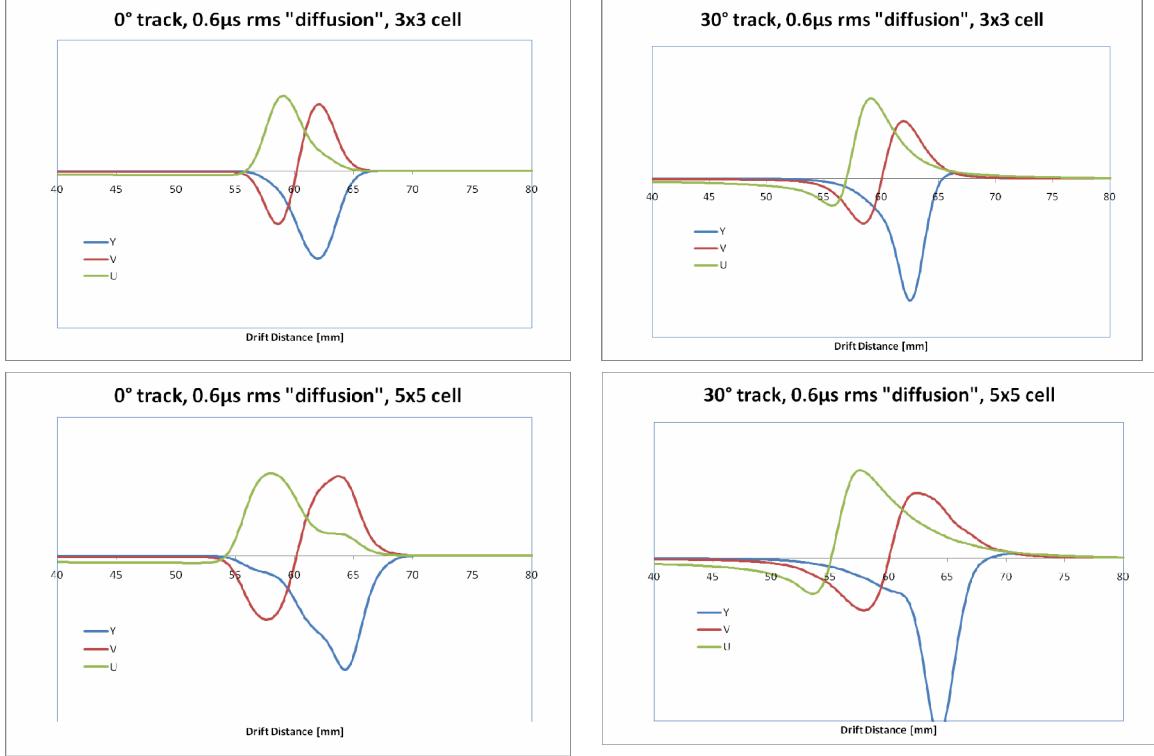


Fig. 2. Induced current waveforms. Wire plane spacing and electron drift velocity determine the time scale of the signals and of all the subsequent signal processing. The transit time between the two planes is about 2 and 3 microseconds for the 3mm x 3mm and 5mm x 5mm cells respectively, for an assumed drift field of 500V/cm. All four sets of signal waveforms have the same horizontal and vertical scale.

3. Electronic Noise

We consider here only the unavoidable sources of noise: 3.1. The ***first transistor noise*** associated with the physics of amplification, and 3.2. The ***thermal noise from the sense wire*** and connection leads (signal cable). We assume that any resistors connected to the amplifier input, such as the feedback and sense wire bias resistors, are chosen so that their thermal noise is negligible.

3.1. The ***first transistor noise*** contribution to the measured signal charge is due to the total capacitance, comprised of the sense wire capacitance, cable capacitance and input transistor capacitance. ***This total capacitance limits the signal-to-noise ratio and it is the one dominant factor on which the feasibility and scalability of a LAr TPC design critically depends.*** This noise contribution is well understood, and the result has been well established analytically and experimentally. The equivalent noise charge (ENC_A) due to the first transistor noise (thermal noise in the case of field effect transistors) can be expressed as,

$$ENC_A^2 = e_n^2 C_{tot}^2 / t_p$$

where : $e_n^2 = 4k_B T R_{sn}$ = transistor series noise spectral density in $[V/Hz^{1/2}]$

R_{sn} =transistor equivalent series noise resistance

$$C_{tot} = C_{wire} + C_{cable} + C_{ampl} \quad (1)$$

t_p = weighting function peaking time = 1 / bandwidth

k_B =Boltzmann constant

3.2. **Thermal noise from the sense wire** is calculated based on the transmission line model of the sense wire. The equivalent noise charge can be expressed as,

$$ENC_w^2 \cong 4k_B T C_w^2 \left(\frac{R_w}{3} \right) \left(\frac{1}{t_p} \right)$$

where : C_w =sense wire capacitance

R_w =sense wire resistance

(2)

The sense wire noise contribution is equivalent to that of a resistor equal to one third of the wire resistance inserted between the receiving end of the wire and the amplifier. This contribution becomes significant for long sense wires (10 to 20 meters) if stainless steel is used. It can be made negligible by using Cu+Au coated stainless steel, or Cu+Be.

Both expressions (1) and (2) for ENC contain a weighting function width parameter $t_p = \tau$ (the inverse bandwidth). We assume here the simplest weighting function, illustrated in Fig. 3. This function is optimal for transistor white noise and an impulse signal.

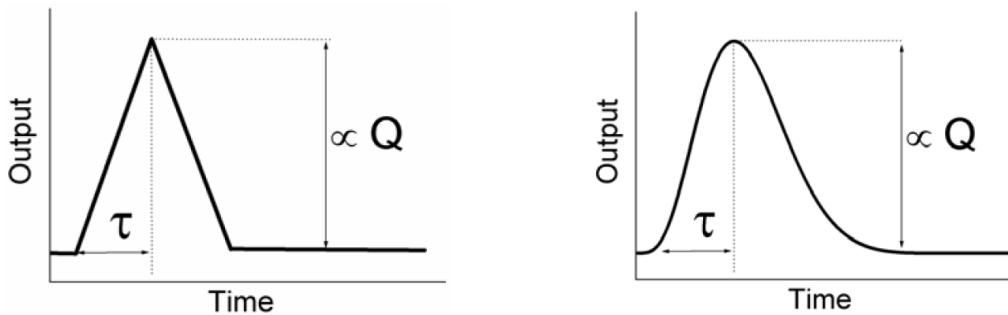


Fig. 3. Signal processing weighting functions: *triangle* is the theoretical optimum for amplifier white series noise and impulse signal; *semigaussian* is easily realized in practical circuits. $t_p = \tau$ in Eqs. (1) and (2), and it results in an ENC within few percent of the triangular one.

In a large TPC we will use different weighting functions to optimize separately the measurements of dE/dx , track segment position coordinates, timing and double track resolution. A function of the type in Fig. 3 will be used for “prefiltering” or “band limiting” prior to sampling. This function will be realized in the front end (preamplifier and pulse shaper) analog circuits. Desired weighting functions for the specific measurements listed above will be realized by weighting multiple samples in subsequent digital processing. For the electron transit times from one wire plane to another of 2-3 microseconds, we choose $t_p=1\mu s$ to define prefiltering and the single-sample ENC , corresponding to a bandwidth of 1MHz. This bandwidth requires a sampling frequency of 2 megasamples/second to avoid noise aliasing.

Input transistor: The best one can reasonably achieve with JFETs at 300K for external (warm) readout and with PMOS at 90K for electronic readout in the cryostat is $e_n = 0.5\text{nV}/\text{Hz}^{1/2}$, which corresponds to a resistance $R_{sn}=15\text{ohms}$. Trying to reduce these values further for warm electronics would bring a diminishing return as the resistance values of the signal cables are approached (~a few ohms). For cold electronics, power dissipation limits any further reduction in the noise.

With these assumptions, three different plots of ENC vs sense wire length and signal cable length are given in Figs. 4, 5 and 6, to cover the likely range of parameters to be encountered in a very large TPC, for either external (warm) or internal (cold) electronics.

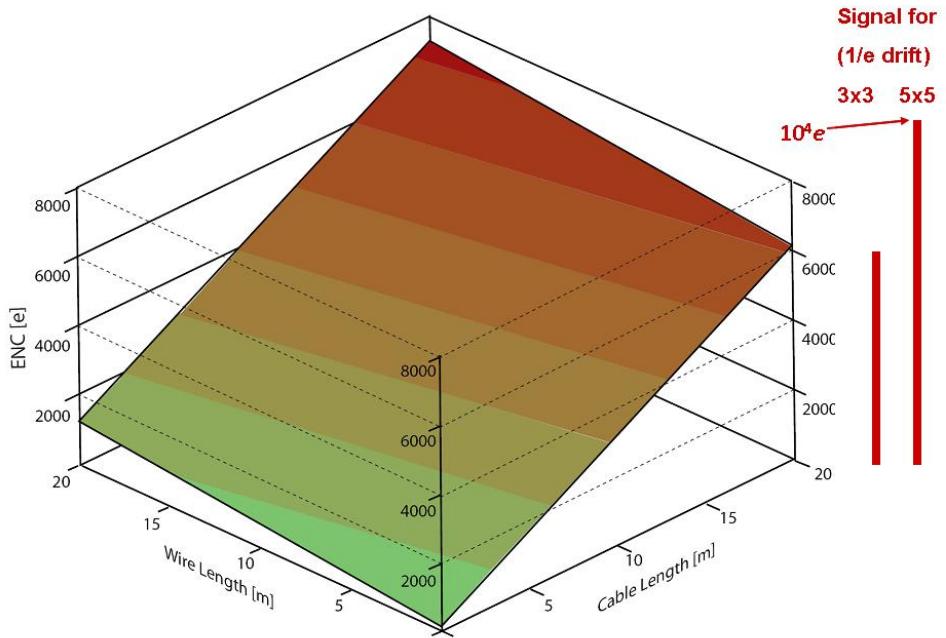


Fig. 4. Contour plot of equivalent noise charge (ENC) vs sense wire length and signal cable length due to amplifier noise with a spectral density of $0.5\text{nV}/\text{Hz}^{1/2}$ and weighting function peaking time $t_p=1\mu\text{s}$. Sense wire capacitance is $\sim 20\text{pF/m}$ and signal cable capacitance is $\sim 100\text{pF/m}$. Note that for cold electronics, the cable length is zero.

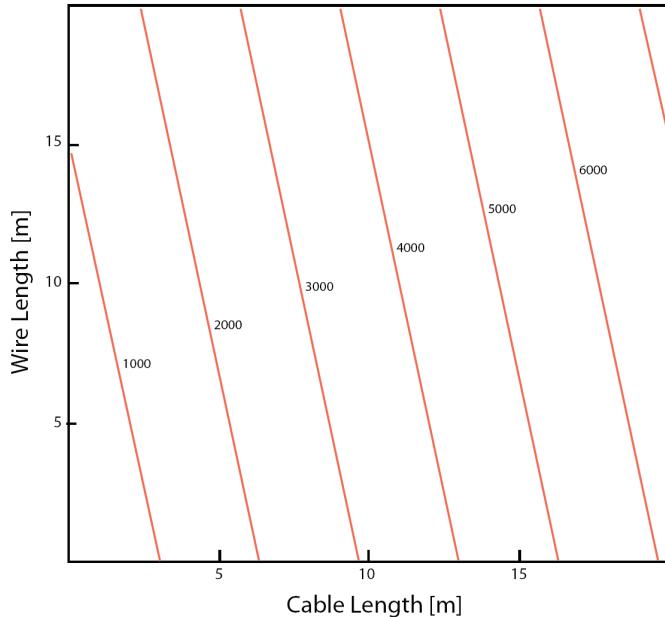


Fig. 5. A plot of constant equivalent noise charge (ENC) vs sense wire length and signal cable length due to amplifier noise with a spectral density of $0.5\text{nV}/\text{Hz}^{1/2}$ and weighting function peaking time $t_p=1\mu\text{s}$. Sense wire capacitance is $\sim 20\text{pF/m}$ and signal cable capacitance is $\sim 100\text{pF/m}$.

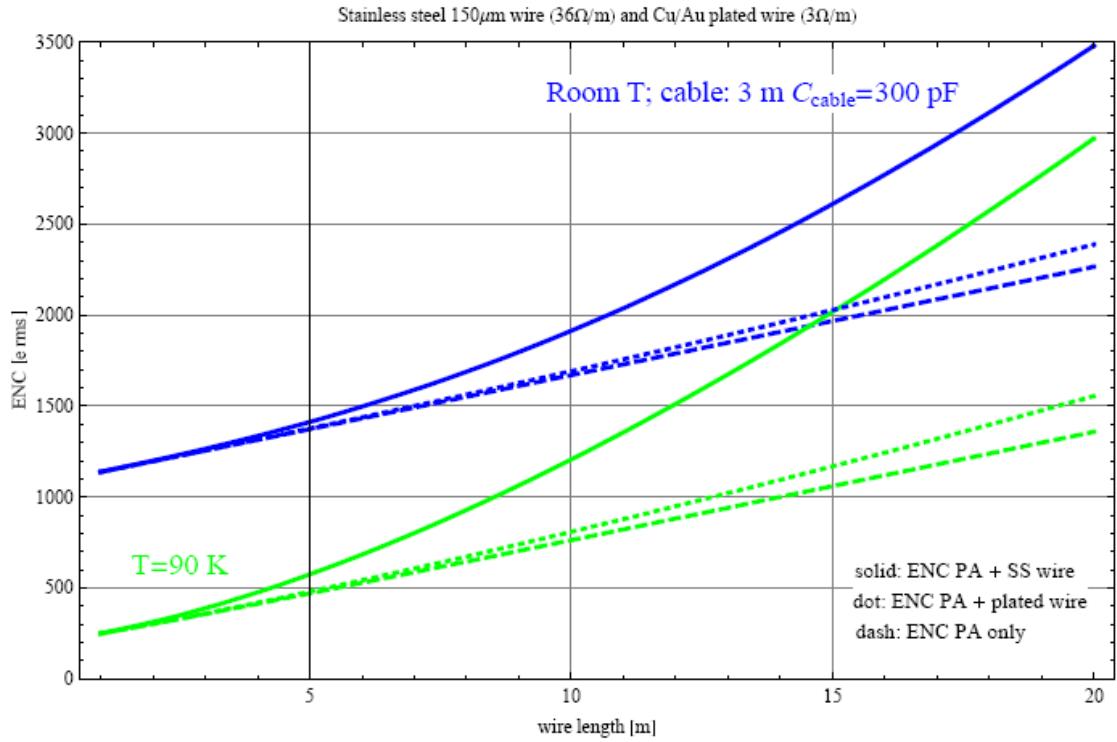


Fig. 6. This plot illustrates the performance expected with internal (cold) CMOS electronics in comparison to the external (warm) electronics. For calculation purposes, the warm electronics is assumed to have, in the best case, a 3 meter cable. The cold electronics has no cable (only a few cm long connections from the sense wires to the ASIC). Shown is ENC vs sense wire length due to amplifier noise with a spectral density of $0.5\text{nV}/\text{Hz}^{1/2}$ for different sense wire materials and weighting function peaking time $t_p=1\mu\text{s}$. Sense wire capacitance is $\sim 20\text{pF}/\text{m}$ and signal cable capacitance is $\sim 100\text{pF}/\text{m}$. For longer wire lengths, low resistance sense wire (such as Cu+Au plated SS wire) offers a significantly lower noise.

4. Signal to noise estimates:

Collection plane S/N for cold electronics with stainless steel wire, 36 ohm/m						
		wire spacing >	3	4	5	
Wire length	Noise	Signal >	6000	8000	10000	
5	550	S/N >	10.9	14.5	18.2	
10	1100	S/N >	5.45	7.2	9.1	
15	1900	S/N >	3.15	4.2	5.3	
20	2900	S/N >	2.1	2.8	3.4	

Collection plane S/N for cold electronics with low resistance (copper+gold plated) wire, 3 ohm/m						
		wire spacing >	3	4	5	
Wire length	Noise	Signal >	6000	8000	10000	
5	500	S/N >	12	16	20	
10	650	S/N >	9.2	12.3	15.3	
15	800	S/N >	7.5	10	12.5	
20	1000	S/N >	6	8	10	

Collection plane S/N for warm electronics (+3m cable) with stainless steel wire, 36 ohm/m						
		wire spacing >	3	4	5	
Wire length	Noise	Signal >	6000	8000	10000	
5	1550	S/N >	3.8	5.2	6.5	
10	2050	S/N >	2.9	3.9	4.9	
15	2750	S/N >	2.2	2.9	3.6	
20	3800	S/N >	1.6	2.1	2.6	

Collection plane S/N for warm electronics (+3m cable) with low resistance (copper+gold plated) wire, 3 ohm/m						
		wire spacing >	3	4	5	
Wire length	Noise	Signal >	6000	8000	10000	
5	1500	S/N >	4	5.3	6.7	
10	1750	S/N >	3.4	4.6	5.7	
15	2150	S/N >	2.8	3.7	4.7	
20	2450	S/N >	2.4	3.3	4.1	

The above S/N calculations used 3 meter cables for connecting the warm electronics to the collection wires. This is the most optimistic assumption for warm electronics. In a large TPC the S/N ratio for warm electronics will be considerably worse than shown above, particularly for the U, V signal wires near the bottom of the detector due to much long cable lengths. It should also be noted that the signal to noise ratio will be lower than shown above (at the collection plane) for both warm and cold electronics on the U and V induction planes due to smaller signals.

5. Number of Wires (signal channels) in Large TPC Detectors

5.1. Lower limit: If we assume the sense wire length of 10 meters, the electron drift distance of 2.5 meters and the sense wire spacing 5mm x 5 mm, the number of sense wires (and readout channels) for a 3-coordinate readout will be ~18/ton in a large module.

5.2. Upper limit: Sense wire length = 5 meters, electron drift distance= 2.5 meters, sense wire spacing, 3mm x 3 mm, the number of sense wires (and readout channels) for a 3-coordinate readout will be ~60/ton in a large module.

5.3. A possible intermediate case: Sense wire length = 5 meters, electron drift distance= 2.5 meters, sense wire spacing, 5mm x 5 mm, the number of sense wires (and readout channels) for a 3-coordinate readout will be ~36/ton in a large module.

6. Scaling in Size of the LAr TPC and Signal Cable Lengths with “Warm” and “Cold” Electronics

Cryostat Design: “Warm” vs “Cold” Electronics

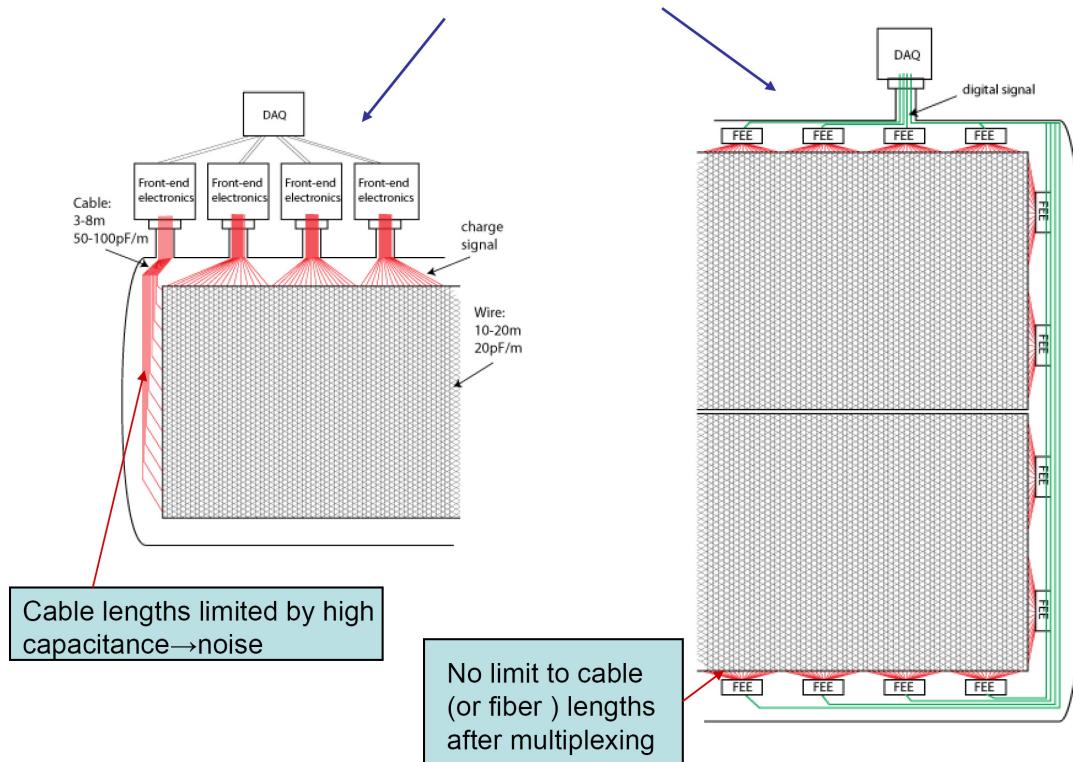


Fig. 7. An illustration of cable lengths for readout with warm and cold electronics. With external (“warm”) electronics, signal cable lengths $>10\text{-}20$ meters are needed for detector fiducial volumes $>1\text{ kton}$ resulting in high capacitance and high noise. Cold electronics decouples the electrode and cryostat design from the readout design. Thus it provides freedom in the design and location of the wire electrode modules, as well as in the choice of the form of the cryostat.

7. Internal (“cold”) electronics

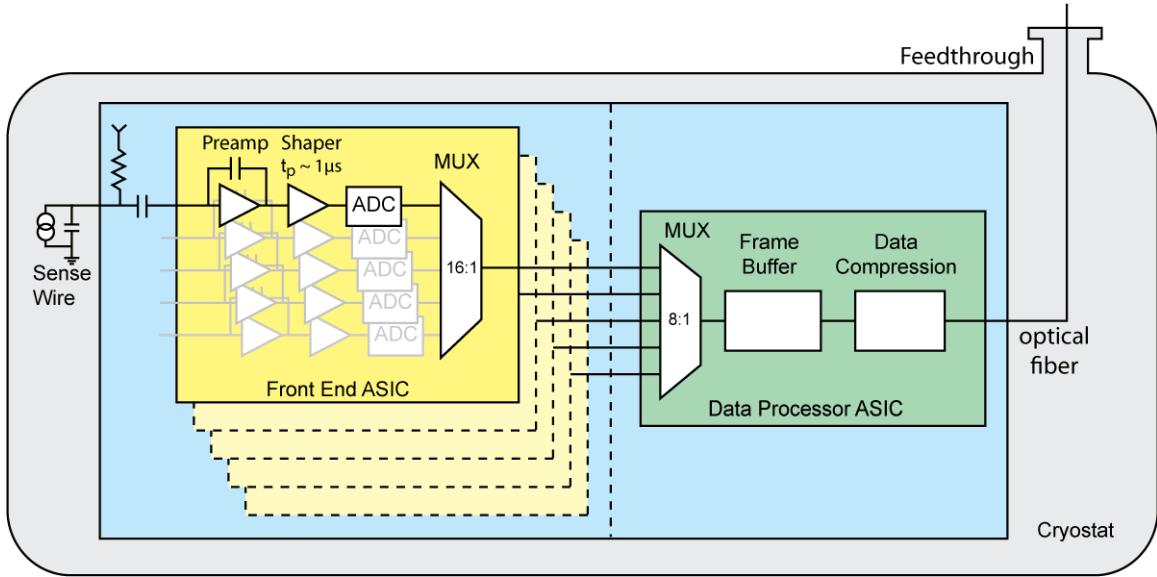


Fig. 8. A Functional Outline of a Multiplexed Readout Chain for Very Large LAr TPCs. Multiplexing will be performed in two steps at appropriate locations within the cryostat. A CMOS, or a BiCMOS technology with circuit design and operating conditions for long term operation in LAr will be used. A preliminary goal is multiplexing in two steps by $16 \times 8 = 128$. Power dissipation has been estimated to be $\leq 10\text{mW}/\text{signal wire}$.

7. Concluding Technical Remarks

- For detector fiducial volume $> 1\text{kt}$ signal cable lengths of $> 10\text{-}20$ meters will be required due to the cryostat size to bring the signals from the sense wires to the feedthroughs (and external warm electronics) resulting in high capacitance and high noise. (The feedthroughs will have to be located on top of the cryostat to minimize the heat input and to simplify the construction of the cryostat.)
- Cold electronics will make possible to decouple the electrode and cryostat design from the readout design (no limit on the cable length within the cryostat after the signals are amplified and digitized at the sense wires), so that ***the noise will be independent of the fiducial volume and much lower than with the warm electronics.***
- Signal multiplexing within the cryostat will result in a large reduction in the number of feedthroughs/penetrations, an important cryostat design consideration.

8. R&D Plan

Over the last few years there have been numerous publications discussing the operation of CMOS and BiCMOS circuits at cryogenic temperatures. In many ways the performance of CMOS improves at very cold temperatures. However, it is known that the transistor models that exist at normal operating temperatures need to be modified for operation at LAr temperatures. In addition it is known that the reliability of CMOS is degraded due to hot carrier effects at cryogenic temperatures. Fortunately, new models can be developed for cryogenic operation and design techniques can be used to mitigate the reliability issue. Brookhaven and Fermilab plan to work together to develop viable circuits that perform reliably at LAr temperature. There are several parts to the R&D plan.

First, several CMOS devices from different processes will be evaluated for low frequency noise performance and hot carrier effects at LN temperature. This will be done both at Brookhaven and Fermilab. Circuit models will be developed for the most promising process(s). To help with the process evaluation and model development we plan to work with John Cressler who is a recognized authority on cold electronics and one of his students, both from Georgia Tech. Test structures have already been designed for one promising process.

Second, circuit blocks for the LAr electronics will be designed by both Brookhaven and Fermilab and assembled into a complete electronics chain using the newly developed cryogenic models. Testing of these circuits at both room temperature and LN/LAr temperatures will be done at Brookhaven, Fermilab, and possibly Georgia Tech.

We are planning to complete the above tests and evaluations well in time to have the necessary answers about the feasibility of cold electronics for the readout of very large LAr TPCs to be ready for the CD1 review.