



The Run IIb CDF Detector Upgrade Project

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Background

- The CDF Run IIb project exists to keep the experiment vital during high luminosity operation.
- Originally, the project was motivated by both high integrated and instantaneous luminosity - beyond the Run II specifications.
 - Reduced integrated luminosity projections reduced the motivation for the silicon detector, resulting in its cancellation.
- Design goal instantaneous luminosity projections are still $\sim 3 \times 10^{32} \text{cm}^{-2} \text{s}^{-1}$
 - Now at 396 ns crossing – higher occupancies than planned
- Portions of the project motivated by instantaneous luminosity are still needed and have been retained



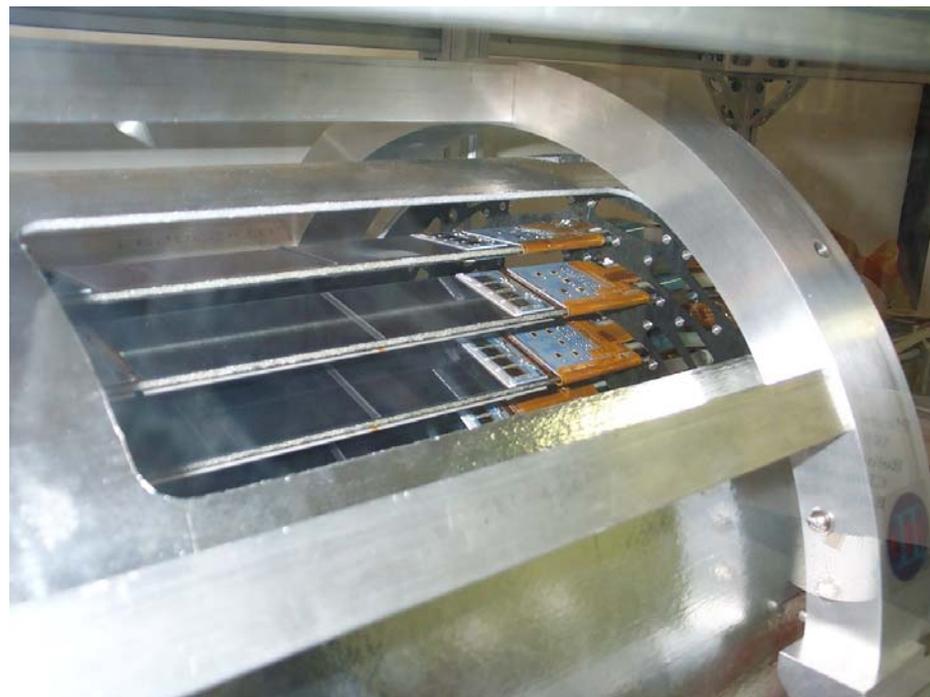
Run IIb Project Scope

- Silicon Detector Replacement
- Calorimeter Upgrades
 - Preshower Upgrade
 - Electromagnetic Timing
- Data Acquisition and Trigger Upgrades
 - TDCs for the drift chamber
 - Level 2 Decision crate
 - Fast track trigger Upgrade
 - Event Builder Upgrade
 - Level 3 computer upgrade
 - Silicon Vertex Trigger upgrade



Silicon Detector Replacement

- Originally planned because the radiation damage lifetime of the current silicon detector was thought to be $\sim 4 \text{ fb}^{-1}$.
 - Run IIb spec. was 15 fb^{-1} .
- New detector was much more rad. hard, optimized for high occupancy.
- Production was cancelled in Sep. 2003.



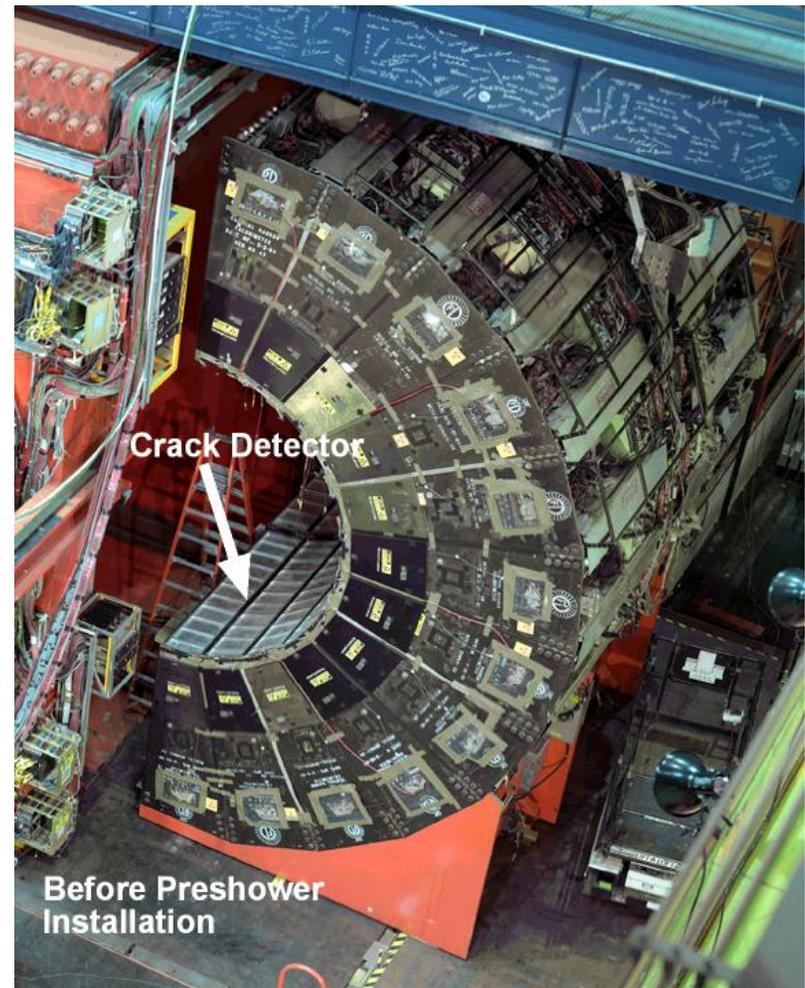
- 7% of the staves were built
- One $\sim 15^\circ$ section assembled and operated



Preshower / Crack Detectors

- The preshower upgrade replaces the older gas chamber system with scintillator.
 - Last accessible piece of gas calorimetry
 - Fiber/multichannel PMT readout – similar to what's used on the endplug.
- Significant foreign contribution here
 - PMT from Japan
 - Scintillator/fibers from Italy

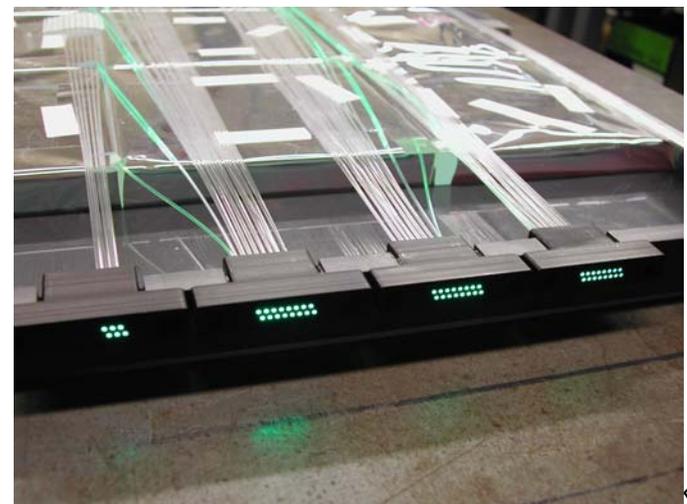
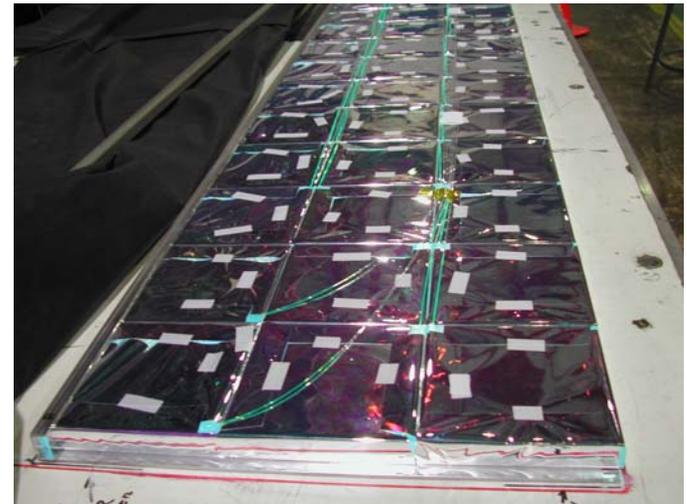
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Preshower Upgrade

- System was planned for an assembly hall installation in FY 2006 (silicon shutdown)
- Schedule was adapted to accommodate accelerator shutdowns
 - Accelerated production of scintillator tiles, modules
 - Procurement of PMTs by Tsukuba was advanced
 - The project targeted Fall 2004





Calorimeter Installation

- Preshower installation involved detector installation on the inner surface of the calorimeter
 - Never serviced in the collision hall previously.
- Phototube and cables are located on the back.
- System installation was completed in Nov., 2004.



- All scaffolds, detector elements, people, passed through this opening.



Preshower / Crack Installation



Stefano Moccia

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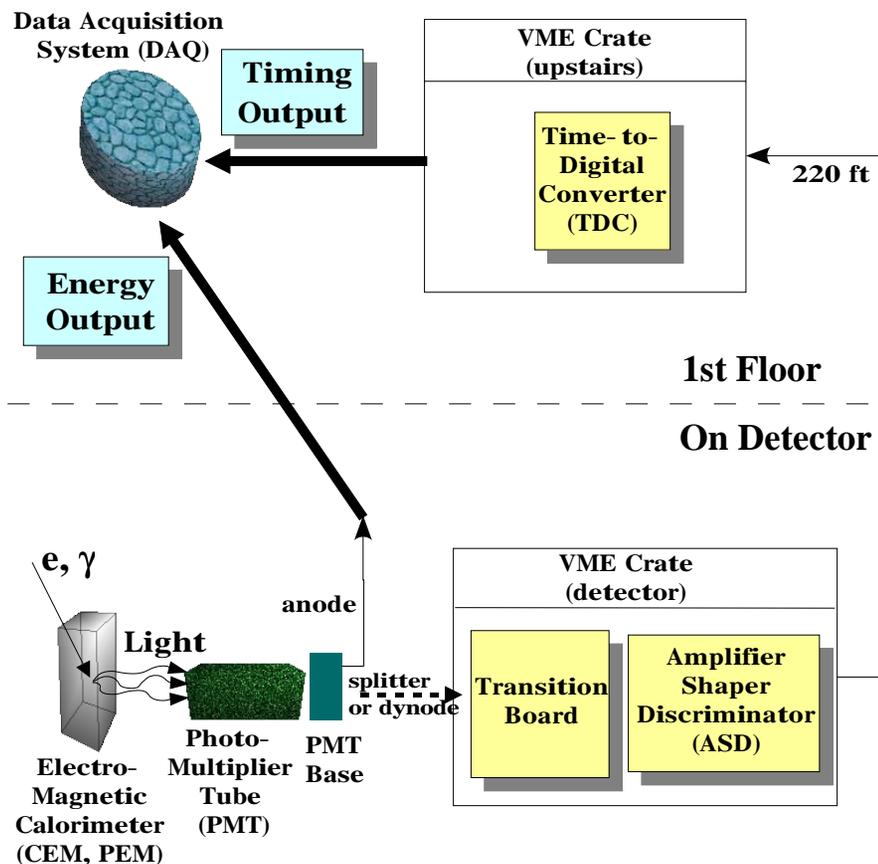


EM Timing

- The electromagnetic timing upgrade splits a small portion of the phototube signal off for timing
 - Reduces cosmic ray or halo backgrounds for photons
- Entire system was installed during the fall 2004 shutdown.
- Has been included in the data since that time
 - (FERMILAB-PUB-05-54 3-E)

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CDF EM Timing Project





DAQ/Trigger Specification

Run IIa vs IIb

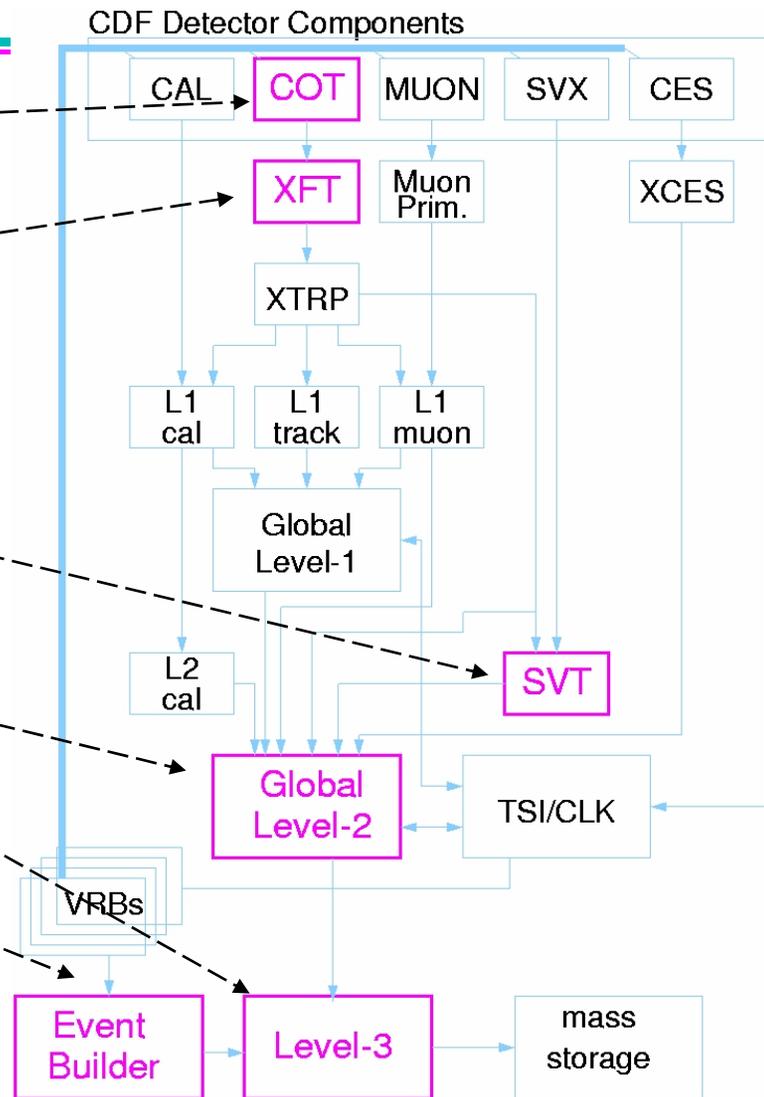
	Run IIa Specification	Run II (2004) Achieved	Run IIb Specification
Luminosity	8.6×10^{31}	1×10^{32}	3×10^{32}
L1 Accept	45 kHz	25 kHz	30 kHz
L2 Accept	300 Hz	400 Hz	1000 Hz
Event Builder	75 MB/s	75 MB/s	500 MB/s
L3 Accept	75 Hz	80 Hz	100 Hz
Rate to Storage	20 MB/s	20 MB/s	40 MB/s
Deadtime Trigger	5%	10%	5% + 5% Δ

- Run IIb bandwidth needs are based on projections for the high P_T program only. B physics trigger are dropped for these purposes.
- † Assume ~5% from readout and ~5% from L2 processing
- Reminder: IIb trigger & bandwidth rates estimated based upon Run IIa, significant underestimate possible (assumes linear growth in fake contribution)



Trigger/DAQ Upgrades for Run IIb

- COT TDC upgrade
 - Original readout rate insufficient
- COT Track Trigger Upgrade
 - L1 trigger rate reduction needed
 - Complexity of events (occupancy)
- Silicon Vertex Trigger upgrade
 - Occupancy demands processing speed
- L2/L3 trigger upgrades
 - Processing speed/modernization
- Event builder upgrade
 - Processing speed upgrade needed
 - Level 2 accept rate is insufficient

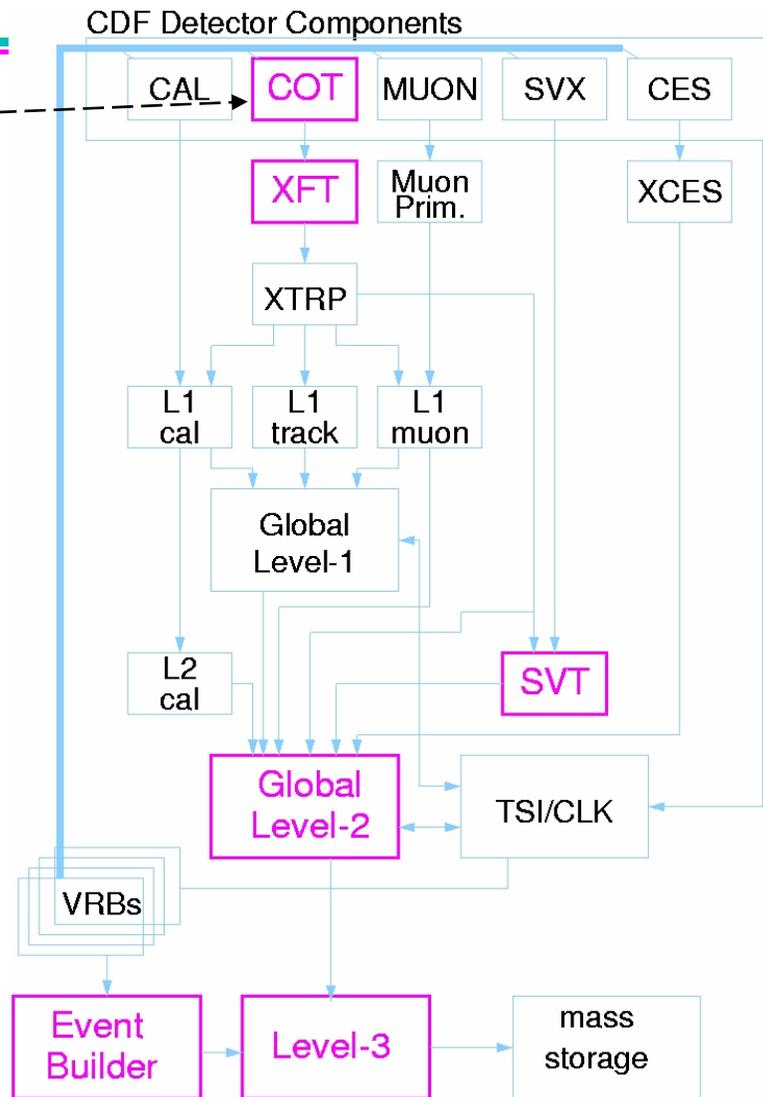




Trigger/DAQ Upgrades for Run IIb

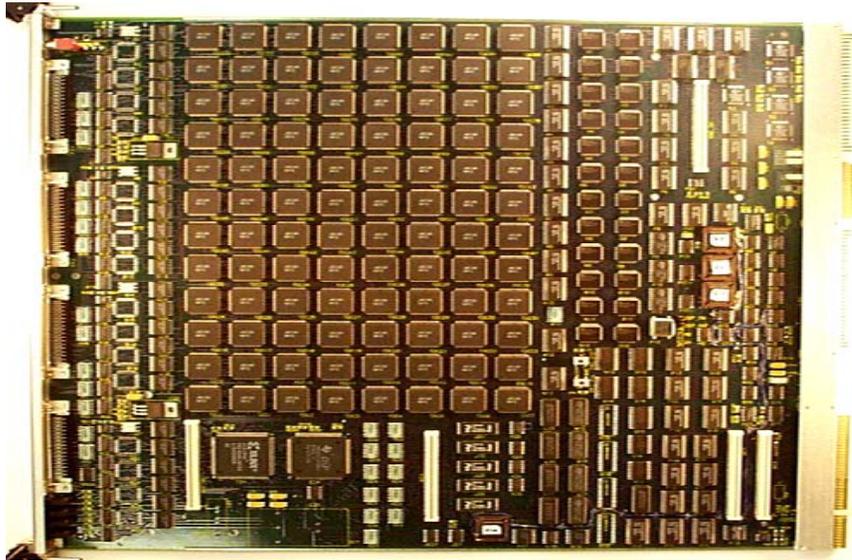
- COT TDC upgrade
 - Original readout rate insufficient
- On-board processing (DSP) Time grows with # of hits
 - $t = 1200\mu\text{s/event}$ for SL1 (4 hits/ch) at $4 \times 10^{32} \text{ cm}^{-2}\text{s}^{-1}$
- VME Readout
 - Read sequentially by one block transfer (~14MB/s at high lum.)
- VME – Event builder link limited to 12 MB/s
- 2002 Internal review recommended replacement

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TDC Replacement



- CDF Run II, 96 channel TDC

- Run IIb TDC
- Far fewer components, functions all within an FPGA





TDC Performance Reviews

- Run 2b TDC
 - 5 preproduction boards received in Sept., 2004 pass tests
 - Implemented 64 bit VME transfer (was 32bit like rest of FE/Trig)
 - In bench tests 18MB/s (32bit VME) → 36MB/s
 - Can achieve 2kHz with less than 5% deadtime
 - **Exceeds all Run 2b specifications (NIM, A554:444-457, 2005)**
- However, from our Prod. Readiness Review –
 - “Commissioning would be smoother if the older TDCs were programmed to have the same data format as the newer ones.”
 - “Yeah, but wouldn’t that make them faster?”



TDC Modifications

- After much hard work at night and on weekends by the Tevatron Department Head:
 - DSP execution now about factor of 2 faster than in 2002
 - New compressed data format (based in Run 2b TDC), halves the data volume.
 - Measured performance with 3 hits/channel of 5% deadtime at 1kHz
 - Need to implement Fast Clear on TDCs in SL5,6 (already on SL1-4) to keep these from taking longer than SL1
 - This is a hardware modification to the existing boards
 - **Meets the Run 2b readout specification**



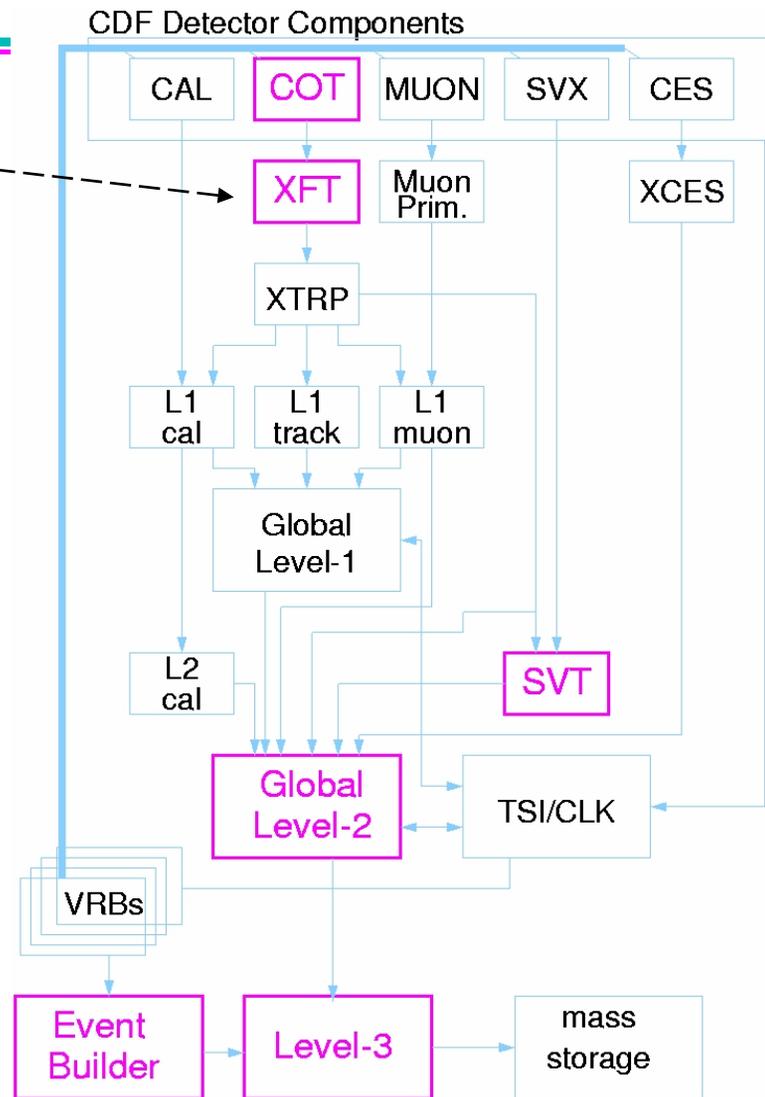
New TDC Strategy

- The decision was made to retain the current TDCs for the remainder of the run
- Modifications of the current TDCs were needed (outer layer modules)
- These modifications were done in small batches throughout 2005, and were installed during access times of ~4 hours.
- Last crate was done in December.
 - The installed set is complete



The Track Trigger (XFT)

- The track trigger was designed with the expectation of ~ 1 interaction/beam crossing
- Higher instantaneous luminosities at 396 ns challenge this system with high occupancies.
 - Fake rates rise very quickly

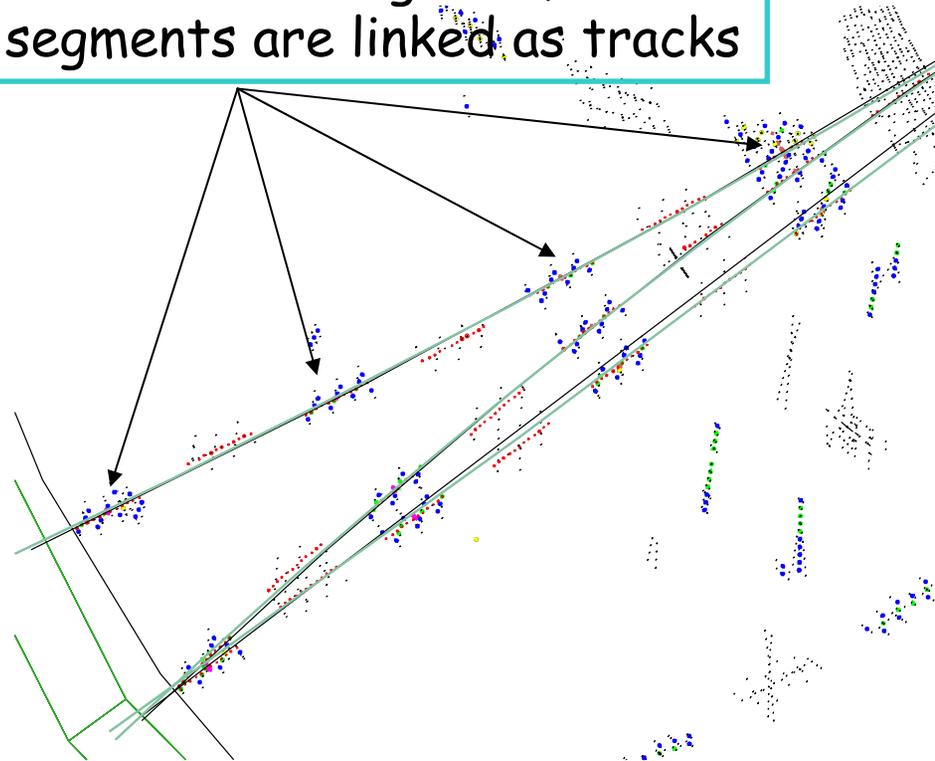




CDF Track Trigger

- Track trigger (XFT) uses the axial layers of the drift chamber to provide track information at level 1 in the trigger
- Critical to most of the CDF physics program.
- High hit occupancy in the tracking chamber creates fake trigger tracks
 - Processing time goes up

Good axial hit patterns are identified as segment, then segments are linked as tracks

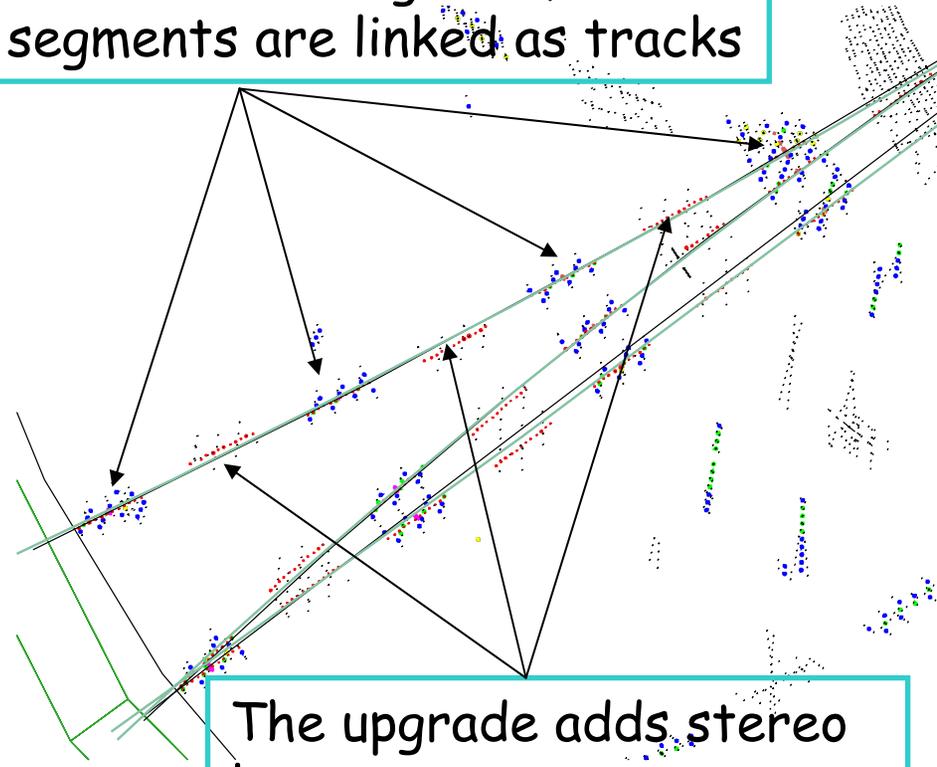




Track Trigger Upgrade

- The upgrade strategy will add information to the trigger tracks
 - Increased information provides greater selectivity
 - Rates will be reduced.
- Stereo layers will be incorporated.
- Simulations show significant improvements are possible

Good axial hit patterns are identified as segment, then segments are linked as tracks



The upgrade adds stereo layers

Missing Et
Et= 3.3 phi=3.7

List of Tracks
Id pt phi eta

Cdf Tracks: first 5

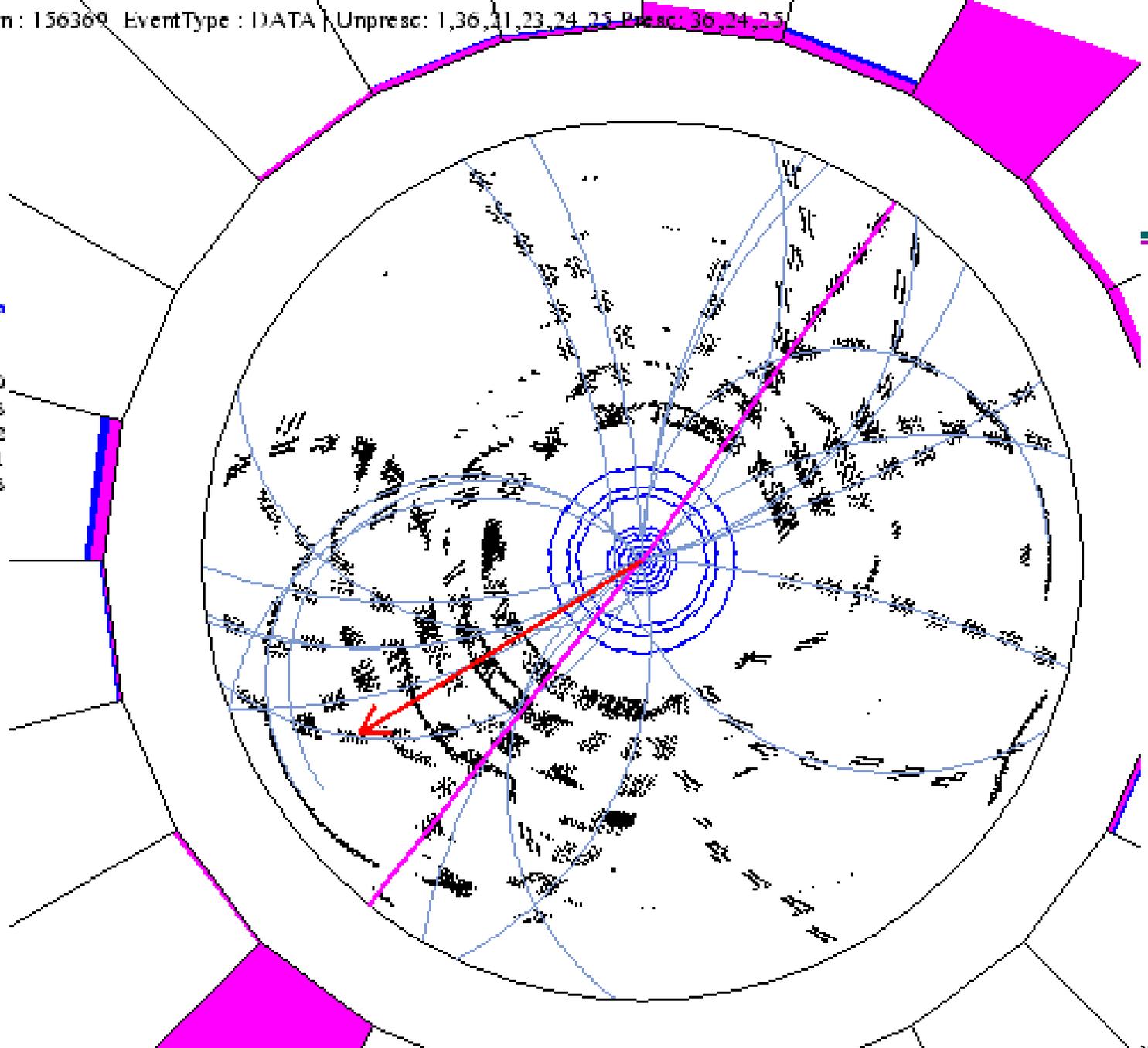
Id	pt	phi	eta
157	-45.4	-2.2	1.0
158	25.7	0.9	-0.3
147	1.2	0.3	0.2
148	-1.6	-0.1	0.1
149	1.2	1.6	-1.3

To select track type
SelectCdfTrack(Id)

Svt Tracks: first 5

Id	pt	phi	eta
0	-5.7	0.2	

To select track type
SelectSvtTrack(Id)



Missing Et
Et= 3.3 phi=3.7

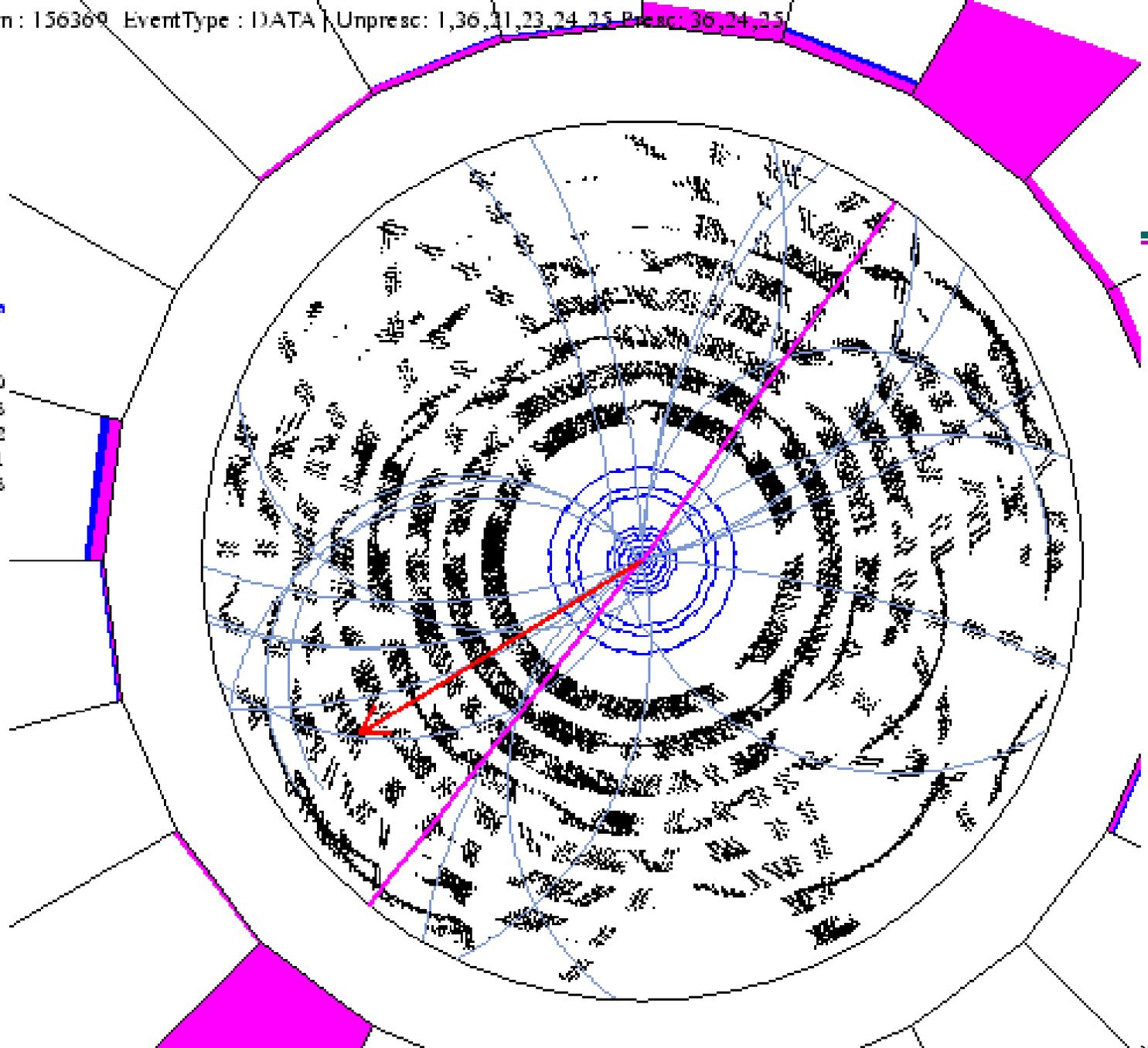
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Cdf Tracks: first 5
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158 25.7 0.9 -0.3
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148 -1.6 -0.1 0.1
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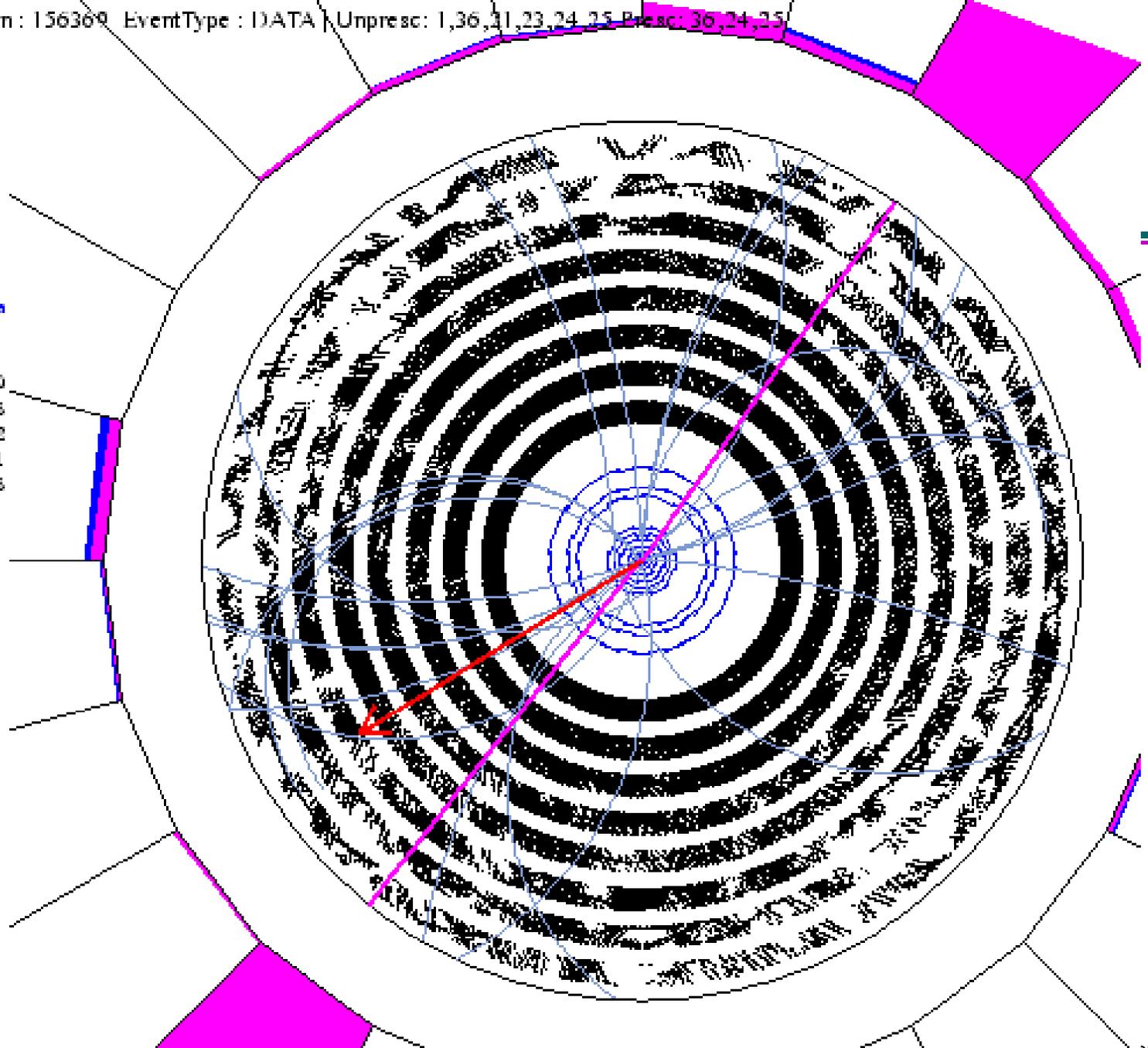
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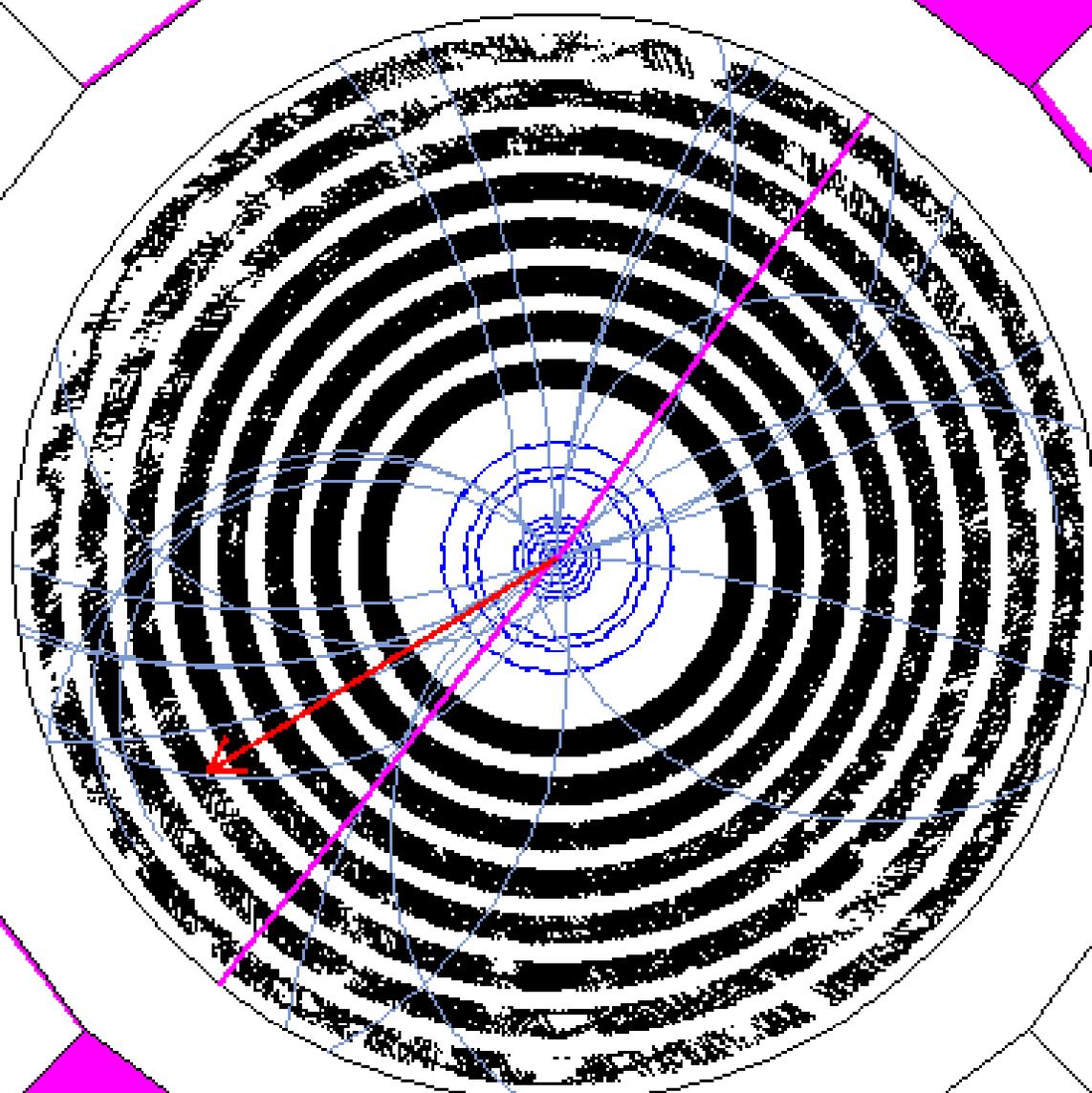
SelectCdfTrack(Id)

Svt Tracks: first 5

0	-5.7	0.2
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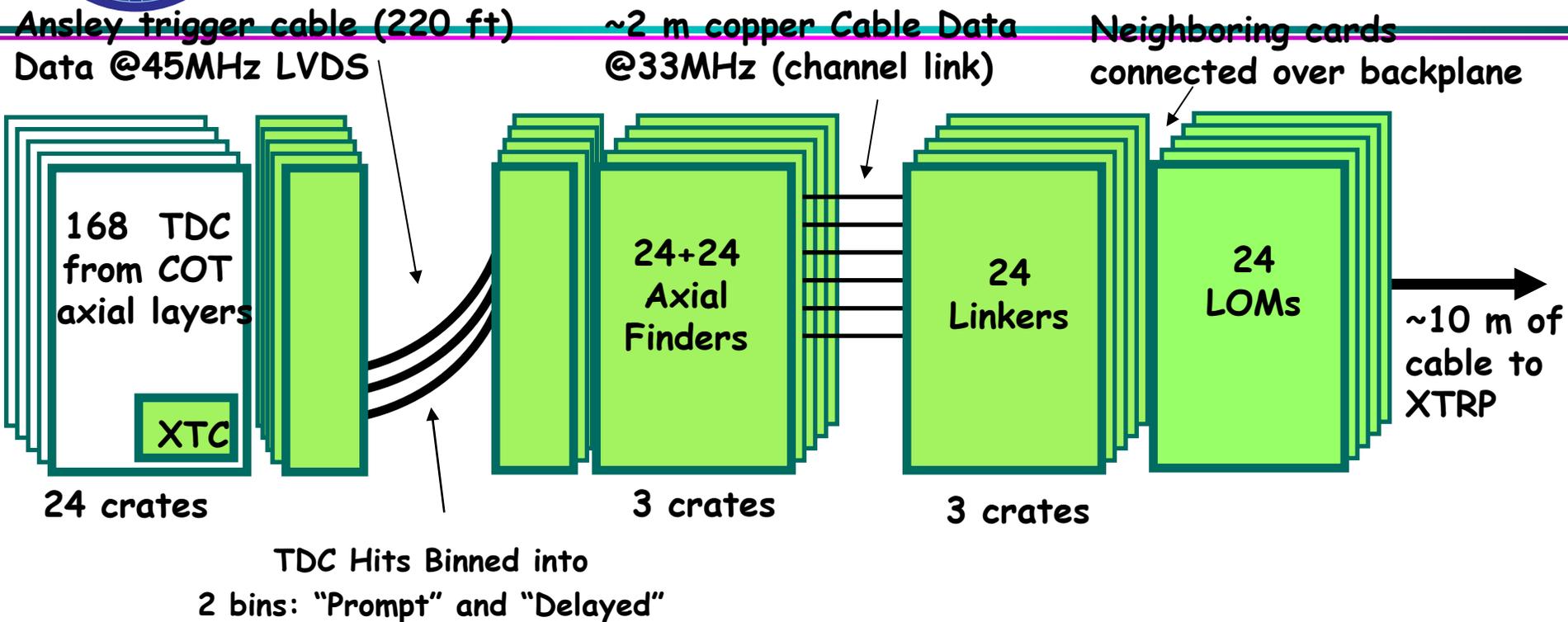
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SelectSvtTrack(Id)



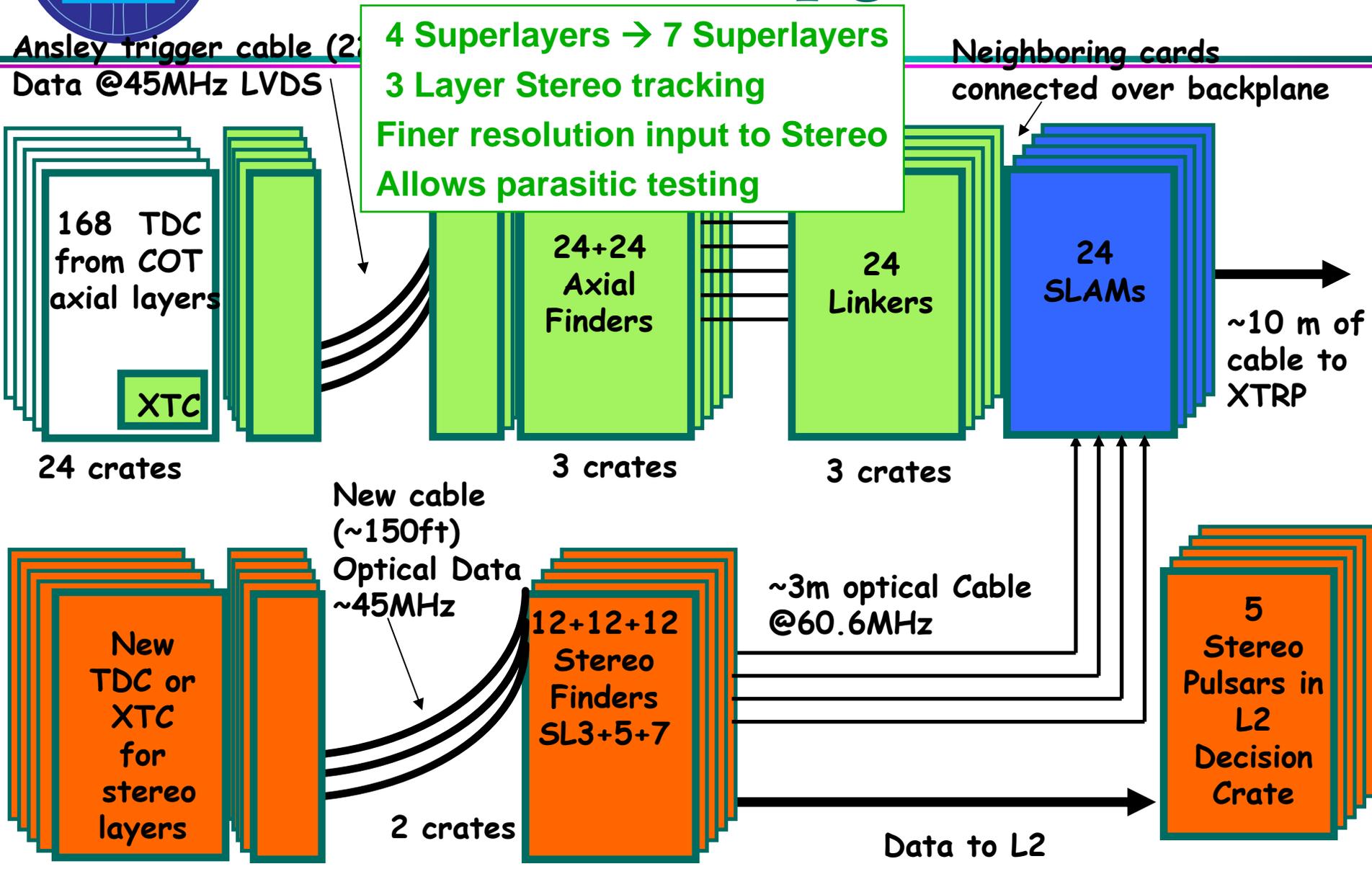


Run IIa XFT Configuration





XFT Upgrade





XFT Hardware Progress

- Collision hall installations
 - XTC2 cards – Installed with the TDC modifications
 - Transition cards and cables – Installed during the December downtime
- Trigger room installations
 - Stereo Finders installed Nov-Dec. – being commissioned
 - Stereo Linker Association Module - being commissioned
- Commissioning can be largely parasitic to operations.
 - Existing axial system will continue to run
 - Stereo upgrade will be fully operational in Summer, 2006

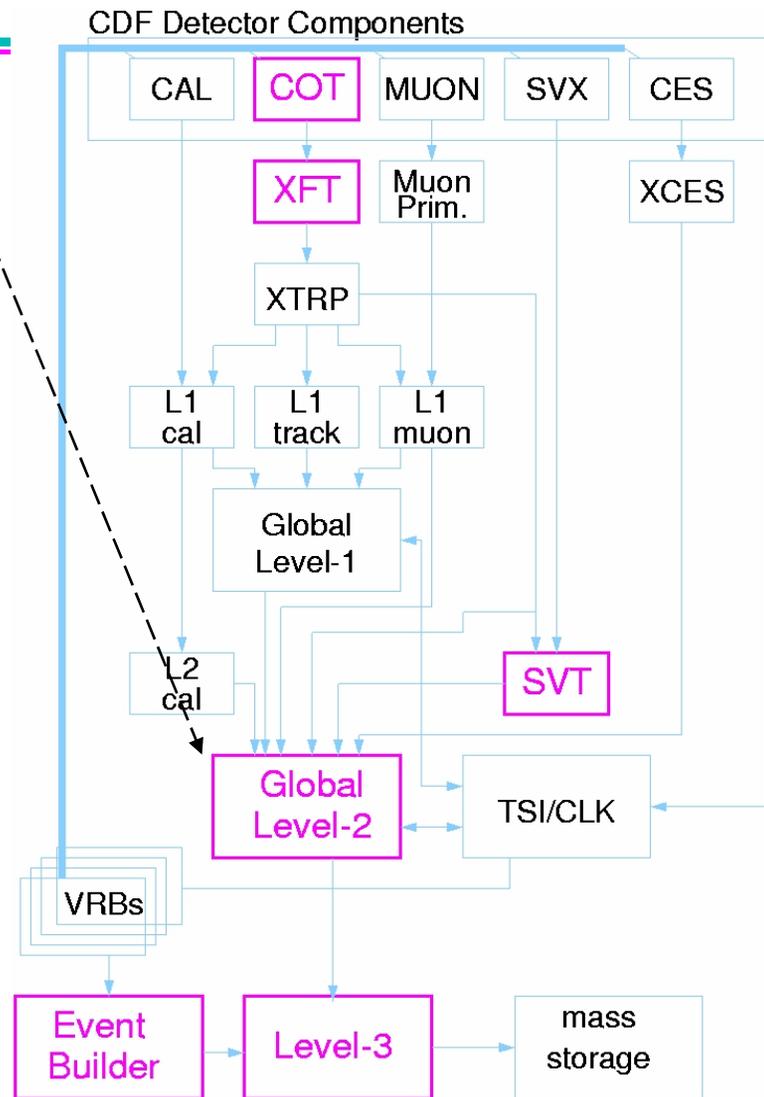


The Level 2 Decision Crate

- The Level 2 decision crate used
 - 6 different kinds of interface boards
 - Obsolete Dec α processors for the trigger decisions
- Replacement system is based on
 - Standard PCs for the trigger decisions
 - A universal interface board
 - Programmable “Pulsar”



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Level 2

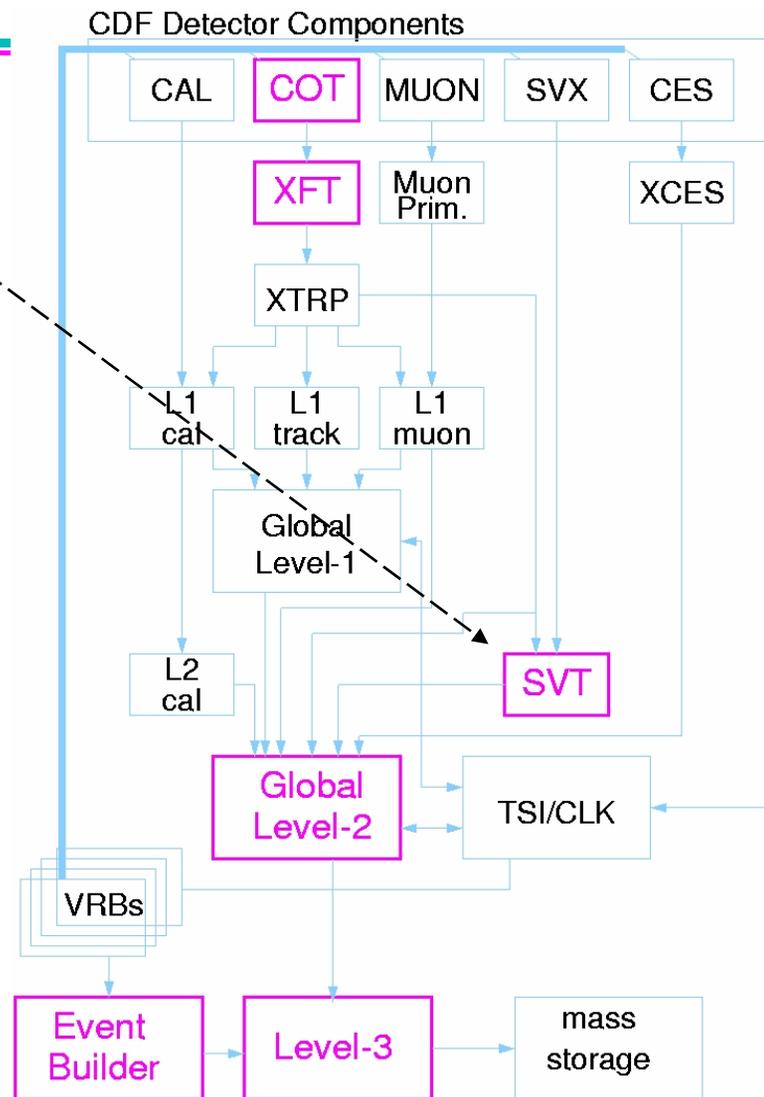
- Extensive testing with beam occurred beginning in summer, 2004
- System was phased in during the winter 2005, and is now fully installed and used in operations.
 - Older, obsolete system was been removed (May 2005).
 - Reliability improvements have already been seen
 - Decisions made with common processors, speed improvements are substantial



The Silicon Vertex Trigger (SVT)

- The Silicon Vertex Trigger has the same occupancy issues as the XFT
 - High occupancy → high fake rate
- Strategy
 - Add front end pattern memory for more patterns
 - Add processing power with Pulsar boards
 - Same hardware, different firmware

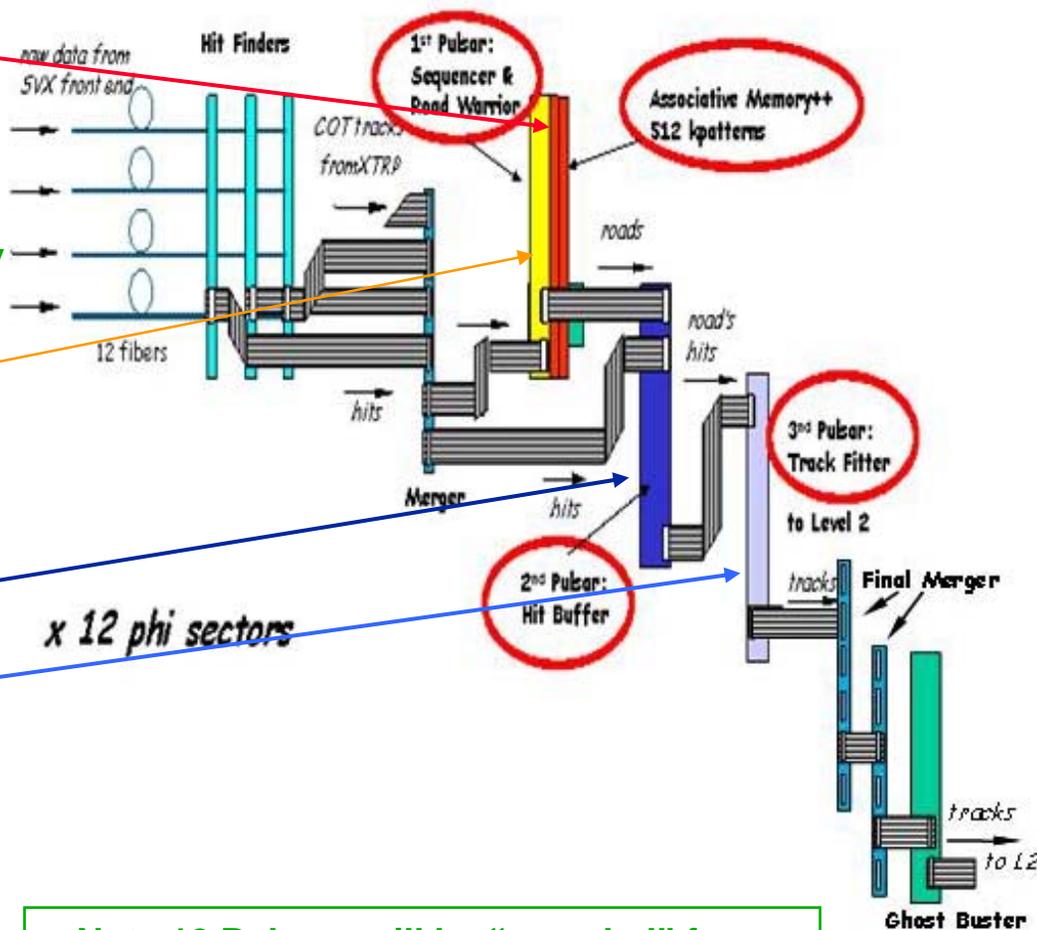
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SVT Upgrade for SVXII

- New **AM++** hardware with narrower roads (32K to 512K) reduces number of tracks to fit
 - Developed by Pisa, bought by INFN
- New **AMSequencer/Road Warrior** (12 Pulsars)
 - Interface for AM++
- New **Hit Buffer** (12 Pulsars)
- Faster **Track Fitters** reduce processing time on found roads (12 Pulsars)



Note 12 Pulsars will be “recycled” from current use as “Road Warrior” boards



SVT Progress

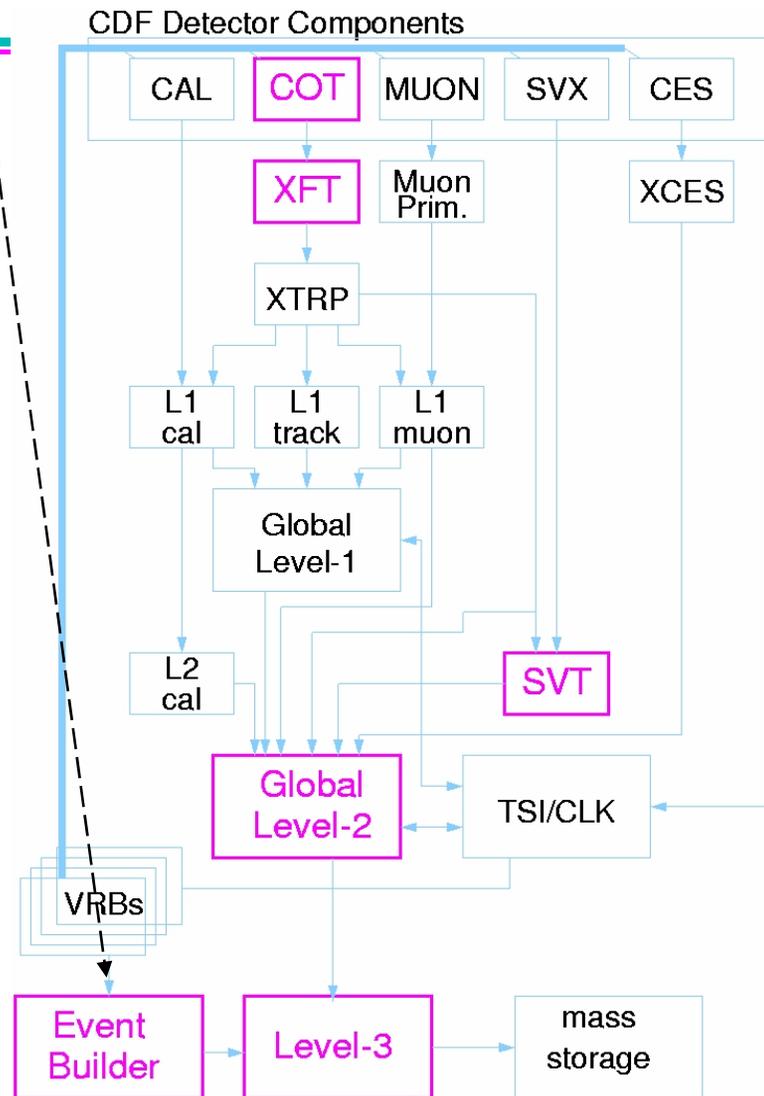
- AM++ (not on project funds) at INFN
 - AM++ and the associated mezzanine boards have been installed and in operations since Sep., 2005
 - Immediate improvement in processing time was seen.
- Hardware :
 - All Pulsar boards have been built.
 - All Pulsar mezzanine boards have been built
- Track fitter units were commissioned in the fall, fully operational in Oct., 2005.
- Hit buffer is being commissioned now.



The Event Builder

- The Event builder organizes data from the many different systems and build a single event record.
- Original system used an ATM switch, and was limited to 300 Hz.
- New system uses common ethernet, a switch commonly used at the lab.
- Commissioned in the summer, 2005. The new system went into full operations in August, 2005
- 800 Hz operations has already been achieved.

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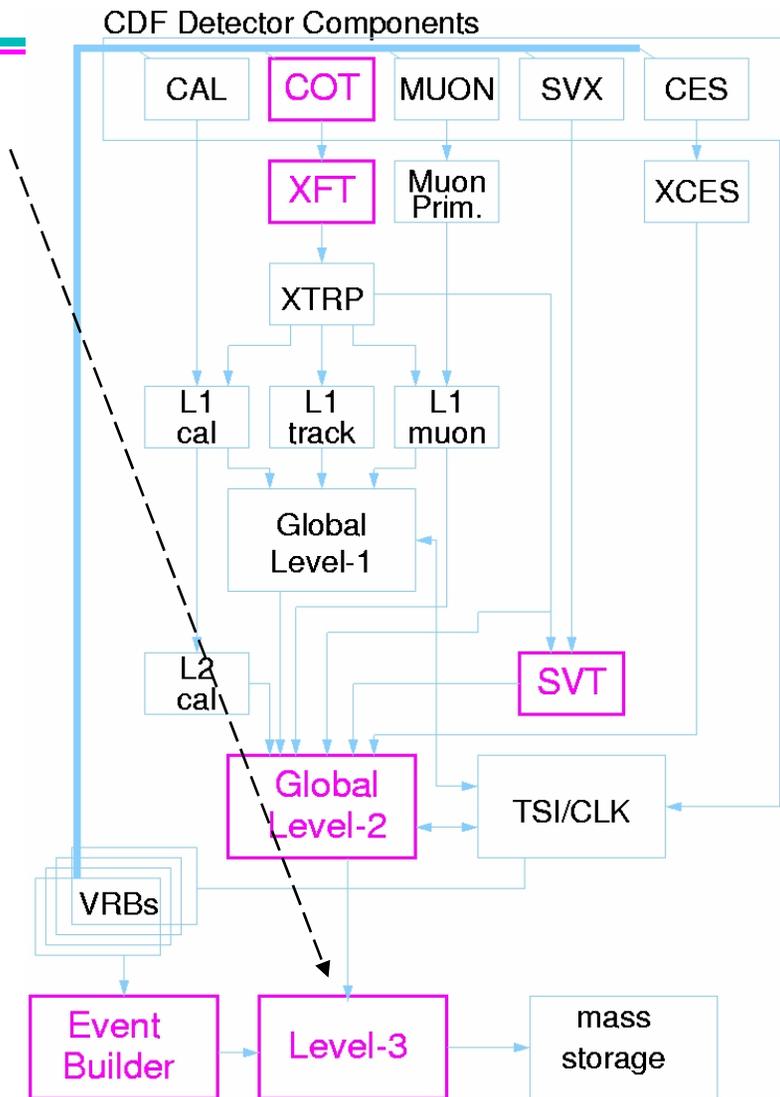


Level 3 Computing

- The Level 3 processing power has been increased to accommodate the event rate.
 - 1 THz → 2.6 THz



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CDF Upgrade Summary

- Silicon Detector
 - New design was prototyped and demonstrated
- Calorimeter
 - Both Preshower and Timing installed in Fall, 2004
- DAQ/Trigger
 - TDCs – modifications of older units is complete
 - XFT – commissioning is in progress
 - Level 2 – in operations since May, 2005
 - SVT – commissioning is in progress
 - Event Builder - in operations since August, 2005
 - Level 3 - commissioning is in progress



Project Completion

- With this, the Run IIb CDF Detector Project has met its technical baseline by its Level 1 completion Milestone, defined in its Project Execution Plan.
- We are formally able to state that we have met the schedule.
- Costs will continue for a couple of months, but the project will come in comfortably within its baseline (\$8.2M).