

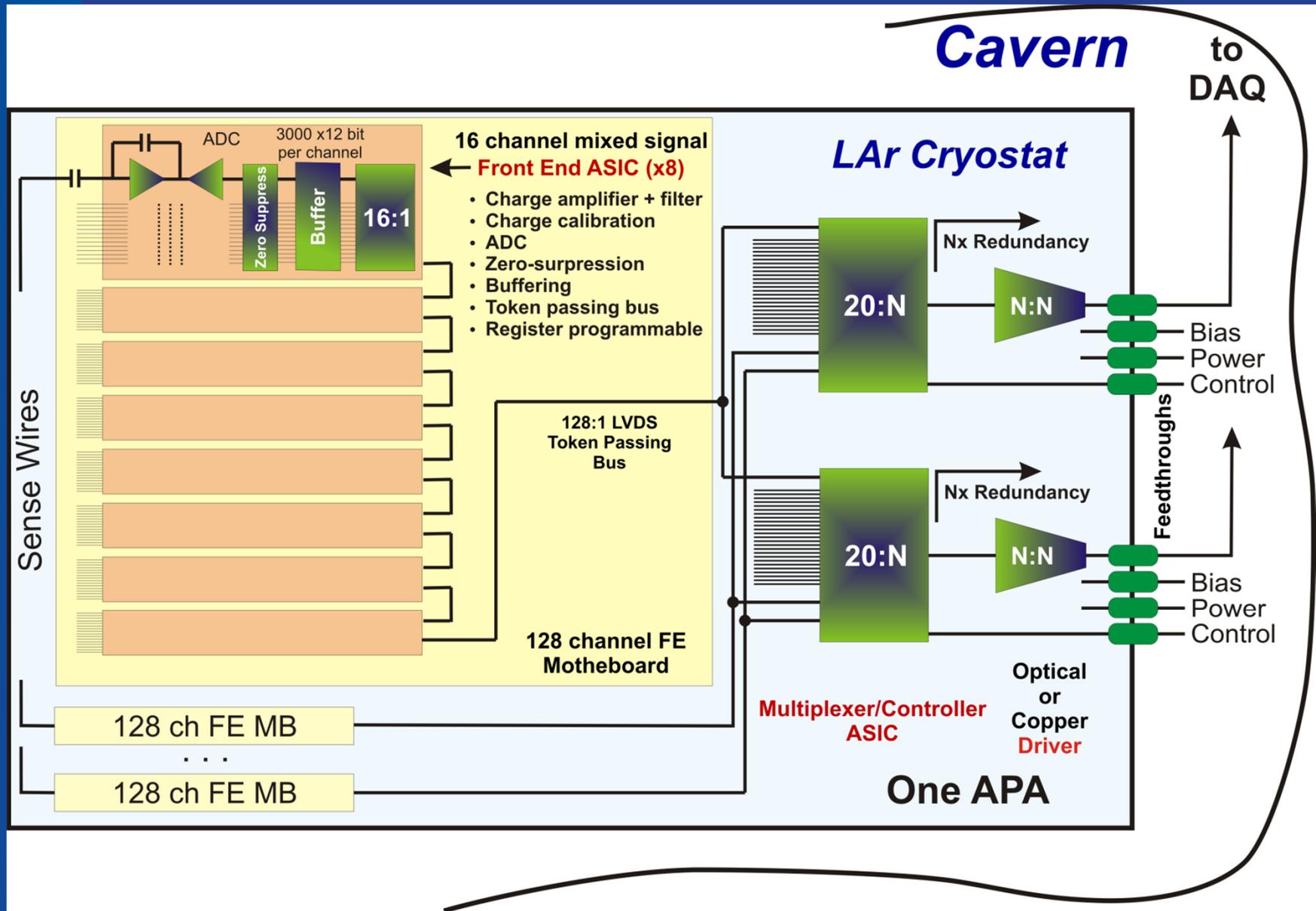
# Cold CMOS electronics for IAr TPC at LBNE

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on behalf of ASIC Development Group  
All Experiments Meeting  
March 5, 2012

# Outline

- Introduction:
  - Sketch of a concept of the readout
  - Division of responsibilities between BNL and FNAL
- Challenges and work undertaken
  - Lifetime of transistors from CMOS technologies
    - Damage mechanisms
    - Characterization of a selected process
  - Towards developing integrated readout
- Conclusion

# LAr TPC – block diagram of Cold CMOS readout



LAr40 Alternate Design (Craig Thorn BNL Far Site Review, December 6-9, 2011)

## Division of responsibilities between BNL and FNAL:

- It has been assumed:
  - **BNL** – responsible for front-end part (analog + ADC + first buffering) *relatively unconstrained and self-consistent design with well defined specification related to the source of physical signals and event  $\leftrightarrow$  data rates,*
  - **Fermilab** – responsible for digital multiplexing and transmission of data to outside of cryostat and in collaboration with Georgia-Tech. for in-cryo parts, like voltage regulators, etc. *development is strongly dependent and driven by strategic decision of the experiment, like choice of the physical transmission media, degree of combining channels into single links, strategy for delivery of power supplies, design risks to be specific, singular use, thus care is needed to elaborate and follow right set of choices with experts,*
  - **Many discussions** with arguments for and against integration of electronics for LBNE have been focused on avoidance of **risking the failure of the experiment due to aging and failure of readout circuits** (inaccessible for repair) if this option is selected.
  - Studies of degradation mechanisms and developing counter-reacting design techniques was performed in collaboration with Georgia Tech. and E. Eng. Dep. of SMU

# Lifetime/~~reliability~~ of transistors from CMOS technologies

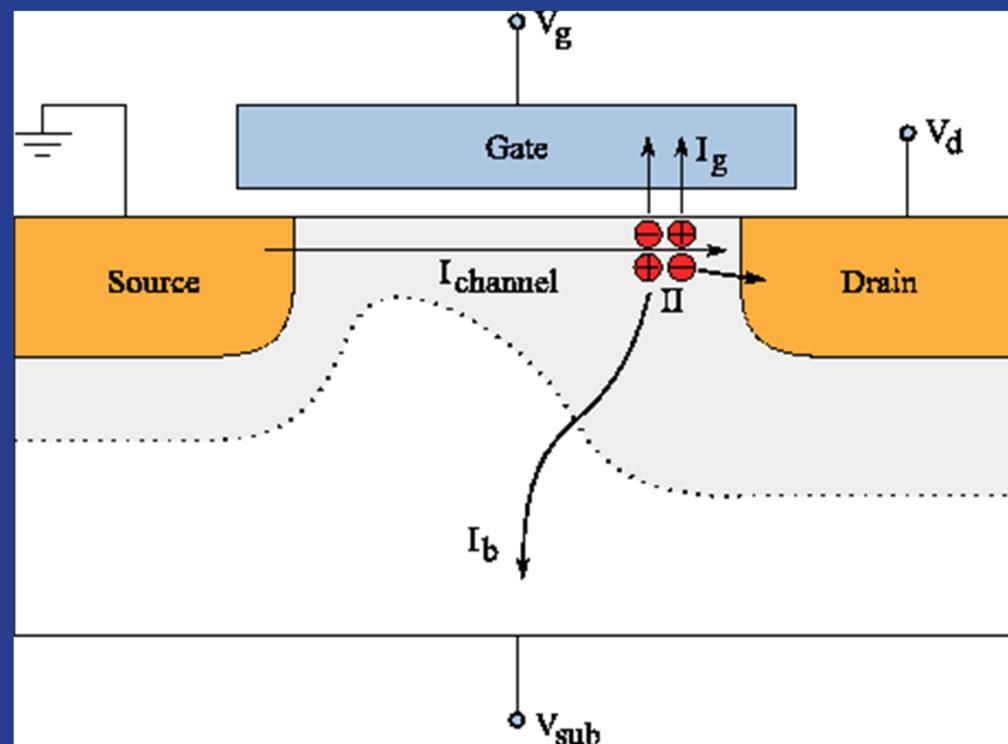
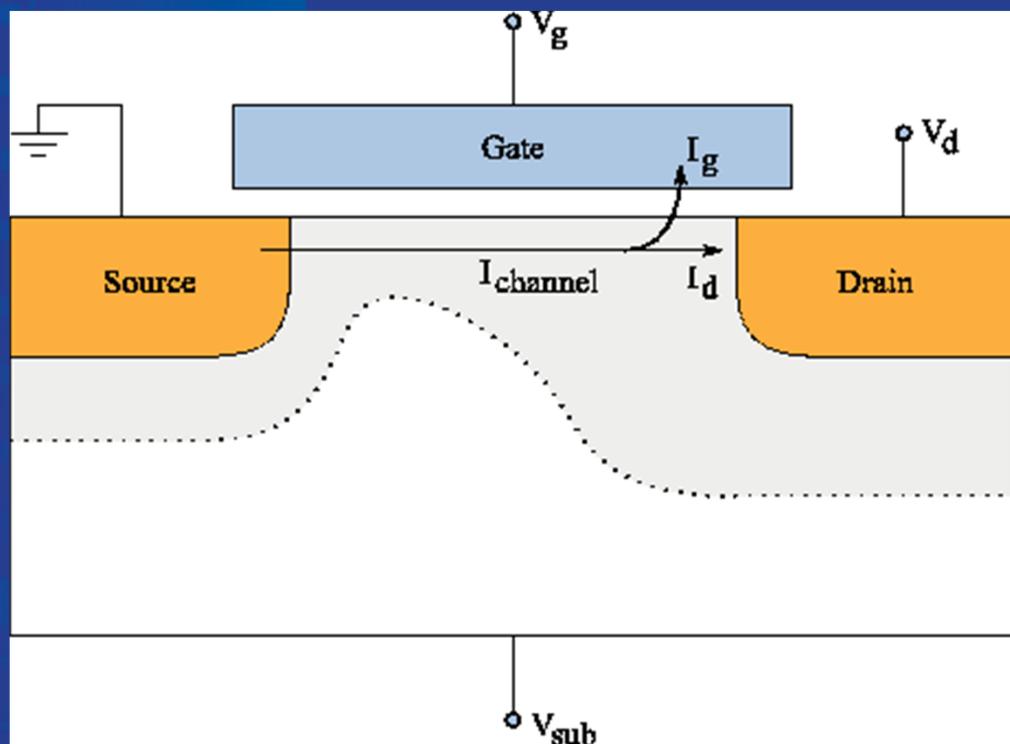
- Integrated circuits fail due to many reasons, e.g:
  - **Poor protection against electrostatic discharge**
    - During handling or use of integrated circuits (through fault of the user or not)
    - During fabrication as result of charging and flow currents in process steps using plasma for etching
  - **Poor design practice and resulting low yield**
    - Targeted parameters cannot be achieved due to designing circuits not respecting and not accommodating to statistical nature of process steps, like doping and mask misalignment (both: concept of the topology and layout)
    - Parameters of circuits change with time (aging) due to the exposure of whole circuitry, some blocks or individual transistors to conditions exceeding known maximum allowed limits (electro-migration, hot carrier degradation, ionizing radiation doses, etc. )
- Question of aging crucial for LBNE (*hot carrier induced damage*)
  - **injection of hot carriers (HC) into the dielectric: four distinguished mechanisms: channel hot-electron (CHE), drain avalanche HC (DAHC), secondary generated hot-electron (SGHE), and substrate hot-electron (SHE) – all exist at room temperature but are more intense at cryogenic temperature if nothing is done**

# Illustration of hot carrier induced damage mechanisms

## NMOS

### Channel hot electron injection

### Drain avalanche hot electron injection



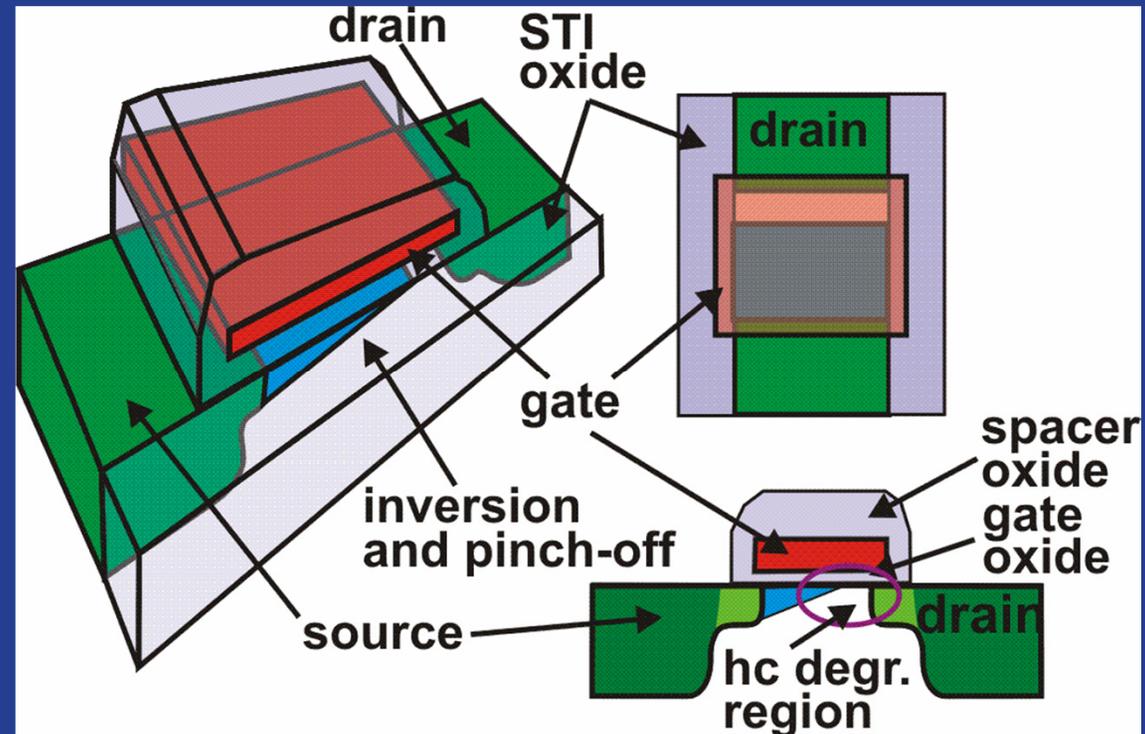
- 'lucky electrons' gain enough energy while drifting across the channel and are injected into the dielectric causing a gate current, interface and oxide degradation

- hot electrons lead to impact ionization generating electron-hole pairs; hot electrons and hot holes are injected into the dielectric. Additionally some of the carriers form a bulk current.

## Characterization of a selected process

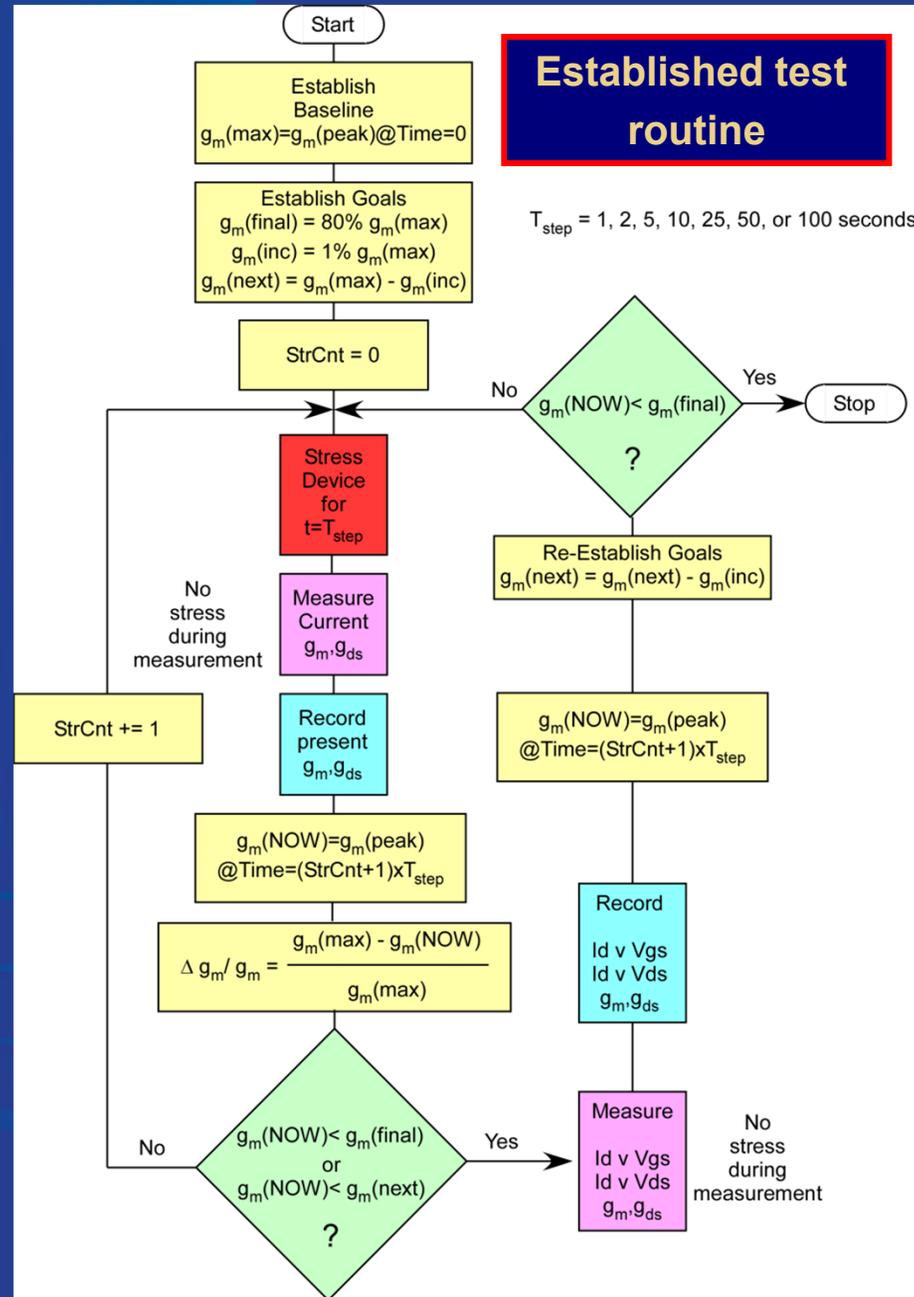
- Foundry manuals address hot-carrier effects and provide design guidelines for RoomT (sometimes in very detailed way, e.g. CMOS 9SF IBM Technology Design Manual – 90nm CMOS process):
  - reduce  $V_{DS}$
  - reduce continuous  $I_{DS}$  (mean  $I_{DS}$  in digital)
  - avoid  $L_{min}$  (very short channel devices)
- MOS transistor is a 3D structure = various material layers + numerous interfaces and the actual damage is:
  - some combination of concurrent processes
  - stress conditions dependent but principally is described by power law (t=time):

$$y = At^n$$
$$y = \frac{\Delta I_{DS}}{I_{DS0}}, \frac{\Delta V_{TH}}{V_{TH0}}, \frac{\Delta g_m}{g_{m0}}$$

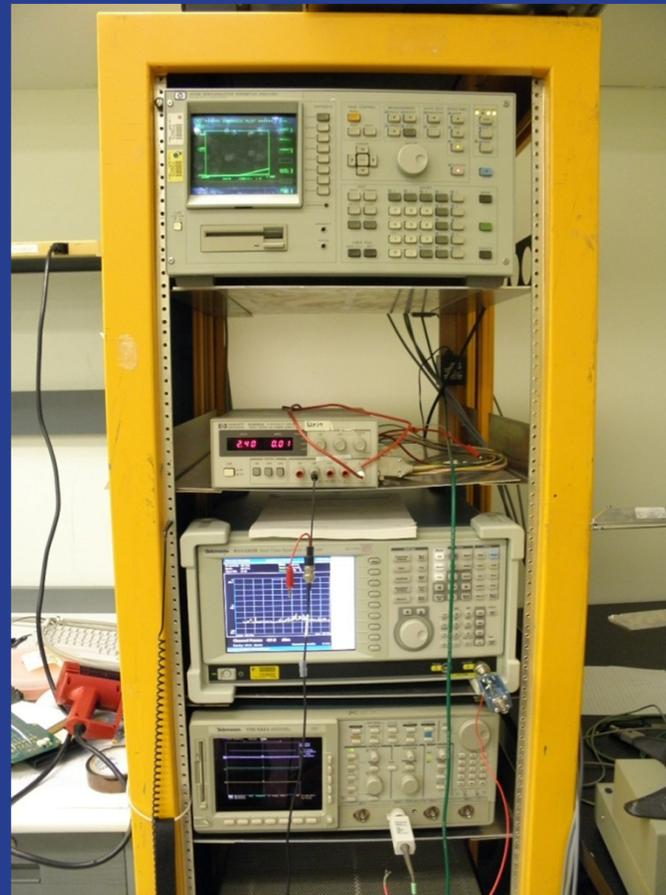


- Literature and foundries manual, e.g. *CMOS 9SF IBM Technology Design Manual* include analyses of even such details as:
  - departures from a single exponent power law for time dependence of progression of HC-induced damage, including general ~50% damage saturation
  - dependence damage on not only transistor channel length ( $L$ ) but on channel width ( $W$ ) too
  - loss of symmetry in operation of damaged transistors, etc.but practically only focusing on RoomT
- Operation in cryogenic conditions “makes transistors faster” for the same bias conditions on device terminals; electron mean free path increases, thus hot carrier degradation may be expected to be more severe and include other processes than known so far, thus:
  - degradation of transistors from 130nm CMOS process from Global Foundries was studied at Fermilab
  - accelerated stress tests were carried out (assuming exponential dependence of parameter  $A$  in power law on  $V_{DS}$ )

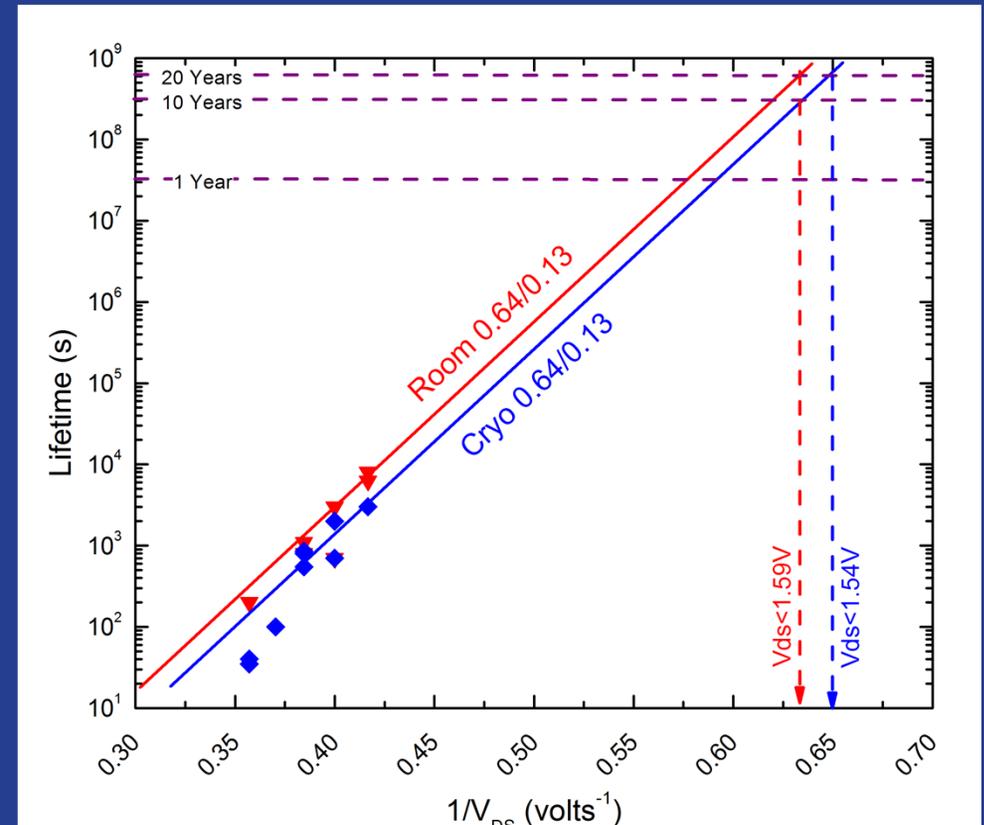
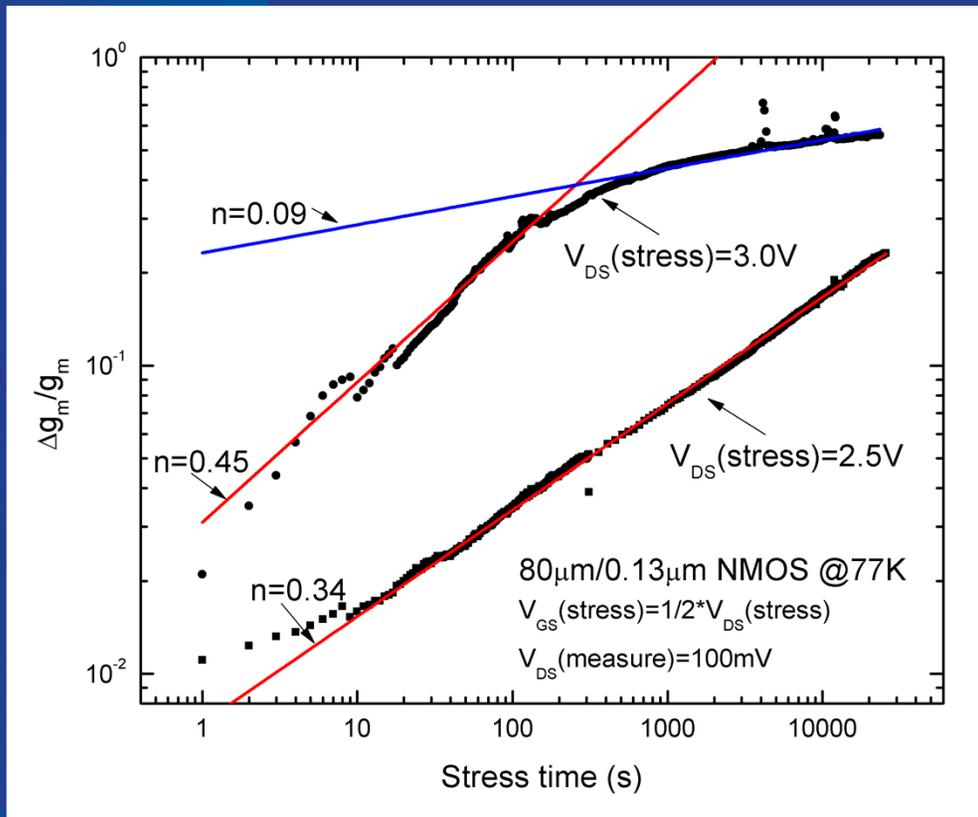
# Setup and procedure for tests at Fermilab



- Accelerated stress experiments were carried out on two separate setups. The low current setup: HP4145B Semiconductor PA; the high current setup: a set of Keithley 237 + Keithley 2400 SMU. Both setups were controlled by custom LabView programs that were created for these experiments and modified as needed.



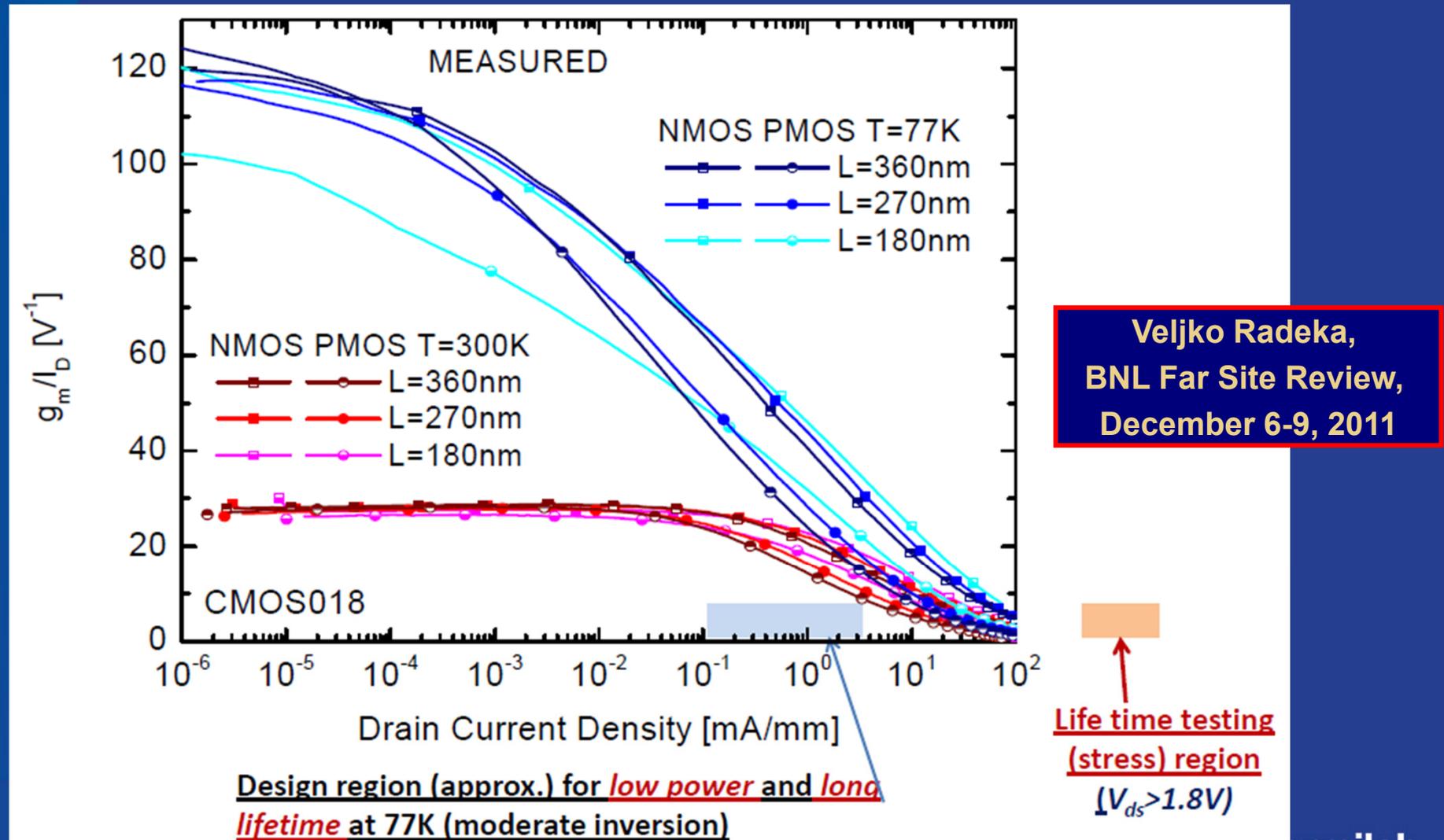
## Tests performed on 130nm Global Foundries transistors from TX and TY chips from 3D-IC MPW run – close collaboration with experts from Georgia Tech.



- Example of degradation of maximum transconductance for minimum channel length NMOS transistor; visible presence of a fast component (early mode degradation) and  $\sim 50\%$  saturation of degradation for two  $V_{DS}$  in accelerated stress conditions – the results qualitatively correspond to foundry manuals for RT.
- Lifetime derived from limited time measurements **under worst stress** conditions; extrapolation of lifetime towards full time of the experiment leads to  $V_{DS\text{max}}$  (arbitrary end-of-life criterion of 10%)
- Difference in lifetime for RT and CT is not great for this process; lifetimes at both RT and CT can be projected to more than 20 years at the nominal voltage (1.5V) for this technology

# Correspondence between stress tests and normal operation

- Observations indicate that the main mechanism of degradation is the generation of interface states (although other components are visible),
- accelerated tests retains validity, considered combinations of voltages and current densities is a very worst-case and will never be in a real circuit (analog)



Veljko Radeka,  
BNL Far Site Review,  
December 6-9, 2011

# Conclusions

- **Strategic goals** of process evaluation for cryogenic operation **were achieved** (macroscopic understanding)
- The lifetime at low temperatures is limited by a predictable and a very gradual degradation (aging) **mechanism which can be controlled**
- Hot carrier induced degradation **does not fall under the usual definition of device reliability** (failures occurring randomly in time with some probability)
- Correspondence between RT and CT: the device properties are significantly improved at CT, in part due to increased electron mean free path (MFP) and mobility, the nominal  $V_{DS}$  has to be scaled down, to keep the product of MFP and the electric field constant
- **Deepening understanding**, clarifying on correctness of predictions under stressing, making precision measurements are still appealing (*dedicated, optimized tests structures submitted on the MOSIS 3D-IC MPW run in Nov. 2011, acquiring cryo-cooler to allow measurements in robust conditions*)
- *LBNE will be able to rely on three mainstream CMOS or BiCMOS processes (180nm TSMC studied at BNL, 350nm IBM studied at Georgia Tech, and 130nm Global Foundries studied at FNAL – the latter is chosen for most projects at Fermilab)*
- Actual work on the electronic design can start – need of working out specification. Starting point could be the Giga-bit Optical Link (GOL) chip (designed by CERN for LHC) database of which was obtained from CERN by Fermilab – manpower needs to be carefully addressed

## Lifetime Studies of 130nm nMOS Transistors Intended for Long-Duration, Cryogenic High-Energy Physics Experiments

submitted to IEEE  
Trans. on Nucl. Sci.

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