Linear Collider Detector R&D at Fermilab

Fermilab PAC Meeting

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For the Fermilab ILC Detector & Physics R&D Group

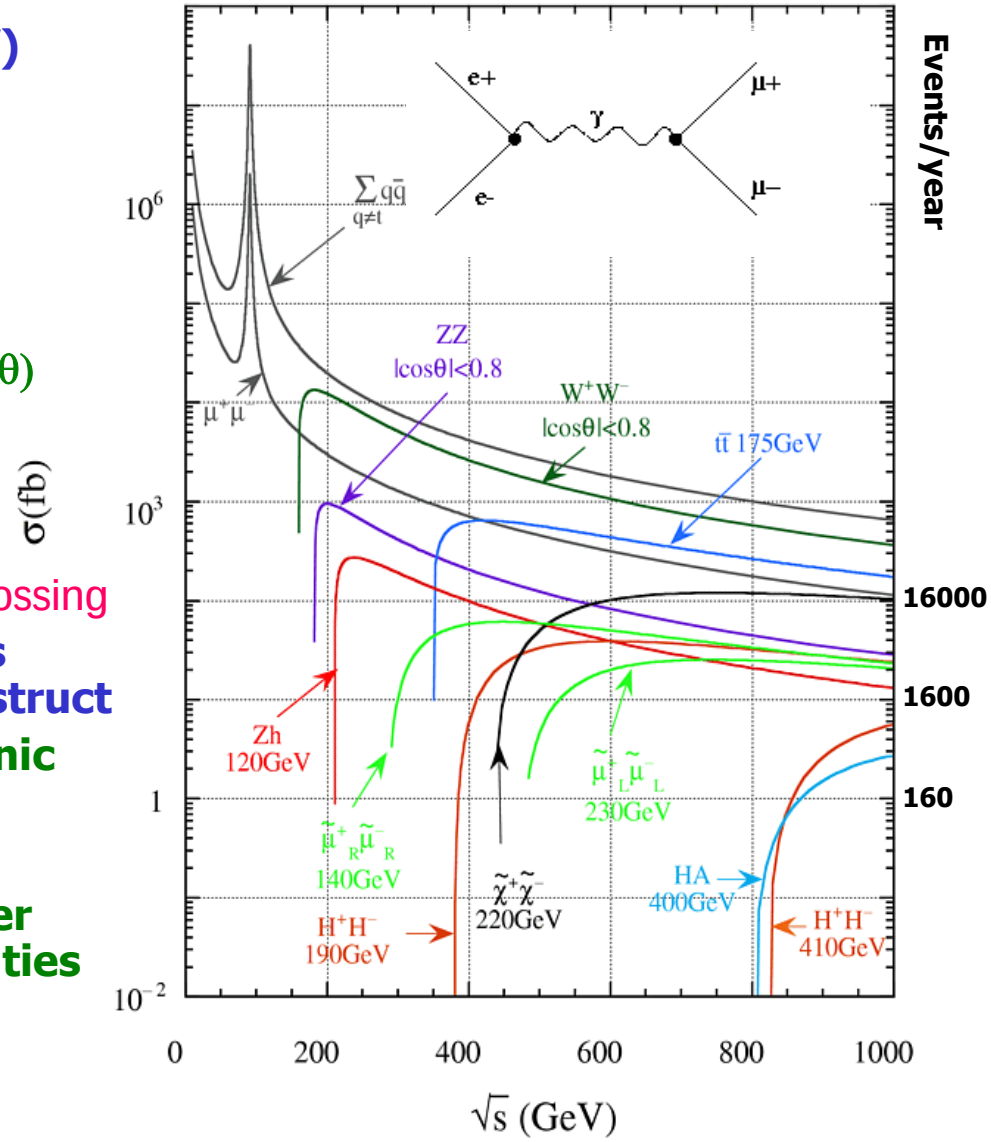
Fermilab
Oct. 20, 2006

Outline

- ***ILC Physics Characteristics***
- ***Brief summary of laboratory's main ILC detector R&D activities***
  - **Pixel Detectors**
  - **Silicon Tracker**
  - **Calorimetry**
    - SiPM test setup
- ***Upgrade of the MTest beamline***
- ***Outreach***
  - **Internal outreach to Fermilab staff**
  - **Outreach to user community**
- ***Program Management***
  - **Budget and Effort**
  - **Plans and Issues**

ILC Physics Characteristics

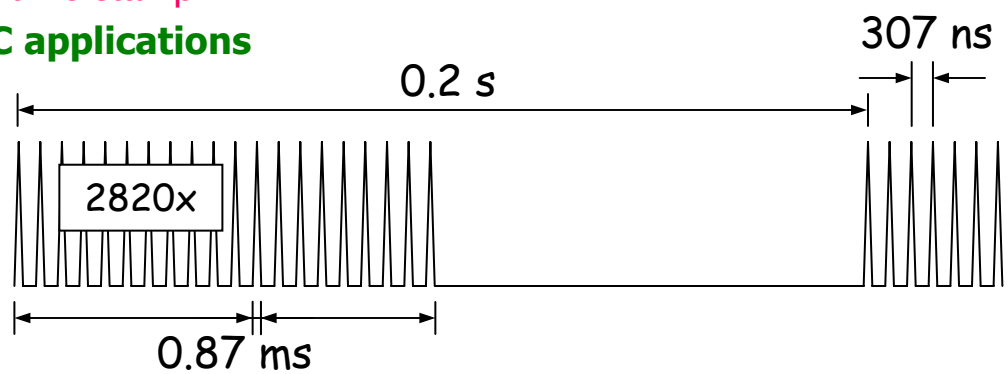
- **Machine design luminosity $\mathcal{L} = 2 \times 10^{34}\ cm^{-2}s^{-1}$ ($\sqrt{s}$ = 500 GeV)**
- **Processes through s-channel spin-1 exchange: $\sigma \sim 1/s$**
  - **Cross sections relatively democratic**
  - **Cross sections are small**
  - **Angular distribution: $(1 + \cos^2\theta)$**
    - Premium on forward region
    - Hermetic detectors
  - **Relatively large backgrounds**
    - 100k e^+e^- - pairs per bunch crossing
- **W and Z bosons in all decay modes become the main objects to reconstruct**
  - **Discriminate W and Z in hadronic decay mode**
- **Highly polarized e^- beam: ~ 80%**
  - **To employ discriminating power requires running at both polarities**
- **Every event counts !**



ILC year: 50% machine duty cycle
50% overall detection efficiency

ILC Pixel Detectors

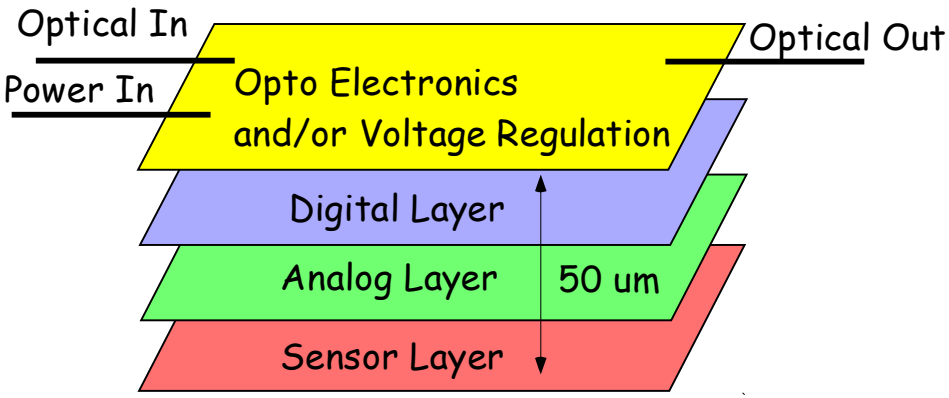
- **ILC requirements push the limits for low mass, low power and high resolution**
  - **Event characteristics require excellent b-identification capabilities through secondary and tertiary vertex finding and jet charge measurement**
  - **High occupancy environment due to machine and IP backgrounds**
- **Vertex detector requirements**
  - **Very low mass: 0.1% X_0 per layer (equivalent of 100 μm of Si)**
    - Low mass requires no active cooling, hence low power
  - **High resolution: impact parameter resolution of ~ 5 μm**
    - Requires smaller pixels which increases the readout circuit density
  - **Good and robust pattern recognition, integrated design**
    - Low occupancies, bunch crossing time stamp
  - **Modest radiation tolerance for ILC applications**



- **ILC beam structure**
  - **2820 crossings in a 1 ms bunch train**
  - **5 bunch trains per second**
- **ILC Maximum hit occupancy**
  - **Assumed to be 0.03 particles/crossing/mm²**
  - **Assume 3 pixels hit/particle (obviously this depends somewhat on pixel size, hit location, and charge spreading)**
  - **Hit rate = 0.03 part./bx/mm² x 3 hits/part. x 2820 bx/train gives 252 hits/train/mm²**

3D Integrated Circuits

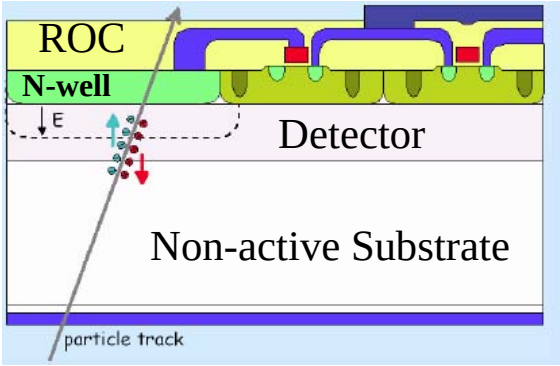
- **After careful consideration of available technologies and given the direction of industry, decided that the most promising approach would be the 3D integrated circuit design.**
- **A 3D device is a chip comprised of 2 or more layers of semiconductor devices which have been thinned, bonded, and interconnected to form a monolithic circuit**
  - **Layers can have devices made in different technologies**
    - Process optimization for each layer



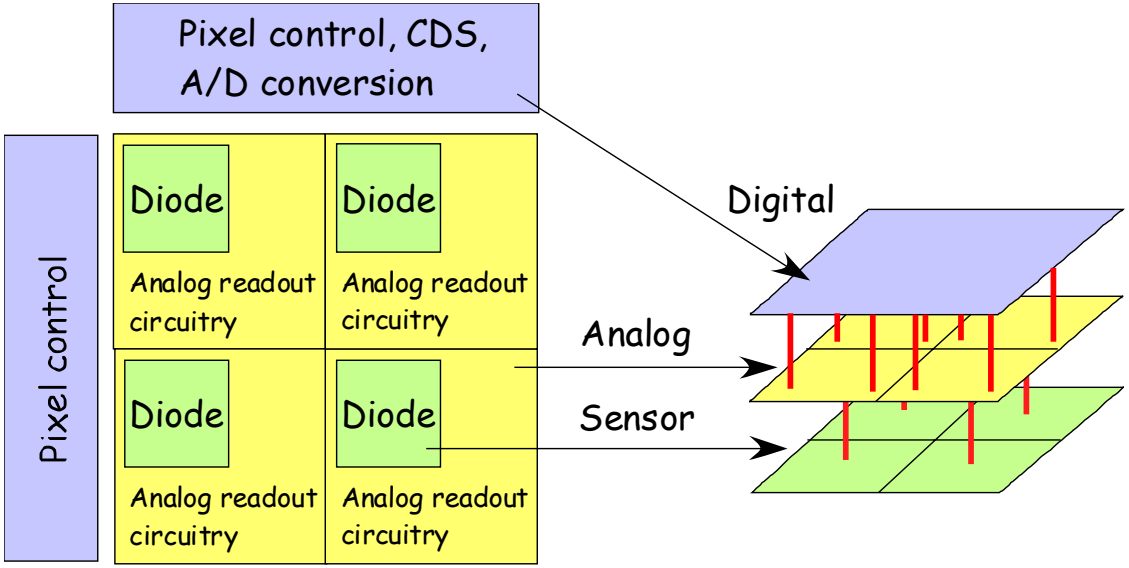
- **Technology driven by industry**
  - **Reduce R, L, C for higher speed**
  - **Reduce chip I/O pads**
  - **Provide increased functionality**
  - **Reduce interconnect power, crosstalk**
- **Critical issue are:**
  - **Layer thinning to < 10 μm**
  - **Precision alignment (< 1 μm)**
  - **Bonding of the layers**
  - **Through-wafer via formation**

3D versus Monolithic Active Pixels

- **A MAPS device is a silicon structure where the detector and the primary readout electronics are all processed on the same substrate**
- **Advantages of 3D devices:**
  - **Significantly higher functionality in a pixel cell using current feature sizes**
  - **NMOS and PMOS transistors**
  - **Processing of each layer can be optimized**
  - **100% active, minimal perimeter area requirements**



MAPS Principle

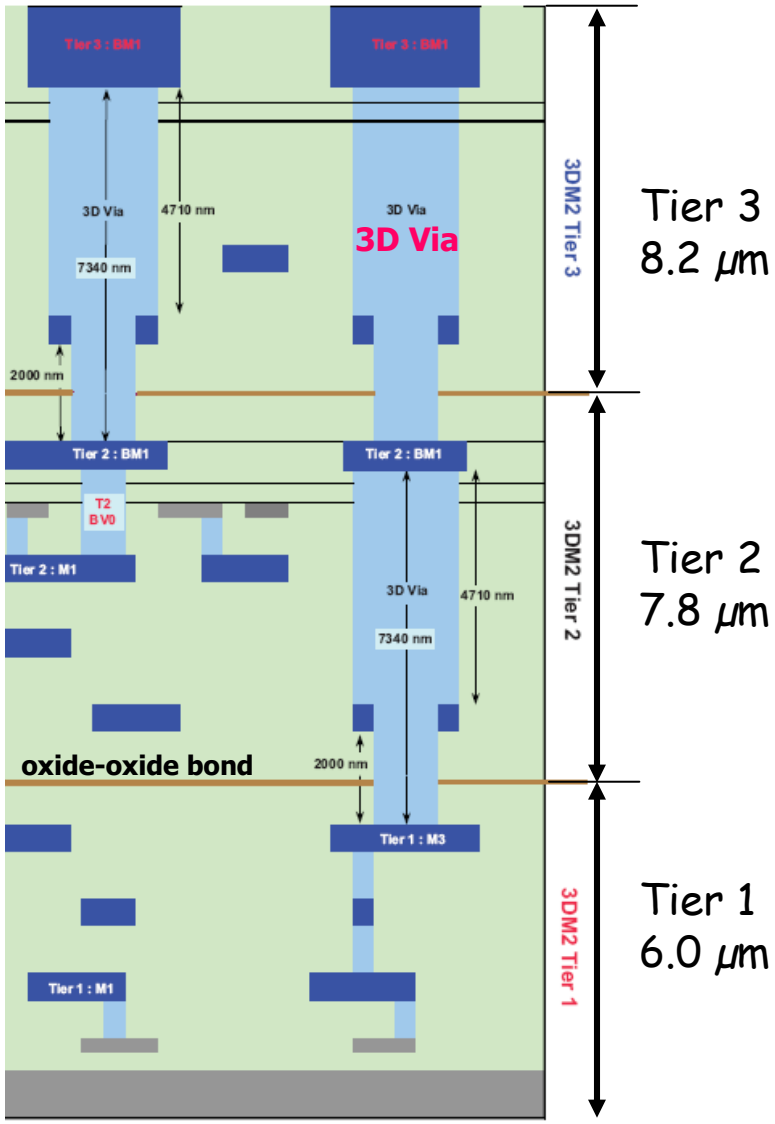


Conventional MAPS 4 Pixel Layout

3D 4 Pixel Layout

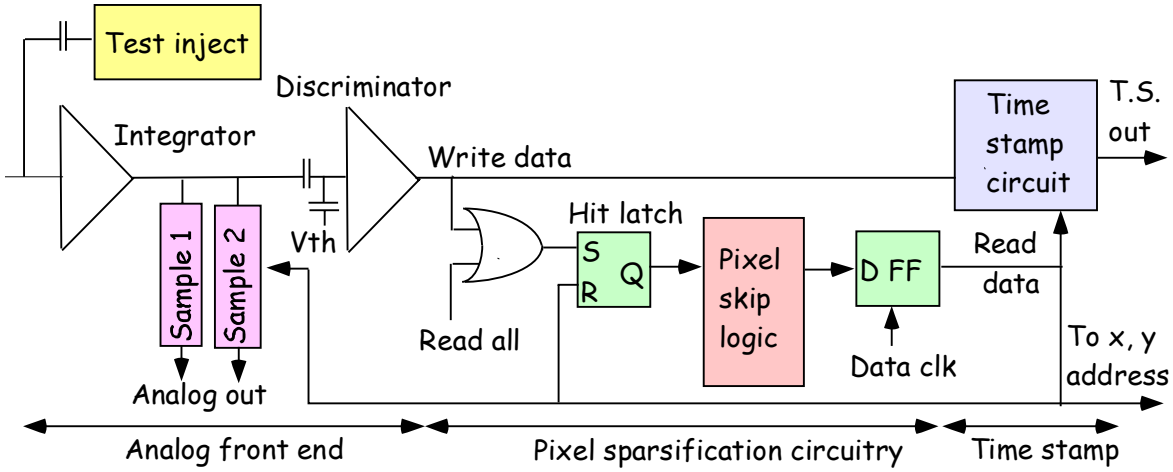
Development of a 3D Demonstrator Chip

- **MIT Lincoln Laboratories (MIT-LL) has developed the technology that enables 3D integration**
  - **Demonstrated the 3D technology through fabrication of imaging devices**
  - **Has infrastructure to allow for 3D Multi-Project Run fabrication**
- **We were invited to participate in the MIT-LL three-tier multi-project run**
  - **3D design to be laid out in MIT-LL 0.18 μm SOI process**
    - SOI provides additional advantages: BOX, full isolation, direct via formation, enhanced low-power operation
  - **3 levels of metal in each layer**
- **Submission deadline was Oct. 15, 2006**
- **Requested wafer space of ~ 2.5 x 2.5 mm^2**
- **Pixel size 20 x 20 μm; 64 x 64 pixel array**
- **No integrated sensor**
- **Chip has been submitted !**



Architecture of Demonstrator Chip

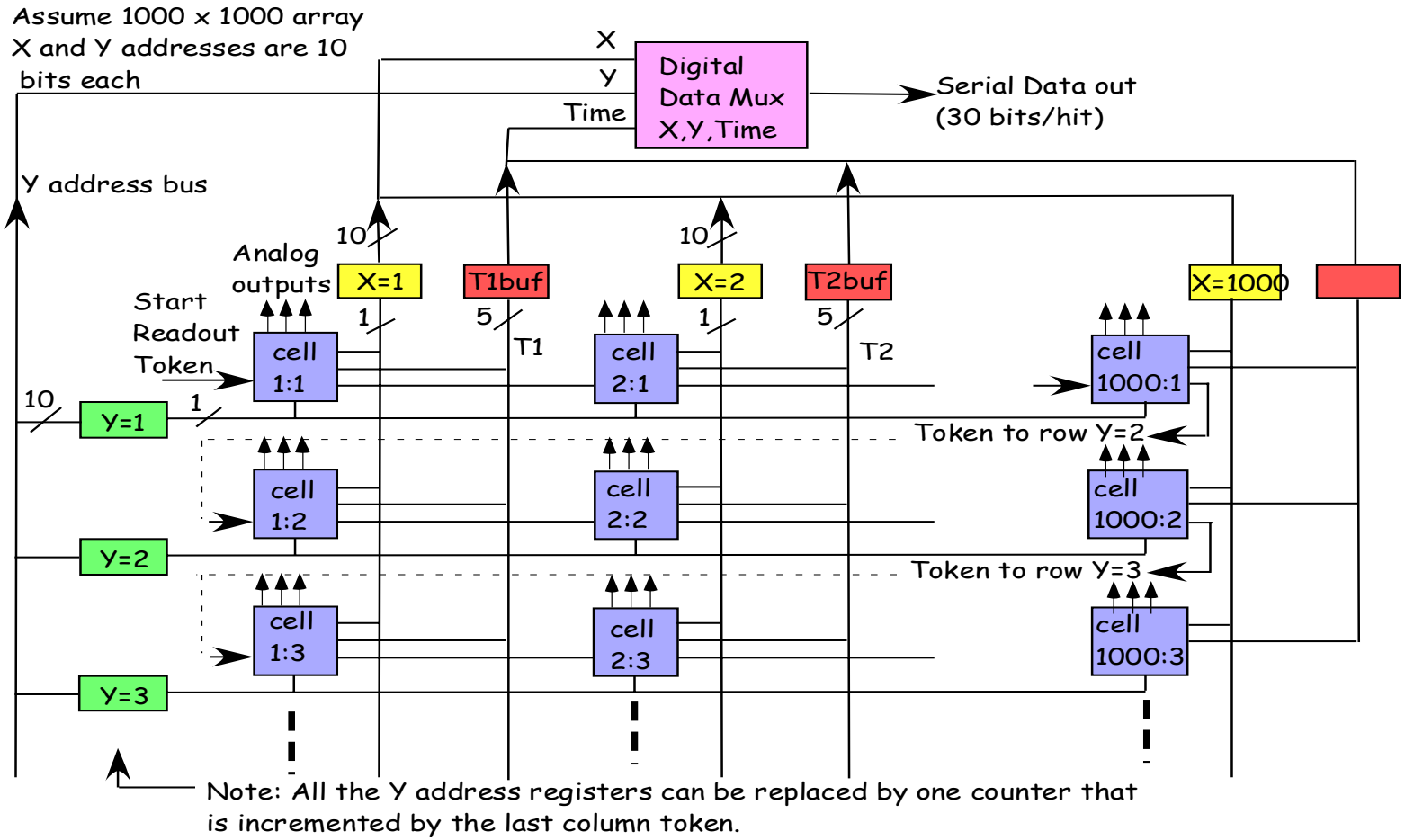
- **Design:**
  - **Provide analog and binary readout information**
  - **Time stamping of pixel hit for ILC environment**
    - Divide bunch train into 32 time slices; each hit pixel can store one time stamp equivalent to 5 bits of time information
  - **Sparsification to reduce data rate**
    - Use token passing scheme with look-ahead to reduce data output
      - During acquisition, a hit sets a latch
      - Sparse readout performed row by row with x- and y-address stored at end of row and column
  - **Chip divided into 3 tiers**
    - Pixels as small as possible but with significant functionality.
    - Design for 1000 x 1000 array but layout only for 64 x 64 array.



Schematic pixel cell block diagram

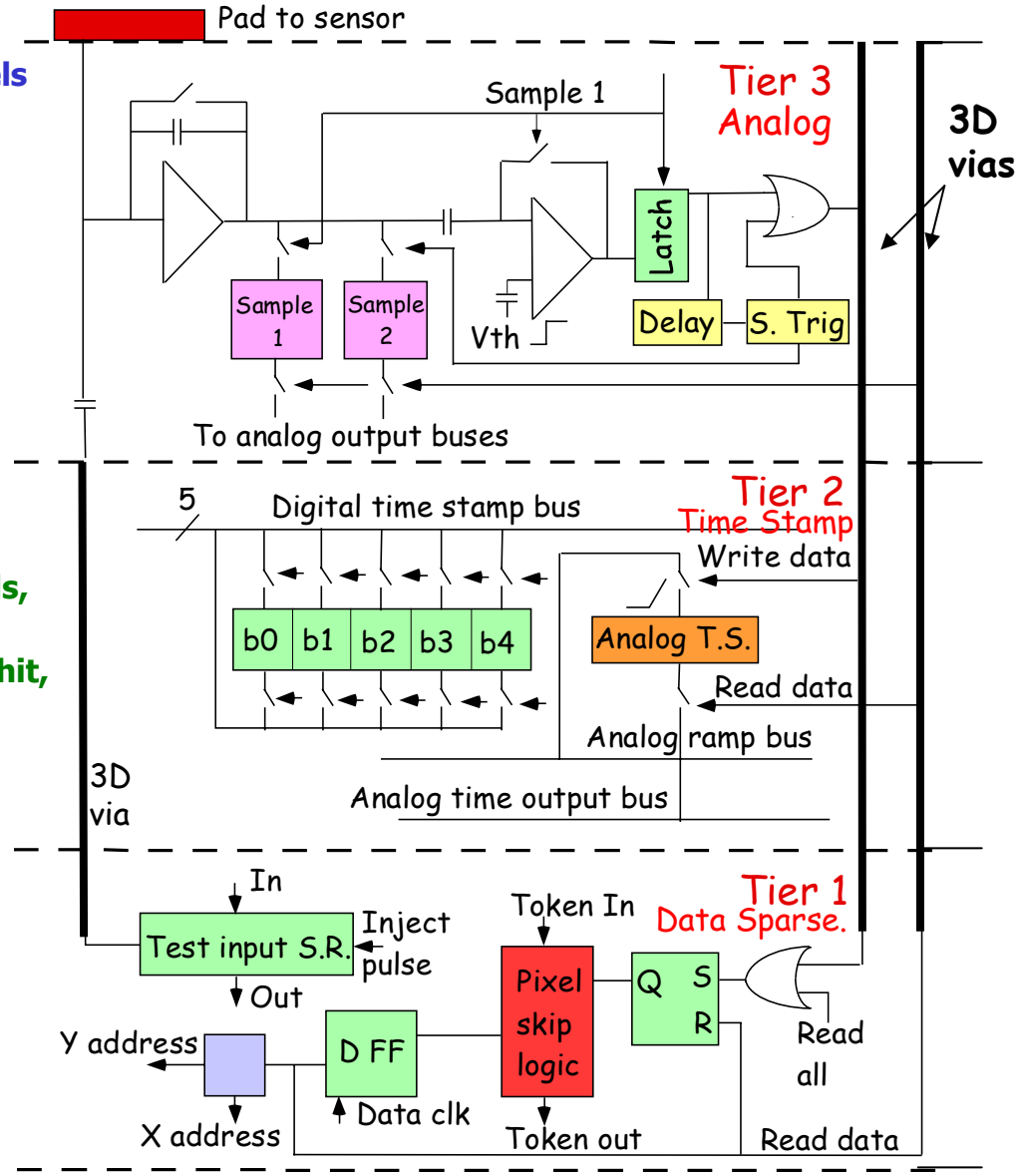
Pixel Readout Scheme

- **Pixel being read points to the x address and y address stored on the perimeter.**
- **At same time, time stamp information and analog pulse height is read out**
- **During pixel readout, token scans ahead for the next hit pixel (200 ps/cell)**



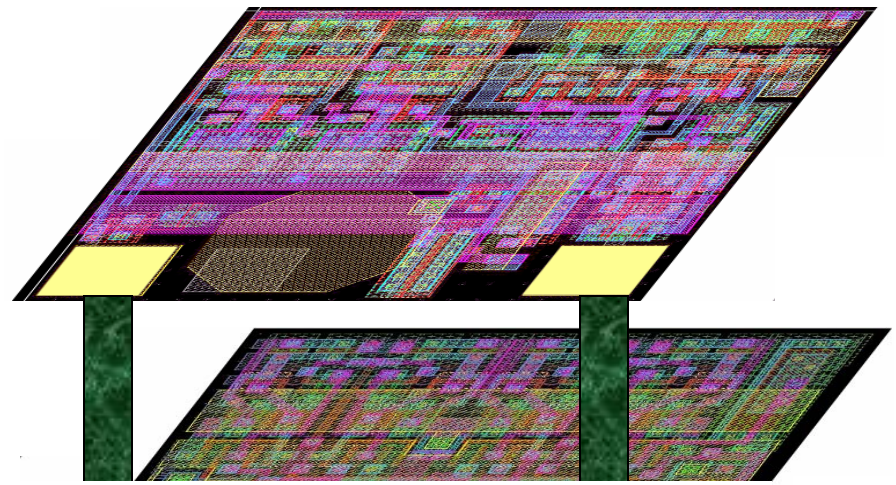
3D Three Tier Pixel Layout

- **Readout speed for an ILC environment**
- **Assume 1k x 1k array with 20 x 20 μm² pixels**
  - **First pixel in each row always read out**
    - Adds 1000 cells, small increase in data volume
  - **Time to scan 1 row: 200 ps x 1000 = 200 ns**
  - **Time to readout cell 30 bits x 20 ns/bit = 600 ns**
  - **Plenty of time to find next hit pixel during readout**
- **Assume maximum number of hits/chip of 250 hits/mm²**
  - **For a 1000 x 1000 array of 20 μm pixels, 100k hits/chip**
  - **For 50 MHz readout clock and 30 bits/hit, readout time: 100,000 hits x 30 bits/hit x 20 ns/bit = 60 msec.**
- **Readout time is far less than the ILC allowed 200 msec. Thus the readout clock can be even slower or several chips can be put on the same bus. Readout time is even less for smaller chips**

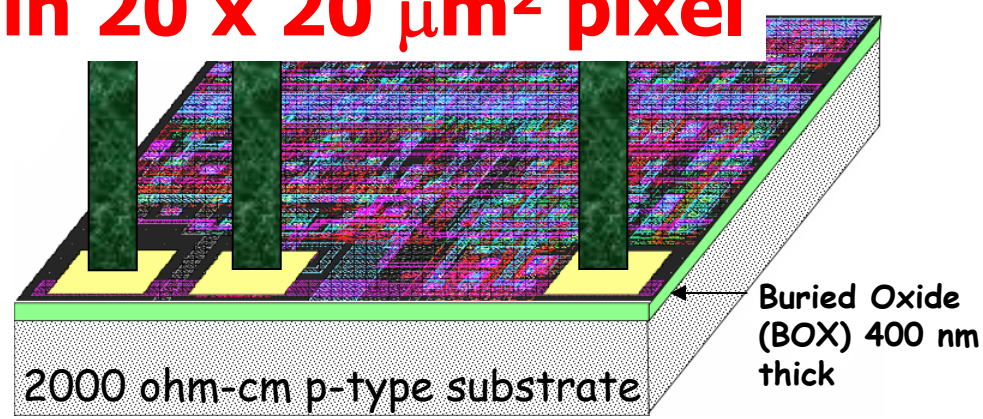


3D Stack

- Form 2 vias, 1.5 x 7.3 µm, through tier 3 to tier 2
- Tier 3
  - Integrator, DCS plus readout
  - Discriminator
  - 2 vias
  - 38 transistors
- Bond Tier 3 to Tier 2
- Form 3 vias, 1.5 x 7.3 µm, through Tier 2 to Tier 1
- Tier 2
  - 5 bit digital time stamp
  - Analog time stamp (ts)
    - Either analog or digital ts
  - 3 vias
  - 72 transistors
- Bond Tier 2 to Tier 1
- Tier 1
  - OR for READ ALL cells
  - Pixel skip logic for token passing
  - 3 vias
  - 65 transistors

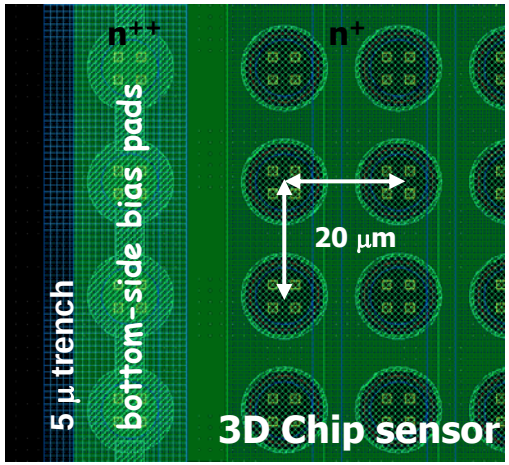


175 Transistors in 20 x 20 μm^2 pixel



Sensor Development

- 3D chip provides only readout. In parallel we are designing mating sensors on 6", high resistivity, float-zone, n-type wafers to be bonded to 3D chips
  - Sensor fabrication also at MIT-LL
  - Thinned to 50, 75, 100 microns, implanted and laser annealed
  - 4-side abuttable, i.e. no dead space
  - Deep trench etch, n doped poly-silicon fill provides edge doping
- Layout of 6" wafer is in progress
  - Standard p-on-n diodes
  - Design to mate with 3D chip, 20 micron pitch
  - Design to mate with FPIX chip, 50 micron pitch
  - Space available on wafer
- Note: LL 3D process has been used with a thinned, edgeless sensor layer as the bottom tier, which is the ultimate goal of our 3D development



- First design which, in principle meets 'all' of the ILC requirements for thickness, resolution, power dissipation, time stamping
  - Power is 75 microwatt/pixel ~ 1875 microwatts/mm^2 (no pulsing)
  - Noise is ~30-40 e^-
  - S/N = 100-200:1

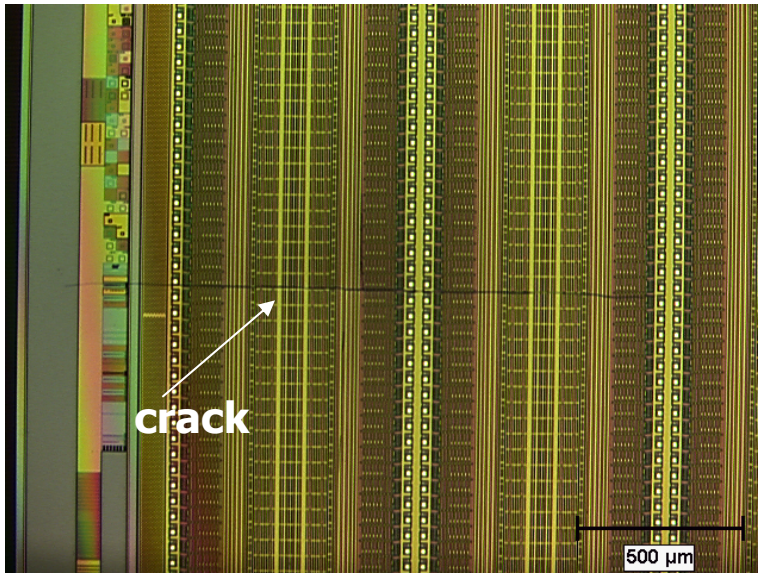
Device Thinning

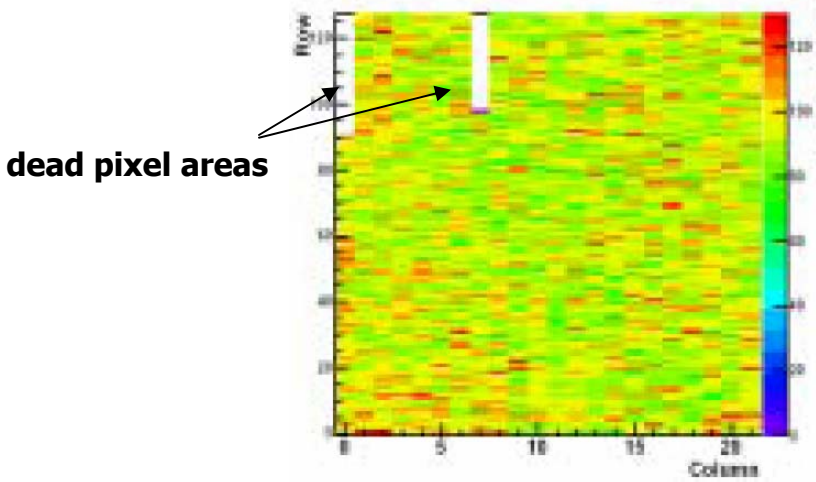
- **Gaining experience on device thinning and thinned devices**
  - **Thinning of FPIX chips at RTI**
    - Electrical and mech. characterization

    1) Backgrind and polish to 150 μm
    - 7 chips failed out of 72

    2) Plasma thinning down to 50/25/15/10 μm
    - Some devices thinned down to metal layers
    - 4 responding out of 20 testable devices; all have areas of dead pixels

# Die	target t (μm)	Ave. t (μm)	Non-Unif. (%)
4	50.0	50.4	11.4
4	25.0	28.5	12.4
4	15.0	15.3	21.1
4	10.0	13.2	56.3





    3) Repeat process after evaluation
    - 6 chips out of 8 working (2 dead) Slightly, but not significant, higher threshold and noise values

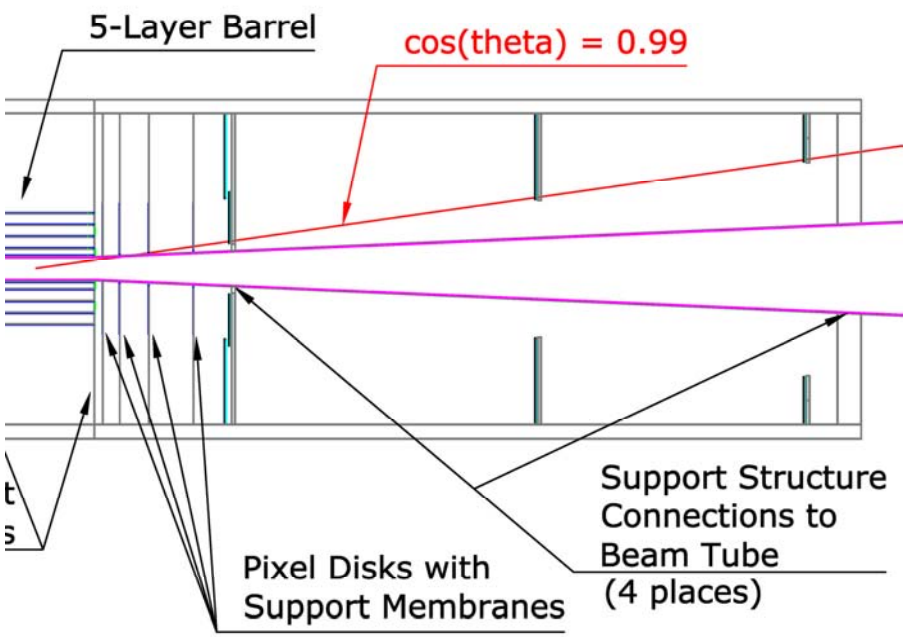
- **Thinning of metallized 6" wafers to 20 μm at commercial facility**
- **Also thinning FPIX wafers at IZM, Fraunhofer, München**

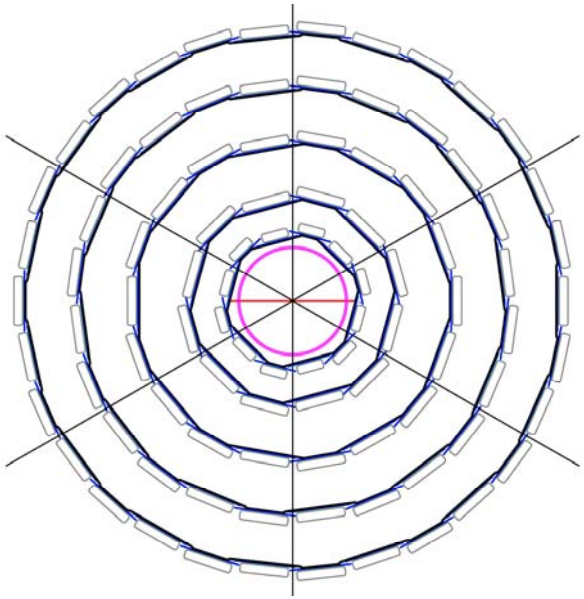
Other Si Sensor Activities

- **Investigating bump bonding options**
  - **20 micron pitch is difficult for most vendors – Indium currently seems to be the most expeditious candidate**
  - **Contacted**
    - RTI, acknowledged trying to bond
    - NASA Goddard, interested in bonding; seems most experienced
    - Need to specify wafer and (if possible) chip metalization
    - Also contacting DRS
  - **Exploring Cu fusion bonding**
- **SBIR with American Semiconductor (ASI), http://www.americansemi.com/**
  - **Develop process technology and models for integrated detector fabrication in their FLEXFET 0.18 μ SOI technology**
  - **Modeling work has started**
- **Started on a design in OKI SOI 0.15 μm process**
  - **Submission date mid-December**
  - **Possibly in collaboration with Japanese institutions**
- **Collaboration with IZM, Fraunhofer, München on device thinning**

Vertex Detector Mechanical Design

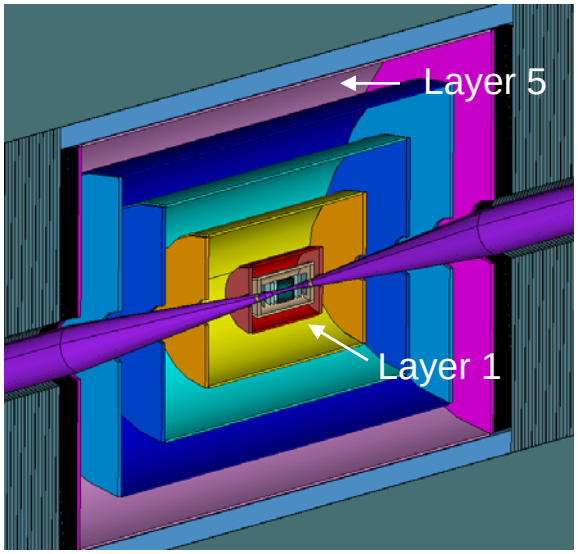
- **Vertex detector mounted in an outer, double-walled support cylinder**
  - **Cylinder is split along beam line to allow assembly around beampipe**
  - **Cylinders couple to the beam tube at z = ± 214 and ± 882 mm, and are supported by the beam tube, and stiffen it**
- **Proceeding to build prototypes of CF support structures**
- **Barrel Region**
  - **Five layers**
  - **Longitidunal coverage: ± 62.5 mm**
  - **Radial coverage: 14 < R < 61 mm**
- **Forward regions**
  - **Four disks**
  - **z = ± 72, ± 92, ± 123, ± 172 mm**
  - **Radial coverage: R < 71 mm**

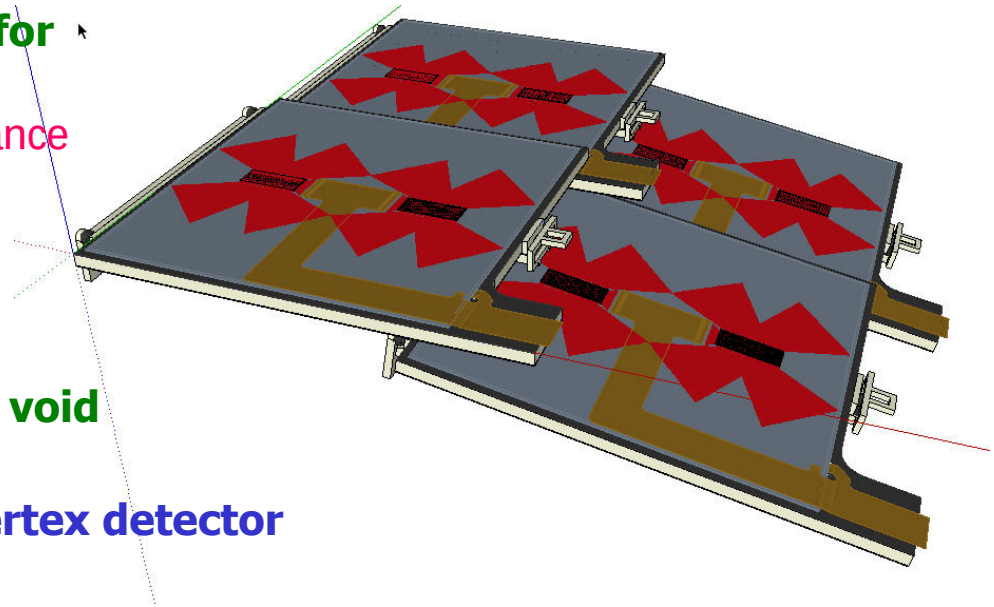




Outer Tracker Sensor and Module Design

- **In collaboration with SLAC, progressing on:**
  - **Optimizing outer tracker design**
  - **sensor and module design for outer tracker**
- **Readout does not employ a hybrid**
- **Sensor design uses bump-bonded readout chip**
  - **Sensor size 93.5mm x 93.5mm**
  - **Strip/Readout pitch 25 / 50 μm**
  - **Number of RO (IM) strips 1840 (3679)**
    - Need two readout chips
  - **Double metal layer optimized for strip geometry**
    - Minimize capacitance and balance with trace resistance
  - **S/N goal of 25**

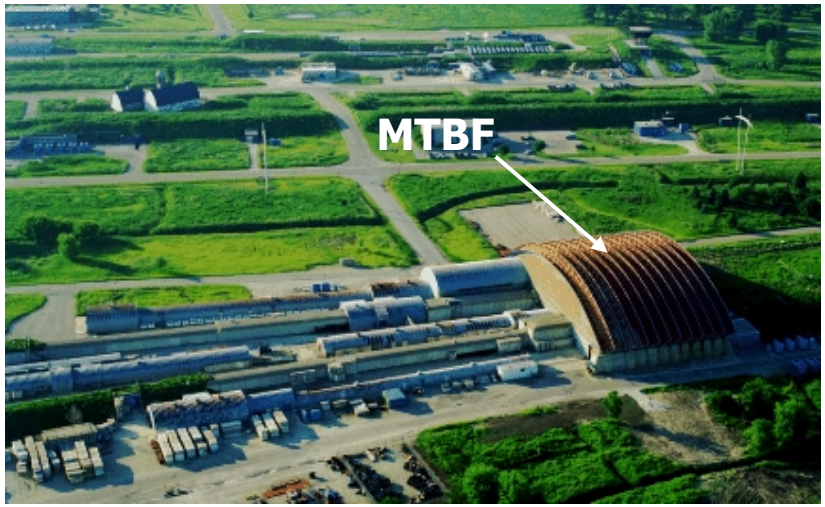




- **Module design**
  - **CF/Rohacell/CF frame: ~50% void**

- **Forward region integrated with vertex detector**

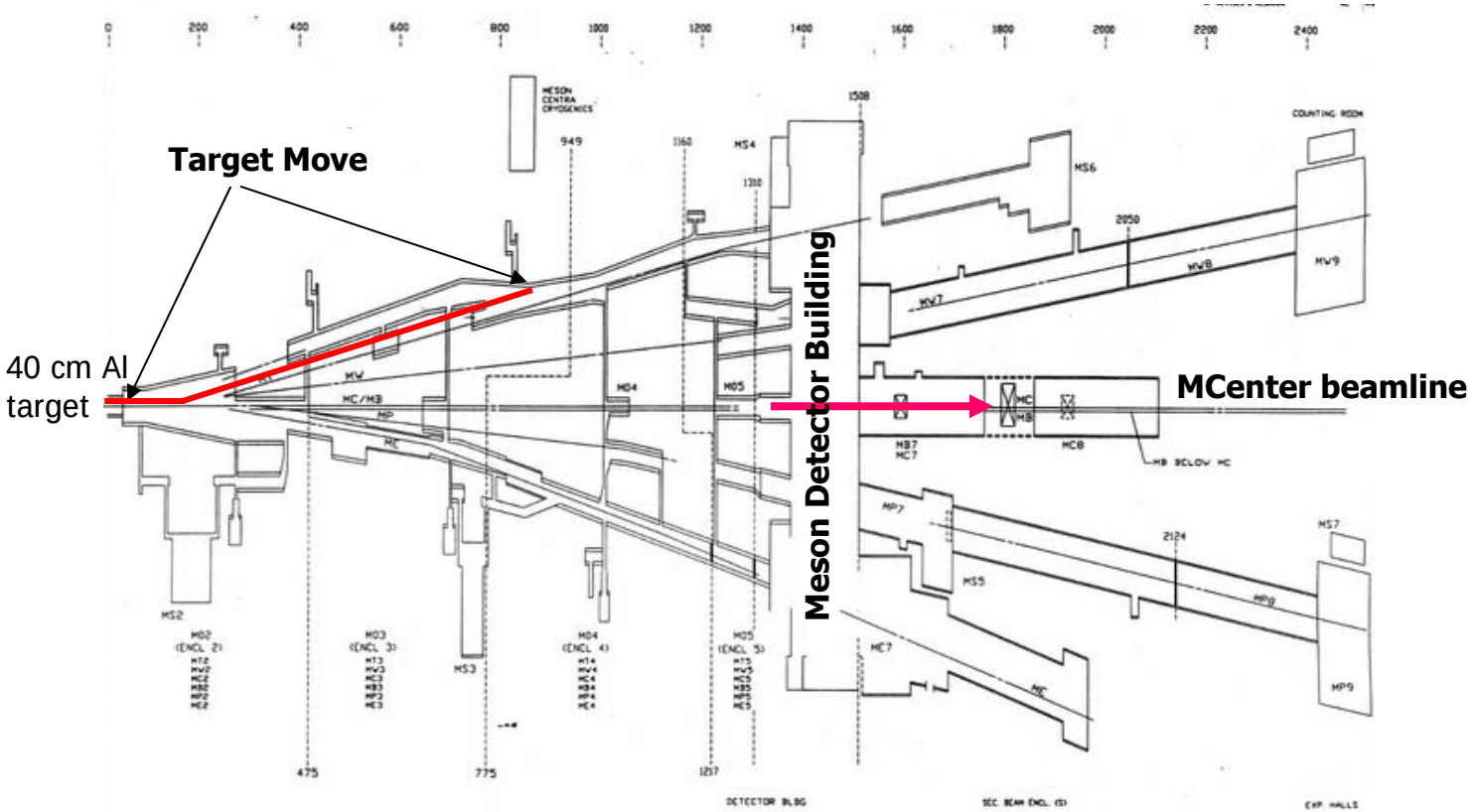
Upgrade of Test Beam Facilities



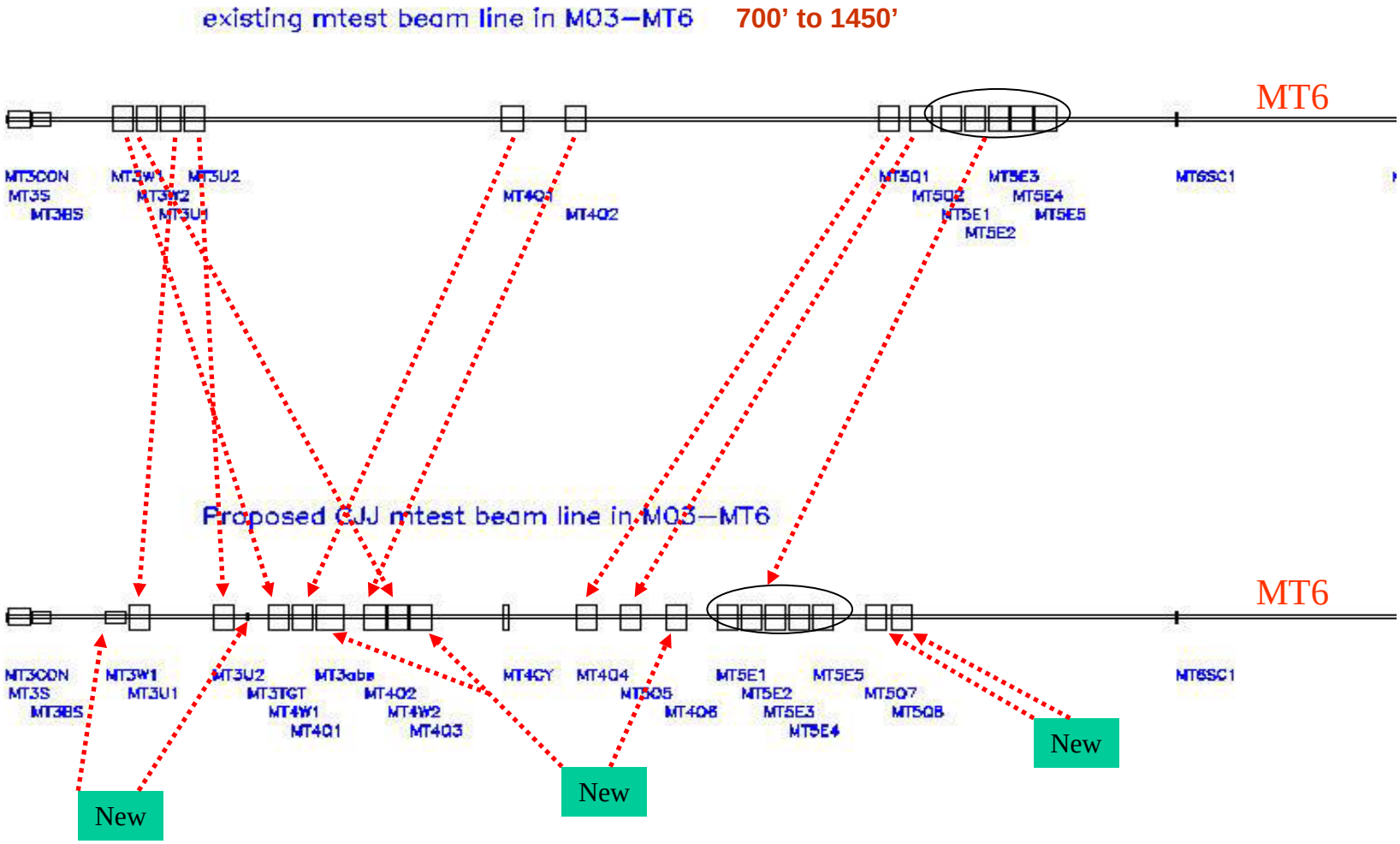
- **Testbeam facility at MT6:**
  - protons, pions, muons, electrons with momentum between 4 and 120 GeV
- **The ILC calorimetry test beam proposal (TM-2291) indicates a need for low energy pions (1 GeV) and high energy electrons (>25 GeV)**
- **Both of these beam types are difficult in the current test beam due to the length of the beamline and sheer number of windows, scintillators, etc.**
- **The External Beams Group has completed a design to install a movable target in the M03 enclosure and a redesign of the downstream part of the beamline**
- **Beamline monitoring and particle ID will be improved**
  - **Reduction of material in the beam**
  - **Addition of differential Cherenkov counter**
  - **Beamline TOF and Tracking with a silicon pixel and SciFi stations**
- **And, most importantly, the roof is being fixed !**

Beam Specifications

- **Beam specifications for upgraded facility:**
  - **Particle momentum as low as 1 GeV**
  - **Momentum bite 2% < 5 GeV, 1% >5 GeV**
  - **Beam Spot 1" > 10 GeV, trigger counter determines below 10 GeV**
  - **Parallel section for Cherenkov <0.3 mrad**
  - **Horizontal dispersion 1% dp/p per inch**



Beam Layout



- **Move 13 magnets, add 7 new elements, add Hall probes, add low current power supplies, move beam line transversely including trim magnets, instrumentation, vacuum pumps**

Expected Performance

- Moving the target to MT3 (L=1273-1388′ goes to L= 451-566′) reduces the decay length for pions
- Reduce the material in beamline
  - From 17.8 % X_0 to ~ 3.4% X_0

Energy (GeV)	Hadron Enhancement	Electron Enhancement
4	25	~90
8	6.4	14
16	2.5	6.3

Energy (GeV)	Gain due to Pion Decay factor
1	90
2	9.2
4	3.0
8	1.8
16	1.3
33	1.2
66	1.1

- New Design has larger momentum (from from ¾% to 2%) and angular acceptance available
- Commissioning of new beam line to start mid-December

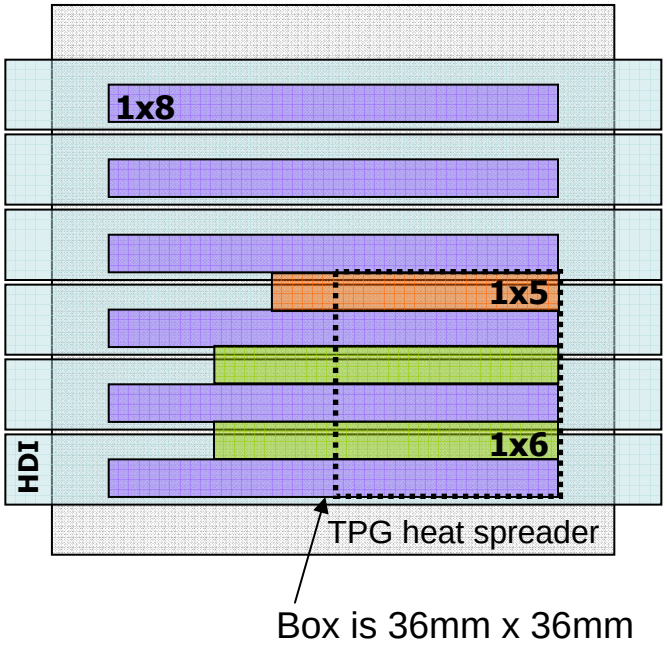
Energy (GeV)	Present Hadron Rate MT6SC2 per 1E12 Protons	Estimated Rate in New Design (dp/p 2%)
1	---	~1500
2	---	~50K
4	~700	~200K
8	~5K	~1.5M
16	~20K	~4M

Spill Structure

- Accelerator Division spent several weeks in June, coming back up from the spring shutdown, to develop a new Main Injector extraction ramp structure for SwitchYard 120 beam.
- Successfully implemented a 0.9 second flattop spill
- The AD is working to automate the switchover from one type of spill to the other, which is difficult due to its effect on anti-proton production.
- Heating of the Main Injector dipole magnets physically limits us to one 3.6 second spill per minute, but allows for approximately 16 0.9 second spills per minute.
- Currently the default scheme is one 3.6 second spill/minute (or two 0.9 second spills/minute), for 12 hours a day.
- The actual number of spills allowed for SwitchYard 120 extraction is determined by Program Planning, since it affects the rest of the Fermilab program. We are limited to a 5% impact on the Tevatron or Neutrino program following a flexible algorithm

Beam Line Instrumentation

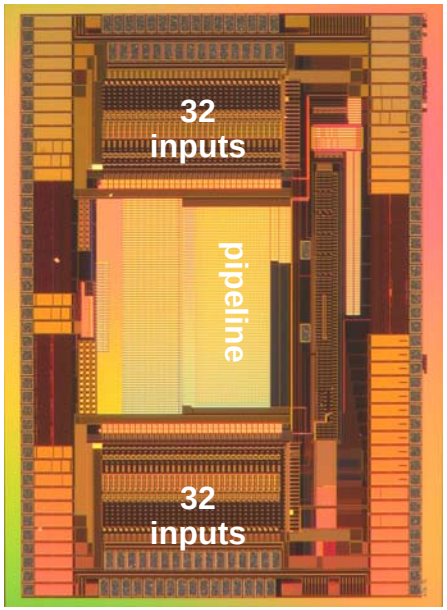
- **Building a pixel beam telescope with a pointing resolution of ~3 μm**
  - **Synergy with the development and testing of thinned readout chips, FPiX in collaboration with RTI**
- **Layout of beam telescope**
  - **Given variety of devices available from BTeV sensor wafers, various options with regard to size of telescope**
    - 1x8 active area corresponds to 73.6mm x 6.4mm
    - light blue shows size of 8-chip HDI



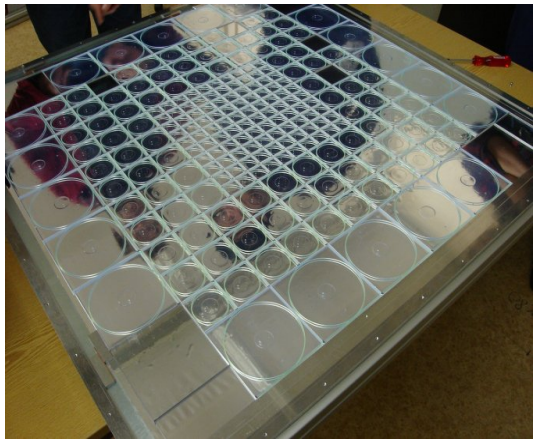
- **Construction of differential Cerenkov counter**
- **Beamline TOF system with ~ 100 ps resolution**
- **Construction of four sets of scintillating fiber tracking detectors**

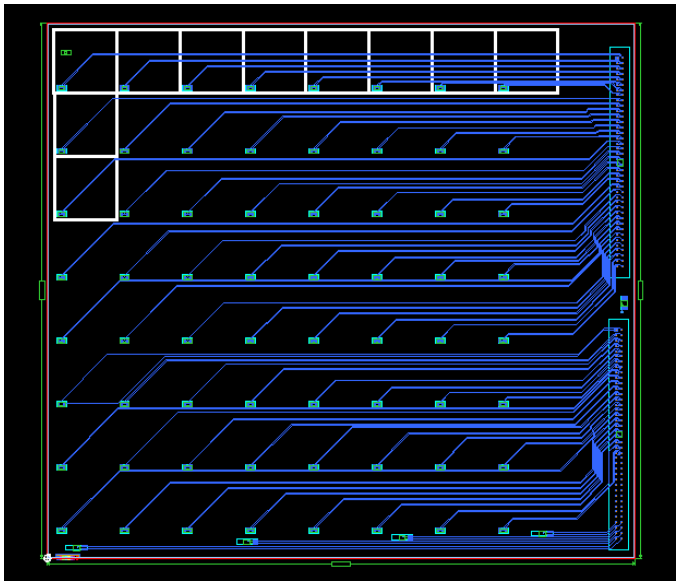
Calorimetry

- **Developed successful readout chip for digital HCAL for RPC's and GEM's (received Oct. 16, 06)**
  - **Critical for establishing proof of principle for RPC based calorimetry**
  - **Slice test of set of 10 planes in fall 2007 in Mtest test beam**



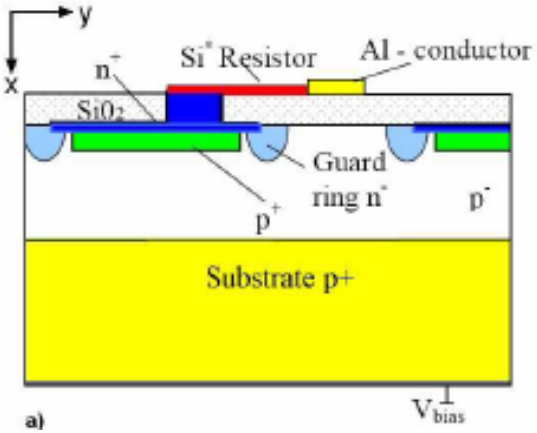
- **Analog calorimetry based on scintillator tiles with WLS fiber readout through Silicon Photo Multipliers**
  - **Focusing on electrical and mechanical integration; designed PCB for readout**
  - **64 Si-pm's and 4 temperature sensors**
  - **8 mil trace with 8 mil spaces.**





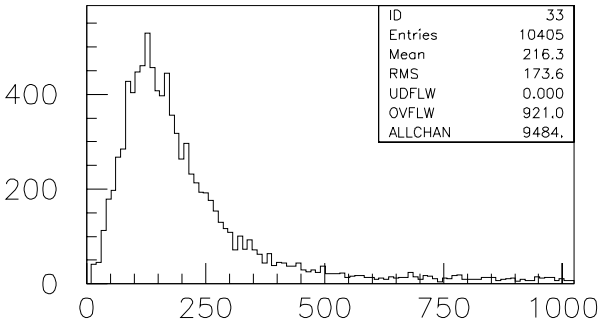
Silicon Photomultipliers

- Avalanche photodiode operating in Geiger mode (also called Multi-Pixel Photon Counter)
  - Array of pixels connected to a single output
  - Signal = Sum of all cells fired
  - If probability to hit a single cell < 1 => Signal proportional to # photons
- New detector development; devices not commercially available yet
- Multiple applications
  - Dual readout, lead-glass – scintillator sampling calorimetry
  - Analog scintillator tile hadron calorimeter
  - Muon detector based on scintillator strips
- In process of setting up a SiPM test station
  - Leverage existing infrastructure at SiDet
  - Starting a collaboration with Ires-Trento (INFN)
  - Contacts with Mephi, Hamamatsu and SensL
  - Gauging interest and possible collaboration with ANL and UofChicago

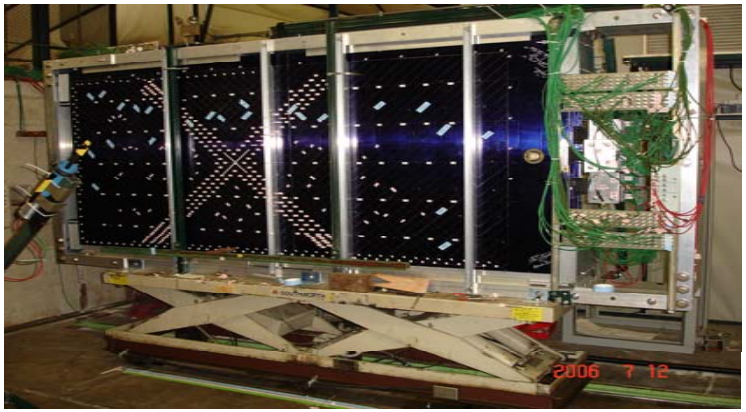


SiPM Characterization

- **Instrumented Muon scintillator strip detector MAPMT and SiPM readout, tested at Mtest**

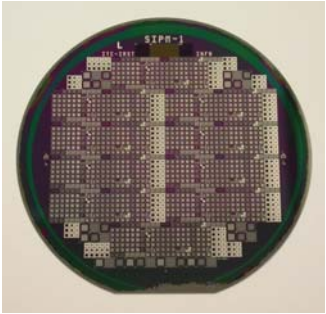


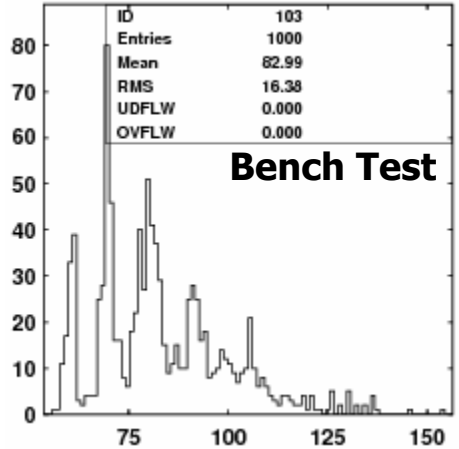
120 GeV protons
MAPMT readout

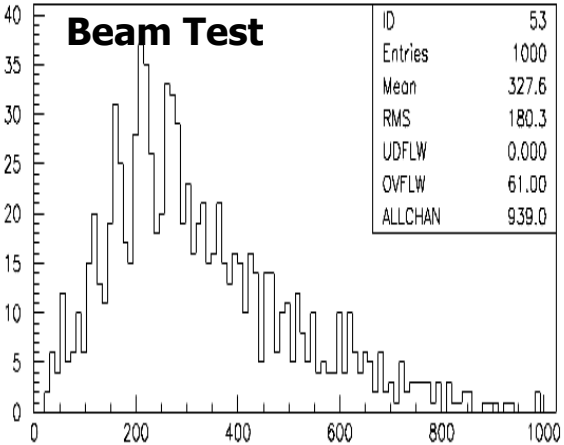


- **INFN/Udine characterizing ITC-Irst SiPM's at SiDet**
  - **Prototype SiPM geometry:**
    - 25x25 cells
    - cell size: 40x40 μm^2
  - **Bench and beam test characterization**
    - V_{bias} = 35 V
    - Dark count 0.8 MHz

$$\text{Gain} = \frac{10 \times 0{,}25.10^{-12} C}{1{,}6 \times 10^{-19} C} = 1{,}6 \times 10^{7}$$







Collaborative Efforts

- Our goal is to establish as many collaborative efforts as possible
- Pixel sensor technology
  - Continuous Active Pixel Sensors (CAPS): Hawaii – Fermilab collaboration
  - Monolithic Active Pixel Sensors (MAPS): UC Berkeley – LBL – Fermilab – Strassbourgh
  - 3D Technology: Fermilab – Purdue – Cornell – Bergamo collaboration
- Vertex detector Mechanical Design
  - Fermilab - SLAC – Strasbourg - UC Berkeley – U of Washington collaboration
- ASIC development
  - DCAL chip for digital hadron calorimetry (RPC and GEM): Argonne – Fermilab – UTA collaboration
- Scintillator Hadron Calorimetry
  - SiPM characterization: Fermilab – NIU – Udine – ITC-irst collaboration
  - Muon Tail Catcher mechanical and electronics design: Fermilab – NIU collaboration
- Muon Spectrometer
  - Fermilab – Indiana - NIU – Notre Dame - UC Davis - Wayne State collaboration
- Solenoid Design
  - Fermilab – Iowa – SLAC - Tokyo – KEK – Toshiba collaboration
- Tracking Software Development
  - Brown – Fermilab – SLAC – Lecce collaboration

Communication

- Merged SLAC lcd meeting with Fermilab ILC detector and physics meeting into a weekly joined ALCPG Physics and Detector meeting
  - Organized by SLAC and Fermilab, Thursdays 11am (1pm) PDT (CDT)
  - Broad US participation

- Re-instituted Fermilab Research Techniques Seminars with emphasis on ILC

– Oct. 25, 06	Claudio Piemonte Nicoleta Dinu	Development of Silicon Photomultipliers at ITC-irst, Measurement of the Photodetection efficiency of SiPMs
– Sept. 25, 06	Frank Gaede	Simulation and Reconstruction Software for the ILC
– July 17, 06	Marcel Trimpl	DEPFET Pixels for the ILC Vertex Detector
– July 6, 06	Adam Para	ILC Calorimetry
– June 6, 06	Hans-Guenther Moser	DEPFET Active Pixel Sensor as Vertex Detector for the ILC
– May 4, 06	Valerie Saveliev	Silicon Photomultipliers: Development and Application
– May 2, 06	Grzegorz Deptuch	MAPS for Not Visible Light Applications: Advantages and …

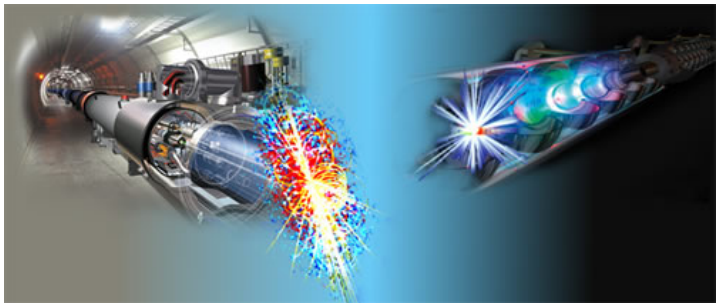
- Weekly ILC lunch discussions

- Review of software frameworks (org.lcsim, Jas, Marlin, Mokka, ILCRoot, …)
  - Evaluate Fermilab participation

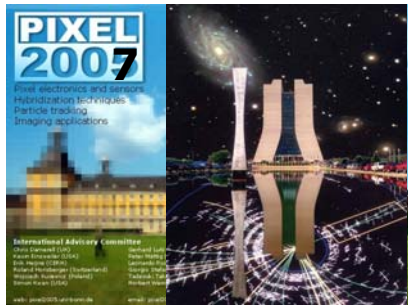
Hosting Various Workshops

- **To address issues of critical importance to the ILC and the community at large and to strengthen its role to bid to host**
  - **Hadronic Shower Simulation Workshop**
    - Understand shortcomings of modeling of hadronic showers
    - Agreement to make it a periodic meeting
    - Sept. 6-8, 2006

  - **Test Beam Workshop**
    - Evaluation of test beam needs at Fermilab
    - Jan. 17-19, 2007
  - **ILC - LHC Connections**
    - "The LHC early phase for the ILC"
    - Continuation of previous set of meetings
    - April 12-14, 2007



  - **Pixel 2007**
    - Most significant conference on pixel detector work
    - Use synergies with Astroparticle physcs applications
    - Spring 2007



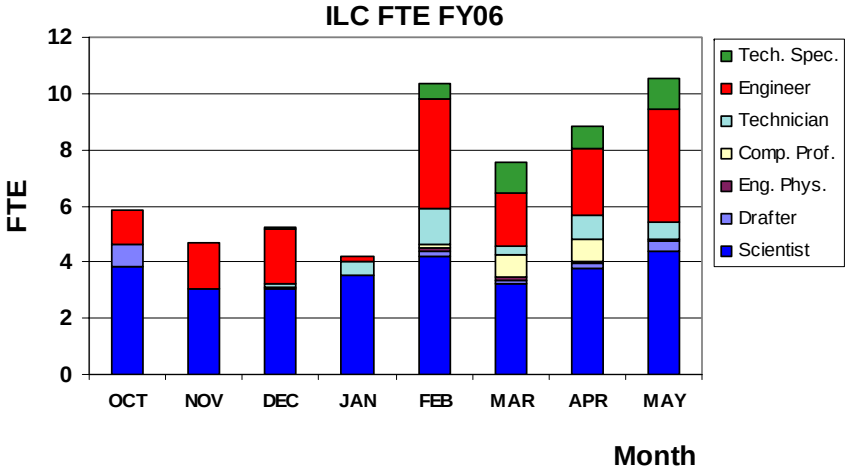
  - **Joint ALCPG/GDE Meeting**
    - Regional ILC meeting
    - October 22-26, 2007

Budget and Effort

- **Actuals for FY06**

#'s in k$	FY05		FY06	
	SWF	M&S	SWF	M&S
PPD Total			2,323.9	
ILC Detector	~400	200	1,001.6	446.6

  - **In addition $960k of CDF re-direct money allocated to upgrade of Mtest**
- **ILC detector breakdown according to resource for FY06**
  - **Spike in January due to correction to effort reporting**
  - **Effort on ILC Test Facilities not included**



- **Request for FY07: M&S $1,900 (assuming a full 3D run) and 20 FTE's**
- **Additional support for MTest improvements required from AD at the level of ~7 FTE**

Plans and Issues

- **Become a leader in design of pixel sensors for the ILC, the readout electronics and the design of mechanical support structures for vertex and tracking detectors**
- **Further enhance the test beam facility with associated support for particle identification, data acquisition and data analysis**
  - **Test beam environment should be as user-friendly as possible**
    - Plug-and-play operation for beam tests
    - Lacking support for data acquisition
- **Participate in the development of the calorimetry for the ILC and the associated algorithms**
- **Our role in the ILC software support is non-existent. We need to determine if, and what role we would like to play**
  - **Presentations by all (except Asian) frameworks at the lab; opportunities exist**
- **Need to take a prominent role in physics benchmarking processes and detector design optimization**
  - **Seriously lacking software support**
  - **Unique opportunity to make local effort very coherent, sharpen the physics potential and optimize detector design for the conceptual design reports**

- **For our "global" role as potential host**
  - **Create an intellectually inviting, supportive environment for ILC collaborators and vibrant user community**
  - **Co-lead and direct world-wide efforts; facilitate test beam coordination**

- **Overall goal to (more than) double our ILC effort again in the coming year**