



The Run IIb CDF Detector Upgrade Project

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Background

- The CDF Run IIb project exists to keep the experiment vital during high luminosity operation.
- Originally, the project was motivated by both high integrated and instantaneous luminosity.
 - Reduced integrated luminosity projections reduced the motivation for the silicon detector, resulting in its cancellation.
- Design goal instantaneous luminosity projections are still $\sim 3 \times 10^{32} \text{cm}^{-2} \text{s}^{-1}$
 - Now at 396 ns crossing – higher occupancies than planned
- Portions of the project motivated by instantaneous luminosity are still needed and have been retained



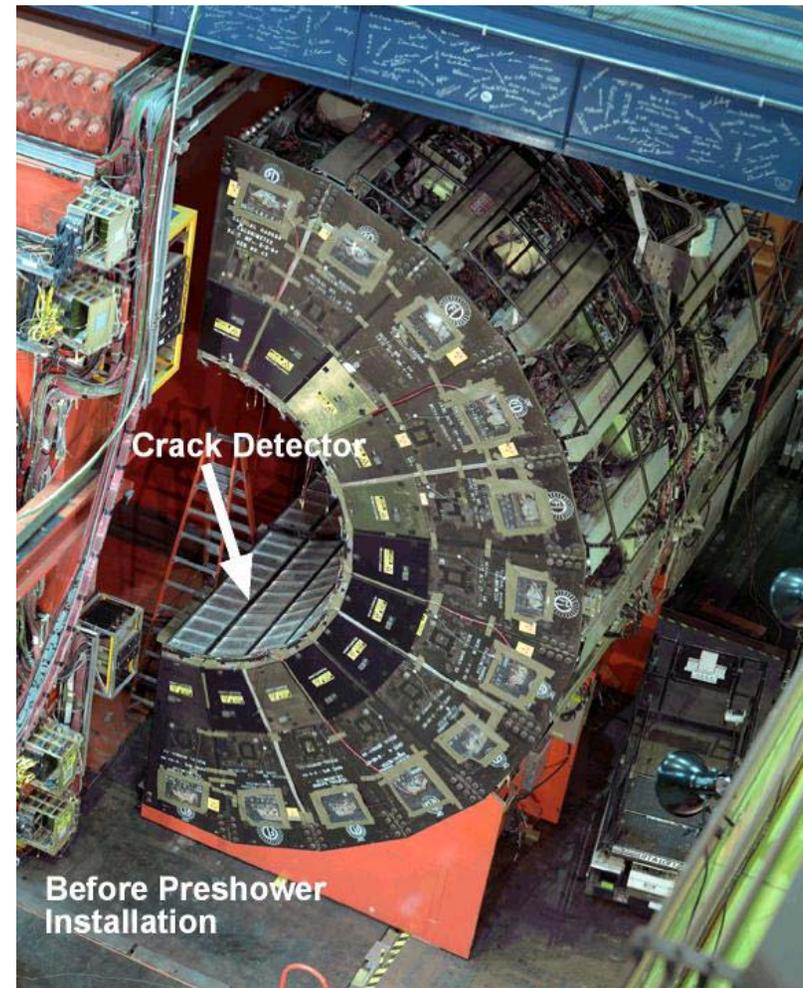
Run IIb Project Scope

- Calorimeter Upgrades
 - Preshower Upgrade
 - Electromagnetic Timing
- Data Acquisition and Trigger Upgrades
 - TDCs for the drift chamber
 - Level 2 Decision crate
 - Fast track trigger Upgrade
 - Event Builder Upgrade
 - Level 3 computer upgrade
 - Silicon Vertex Trigger upgrade



Preshower / Crack Detectors

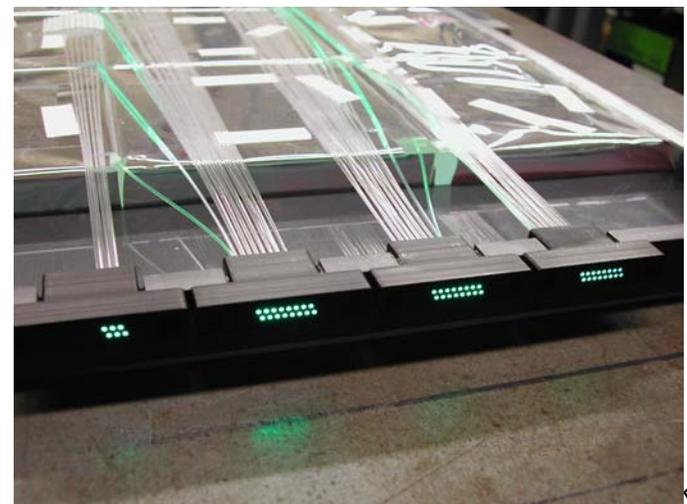
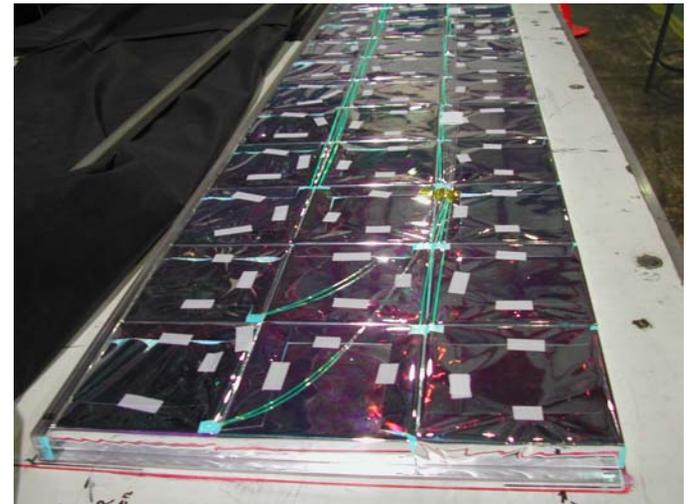
- The preshower upgrade replaces the older gas chamber system with scintillator.
 - Fiber/multichannel PMT readout – similar to what's used on the endplug.
- Significant foreign contribution here
 - PMT from Japan
 - Scintillator/fibers from Italy





Preshower Upgrade

- System was planned for an assembly hall installation in FY 2006
- Schedule was adapted to accommodate accelerator shutdowns
 - Accelerated production of scintillator tiles, modules
 - Procurement of PMTs by Tsukuba was advanced
 - The project targeted Fall 2004
 - Shutdown for 2005 projected to be shorter





Calorimeter Installation

- Preshower installation involves detector installation on the inner surface of the calorimeter
 - Never serviced in the collision hall previously.
- Phototube and cables are installed on the back.
- All parts but optical fibers were available by Sep. 2004



- All scaffolds, detector elements, people, passed through this opening.



Preshower / Crack Installation



Stefano Moccia



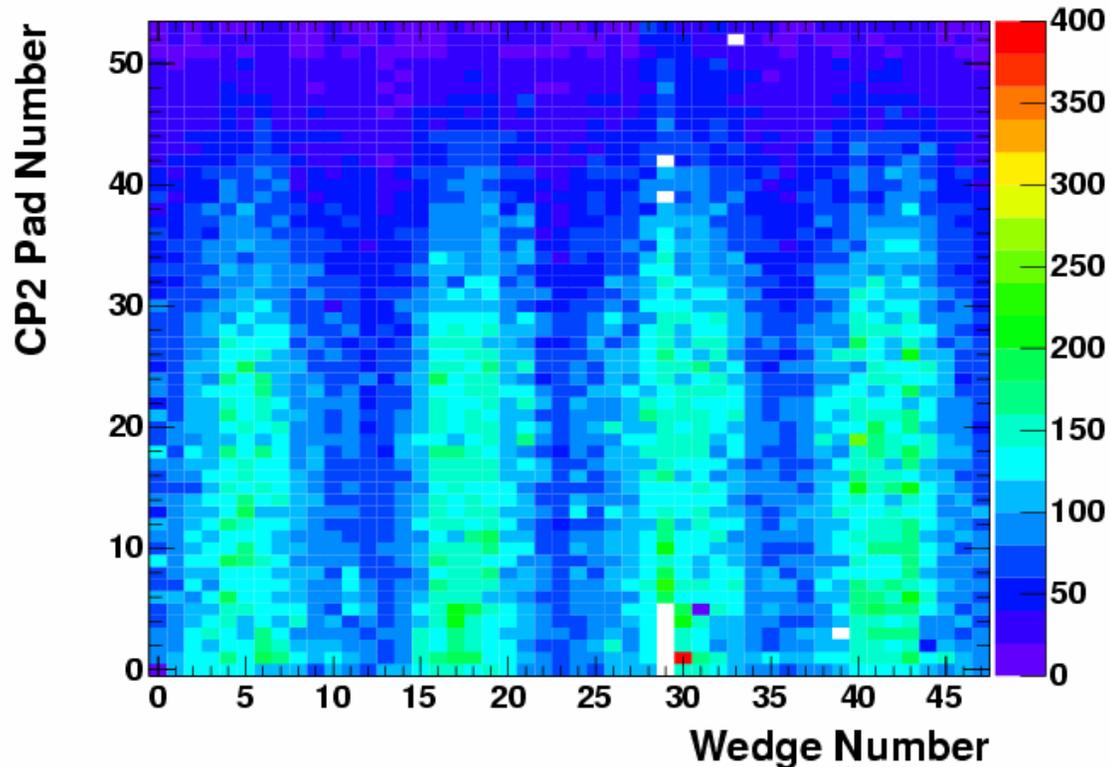
Installation Complete

- The fourth arch was replaced into operating position on 8 Nov. 2004. All front face work is done.
- The CPR is now being incorporated into the full data stream
 - Tile response measured at Argonne, PMT gain measured at Tsukuba
 - Light yield is well above the specification.
 - Gains are well understood at this stage – 13% spread
 - CPR is 99.7% live. Remaining problems are electronics
- The system is installed and working



CPR occupancy

CP2 Pad Hits



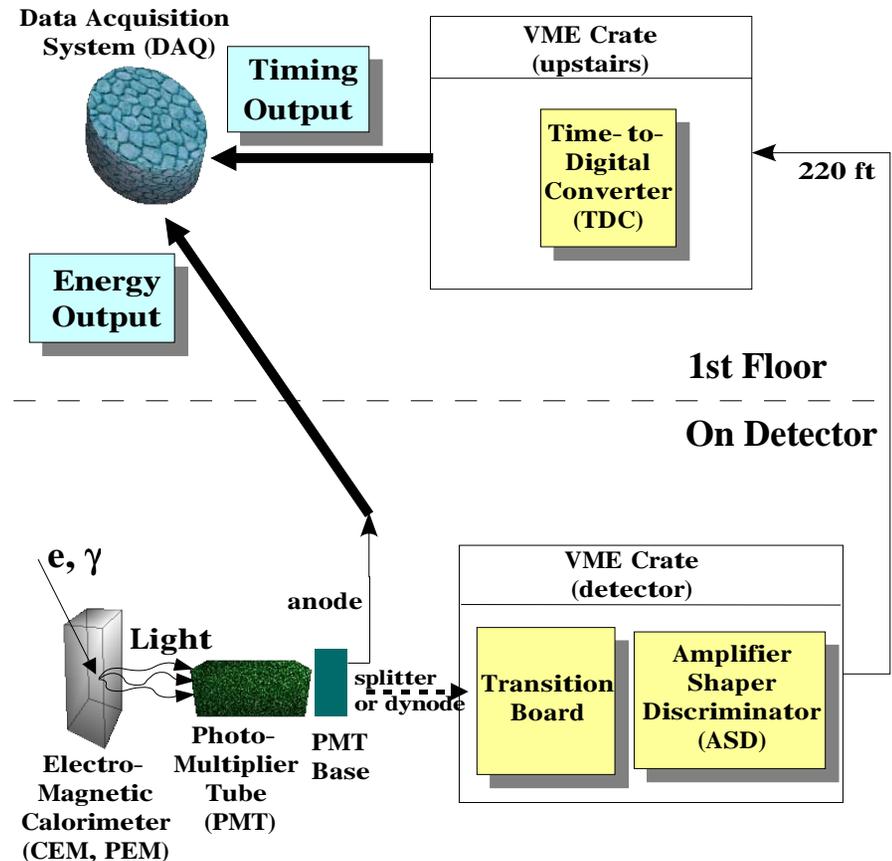
- A cosmic ray run of the CPR system



EM Timing

- The electromagnetic timing upgrade splits a small portion of the phototube signal off for timing
 - Reduces cosmic ray or halo backgrounds for photons
- Entire system was installed during the fall 2004 shutdown. Cosmic ray commissioning is in progress.

CDF EM Timing Project





DAQ/Trigger Specification Run IIa vs IIb

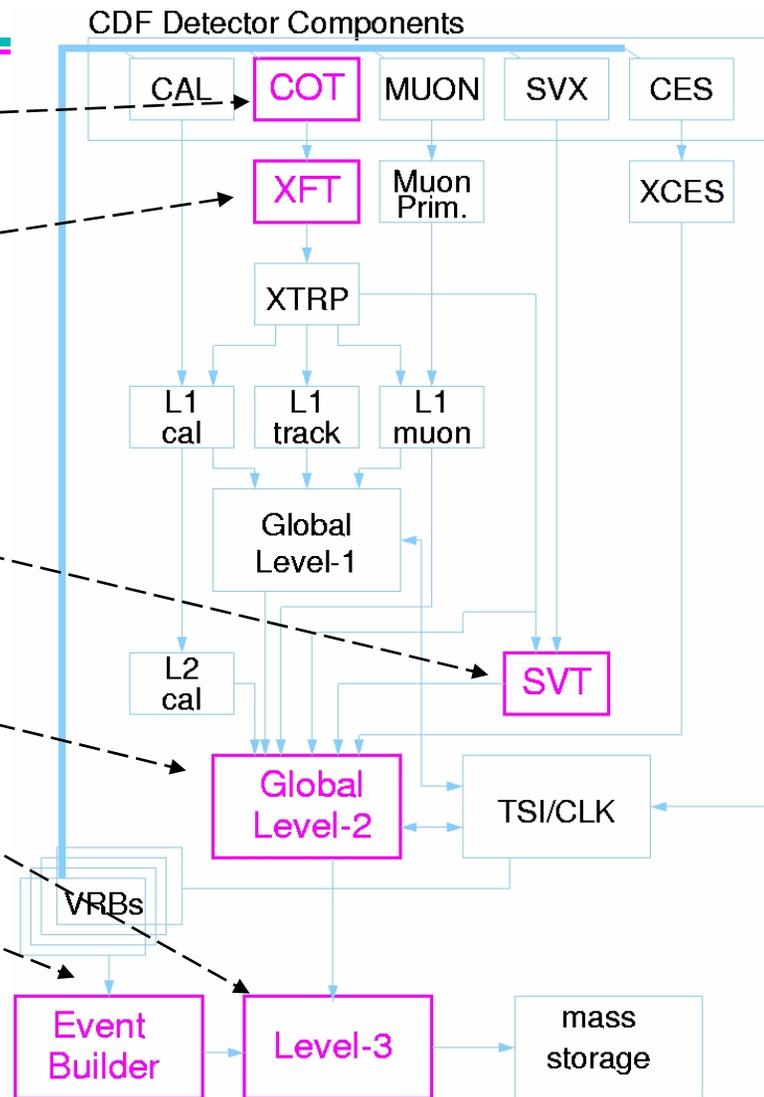
	Run IIa Specification	Run II Achieved	Run IIb Specification
Luminosity	8.6×10^{31}	1×10^{32}	3×10^{32}
L1 Accept	45 kHz	25 kHz	30 kHz
L2 Accept	300 Hz	400 Hz	1000 Hz
Event Builder	75 MB/s	75 MB/s	500 MB/s
L3 Accept	75 Hz	80 Hz	100 Hz
Rate to Storage	20 MB/s	20 MB/s	40 MB/s
Deadtime Trigger	5%	10%	5% + 5% †

- Run IIa L1A not achieved due to higher than specified Silicon Readout + L2 Trigger execution times
- † Assume ~5% from readout and ~5% from L2 processing
- Reminder: IIb trigger & bandwidth rates estimated based upon Run IIa, significant underestimate possible (assumes linear growth in fake contribution)



Trigger/DAQ Upgrades for Run IIb

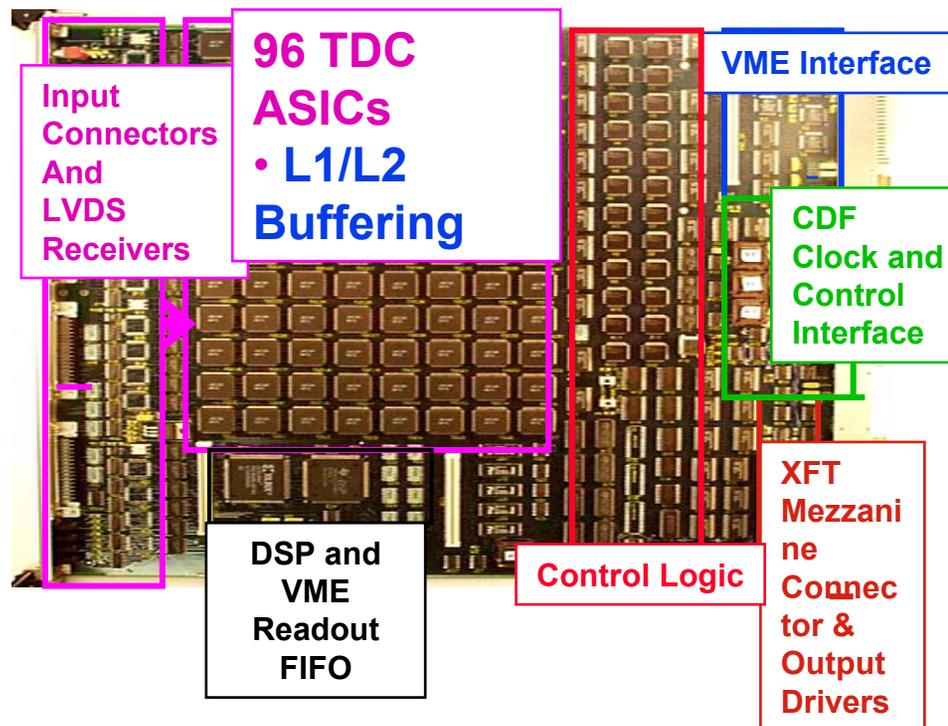
- COT TDC upgrade
 - Original readout rate insufficient
- COT Track Trigger Upgrade
 - L1 trigger rate reduction needed
 - Complexity of events (occupancy)
- Silicon Vertex Trigger upgrade
 - Occupancy demands processing speed
- L2/L3 trigger upgrades
 - Processing speed/modernization
- Event builder upgrade
 - Processing speed upgrade needed
 - Level 2 accept rate is insufficient





Run IIa TDC Limitations (2002)

- On-board processing (DSP)
Time grows with # of hits
 - $t = 1200\mu\text{s/event}$ for SL1 (4 hits/ch) at $4 \times 10^{32} \text{ cm}^{-2}\text{s}^{-1}$
- VME Readout
 - Read sequentially by one block transfer (~14MB/s at high lum.)
- VME – Event builder link limited to 12 MB/s
- 2002 Internal review recommended replacement





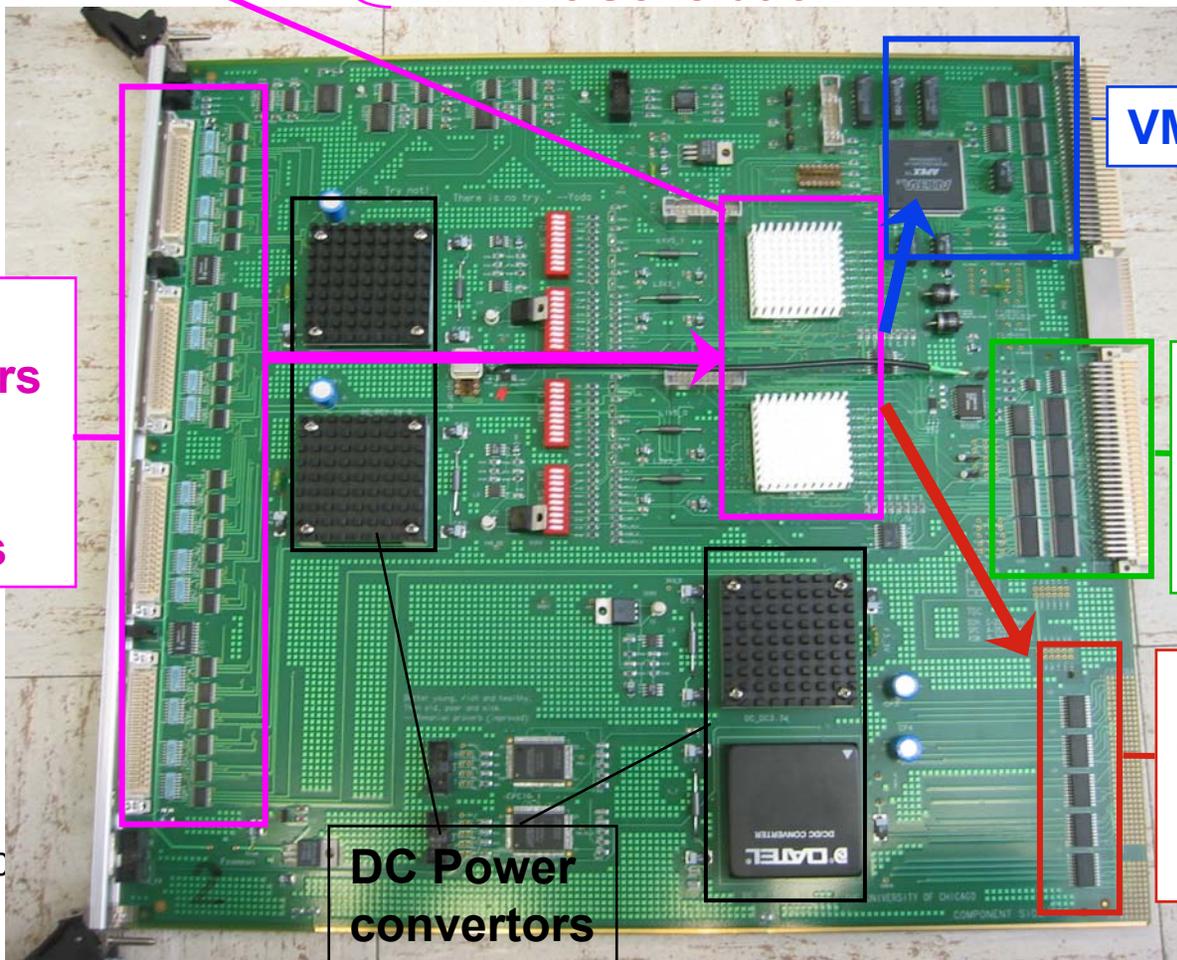
Run IIb TDC

840MHz Diff LVDS inputs

TDC: Serial to 10bit parallel conversion (1.2ns/bit)
L1/L2 Buffering, hit processing + Readout (CBLT)

XFT Hit Generation

Altera Stratix FPGAs
(48chan/chip)



VME Interface

Input
Connectors
And
LVDS
Repeaters

CDF
Clock and
Control
Interface

Trigger
Output
Drivers
(to XFT)

DC Power
convertors



TDC Performance Reviews

- Run 2a TDC
 - DSP execution now about factor of 2 faster than in 2002
 - New compressed data format (based in Run 2b TDC), halves the data volume.
 - Measured performance with 3 hits/channel of 5% deadtime at 1kHz
 - Need to implement Fast Clear on TDCs in SL5,6 (already on SL1-4) to keep these from taking longer than SL1
 - **Meets the Run 2b readout specification**
- Run 2b TDC
 - 5 preproduction boards received in September pass tests
 - Implemented 64 bit VME transfer (was 32bit like rest of FE/Trig)
 - In bench tests 18MB/s (32bit VME) → 36MB/s
 - Can achieve 2kHz with less than 5% deadtime
 - **Exceeds all Run 2b specifications**



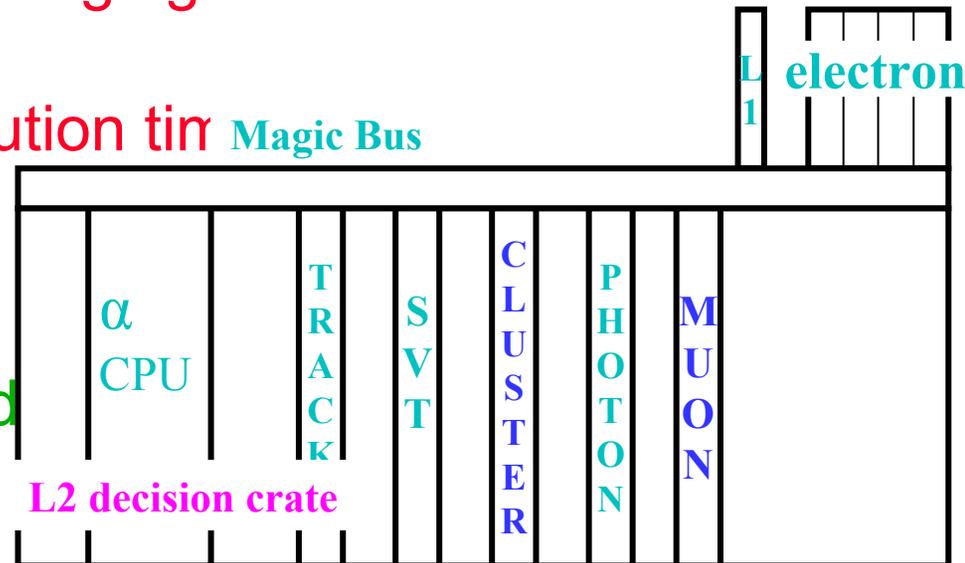
Future TDC Plans

- The review committee recommended retaining the current TDCs for the remainder of the run
- This was motivated by the perceived risk associated with commissioning a new system
 - Installation time will require an 8 week shutdown, followed by commissioning period during Tevatron operations.
- Some modifications of the current TDCs are needed (outer layer modules),
- Final testing of new TDCs will document their performance.



Run IIa Level 2 Decision Crate

- 6 flavors of interface board
 - (XTRP,SVT), L1, ISO, MUON, CES, Cluster
 - each uses different input format, different board designs
- 1 board with Alpha processor for L2 processing/decision
 - system designed to run with 4 Alphas
 - Data input with custom bus (MagicBus)
- Diversity makes system challenging to test & maintain
- DEC α processors obsolete
- Did not achieve design execution time
- CDF internal review recommended replacing Alphas for Run IIb
- Upgrade with PULSAR board as universal interface



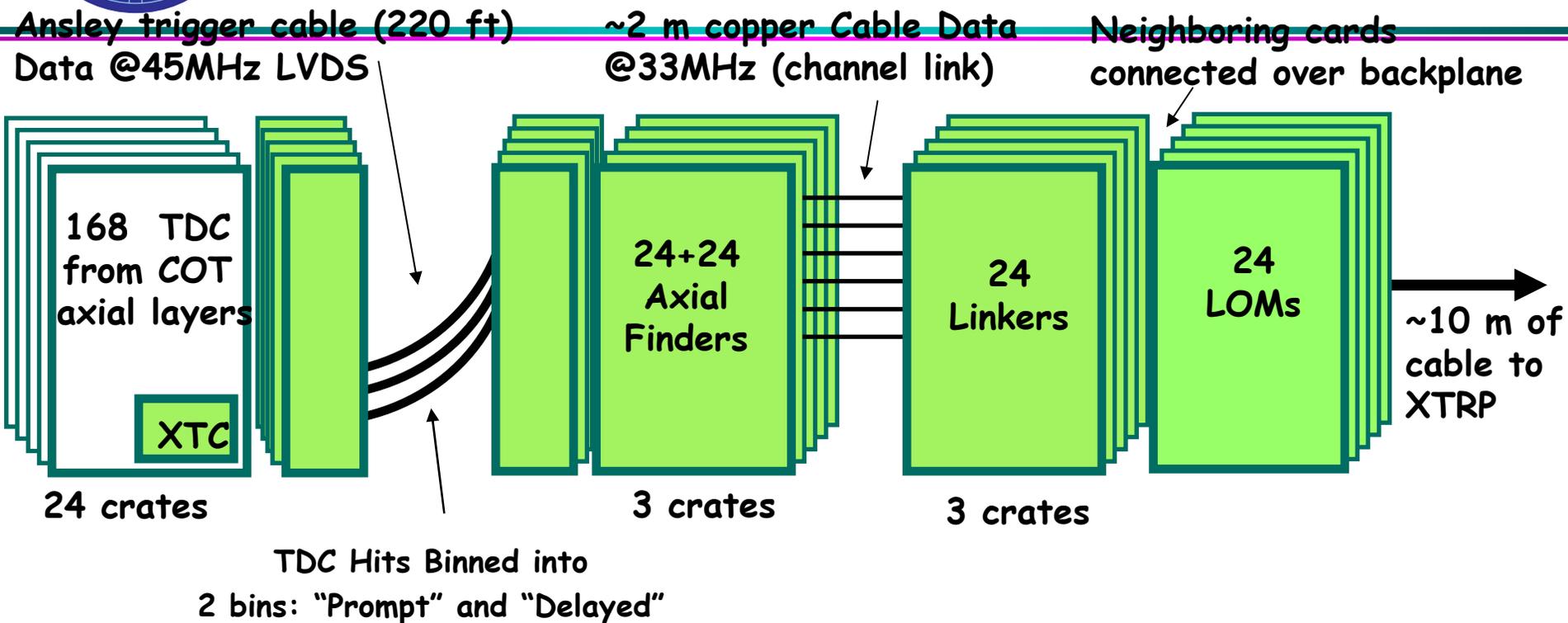


Level 2 Status

- All hardware has been procured for the Level 2 upgrade.
- Testing with beam occurred in summer 2004
 - Parasitic operation, trigger decisions, can be tested without disruption of operations
- Installation review in Sep. identified the “to do” list
- Expect system to be in full operation by March 2005.

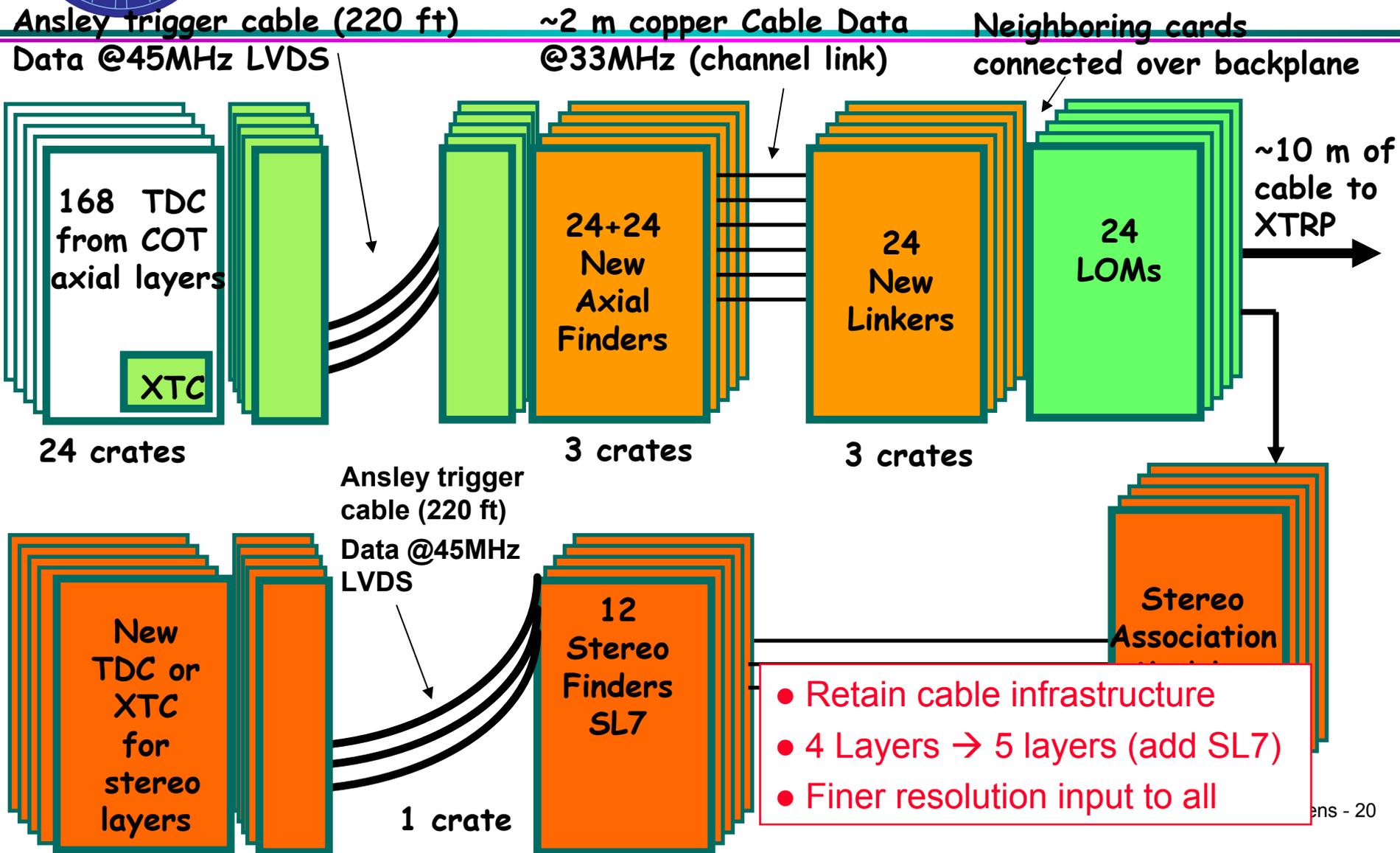


Run IIa XFT Configuration





Original XFT Upgrade



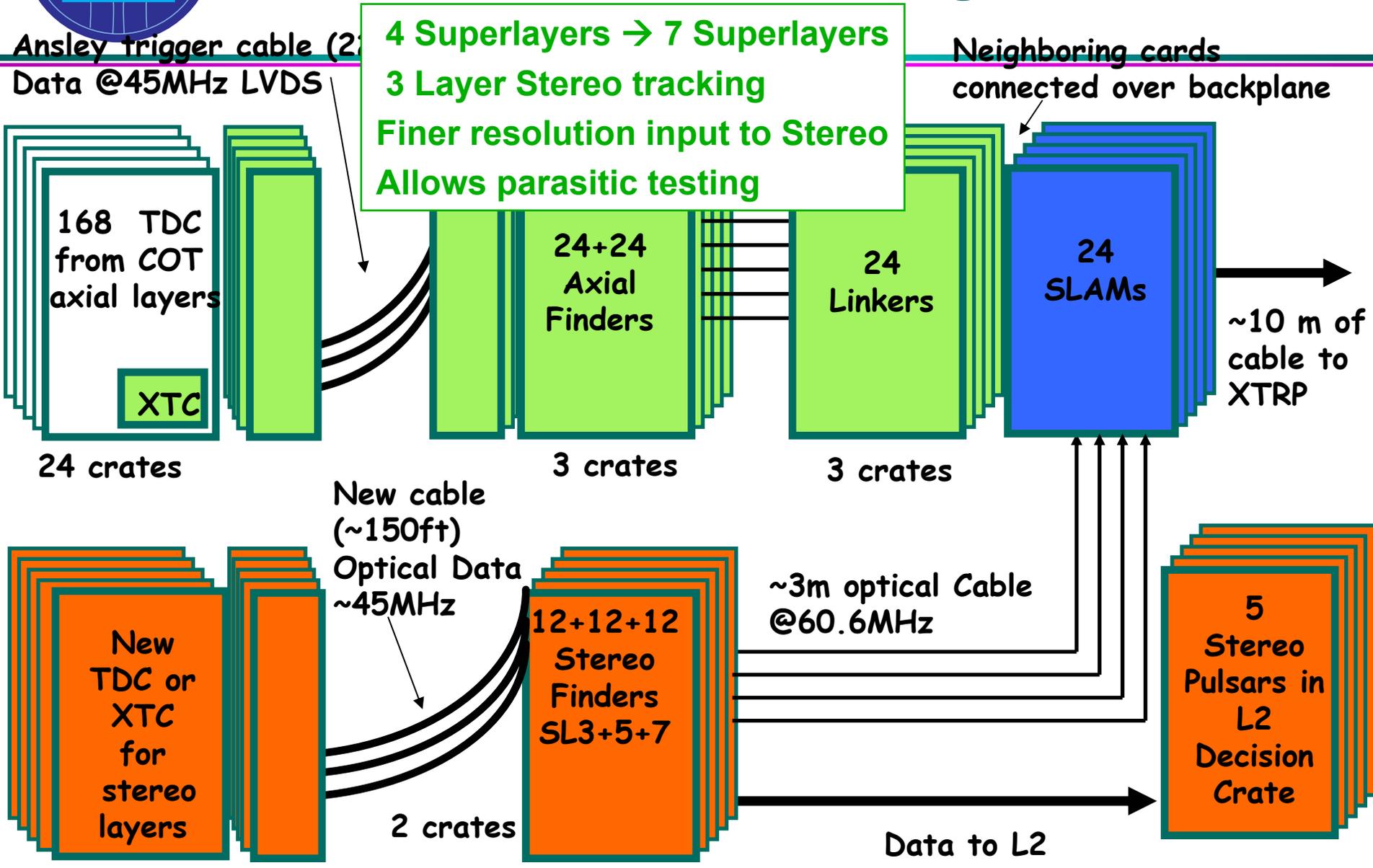


XFT II Scope Reviews

- Two CDF reviews (5/21 and 6/21) to evaluate performance and scope of the XFT upgrade and recommend course of action.
 - Hardware progress was slow
 - Not enough good Ansley cables (TDC to XFT) to instrument stereo SL7
- Significant progress in simulation since Fall 2003.
 - Reproduces trigger rates of recent higher luminosity operation
 - Performance degradation of IIa system smaller than original projections
- Committee Conclusions
 - Simulations demonstrate that original XFT upgrade can achieve goals
 - However, original XFT upgrade no longer feasible, given the time available to complete and commission the project.
 - Consensus (Committee, XFT proponents, Run IIb management) that addition of more stereo (SL 3, 5 and 7) is the most reasonable course.



Revised XFT Upgrade





XFT Hardware Progress

- Prototype XTC under test at Illinois and FNAL since July
 - Tested w/2 time bin and 6 time bin firmware
 - Production review Nov 12
 - Start fabrication by December
- Prototype TDC transition board and fiber transmitter mezzanine card (Illinois) under test at Illinois
 - Mezzanine card also used on finder for SLAM and L2 connections
- Target data for completion is the August, 2005
 - These components require collision hall installation

Stereo XTC Card - Illinois





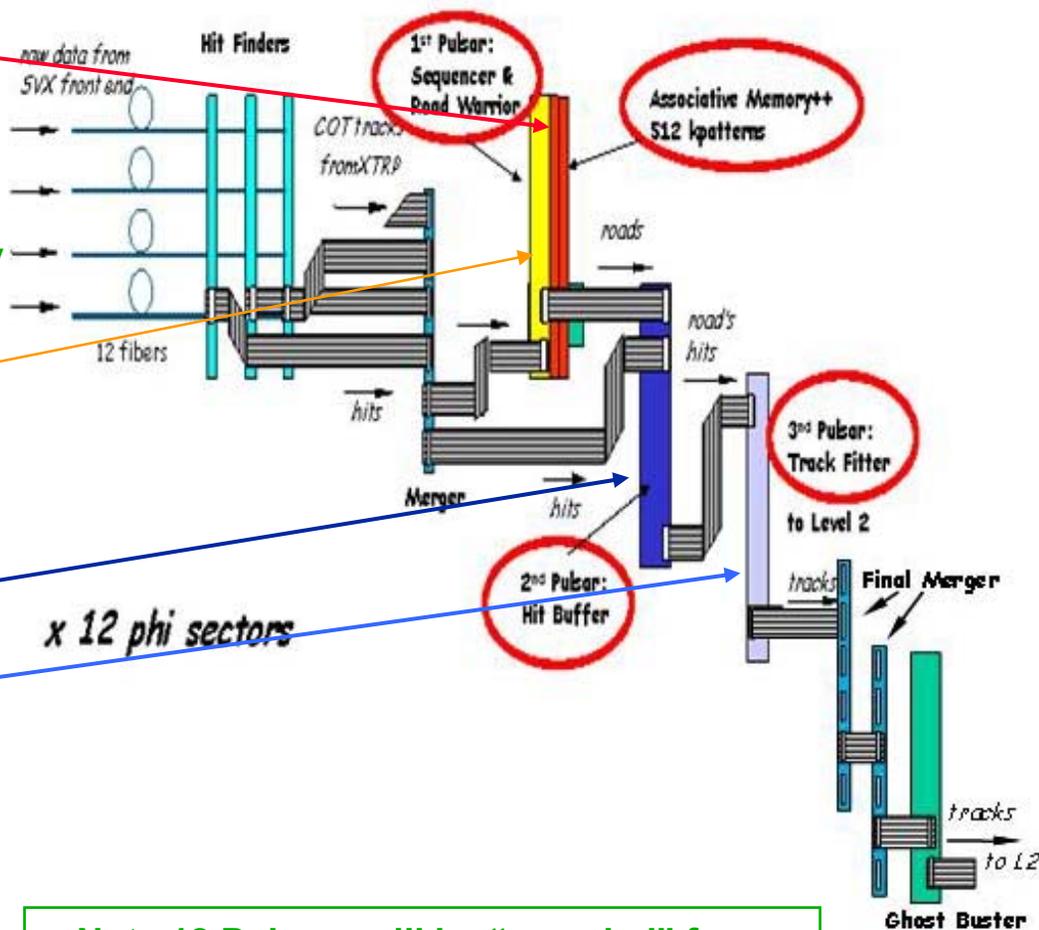
XFT Hardware Progress

- Stereo Finder (Fermilab)
 - Schematics and layout complete, design review Nov 5
 - Parts in hand, out for fabrication/assembly by Dec 1
 - Most functionality for Finder FPGA firmware complete
- Stereo Linker Association Module (SLAM - OSU)
 - Schematics and layout complete, design review Sept 24
 - Parts ordered, Out for fabrication this week
 - Implemented “Pass-through” firmware
- These items are in the counting room
 - Commissioning can be largely parasitic to operations.



SVT Upgrade for SVXII

- New **AM++** hardware with narrower roads (32K to 512K) reduces number of tracks to fit
 - Developed by Pisa, bought by INFN
- New **AMSequencer/Road Warrior** (12 Pulsars)
 - Interface for AM++
- New **Hit Buffer** (12 Pulsars)
- Faster **Track Fitters** reduce processing time on found roads (12 Pulsars)



Note 12 Pulsars will be “recycled” from current use as “Road Warrior” boards



SVT Progress

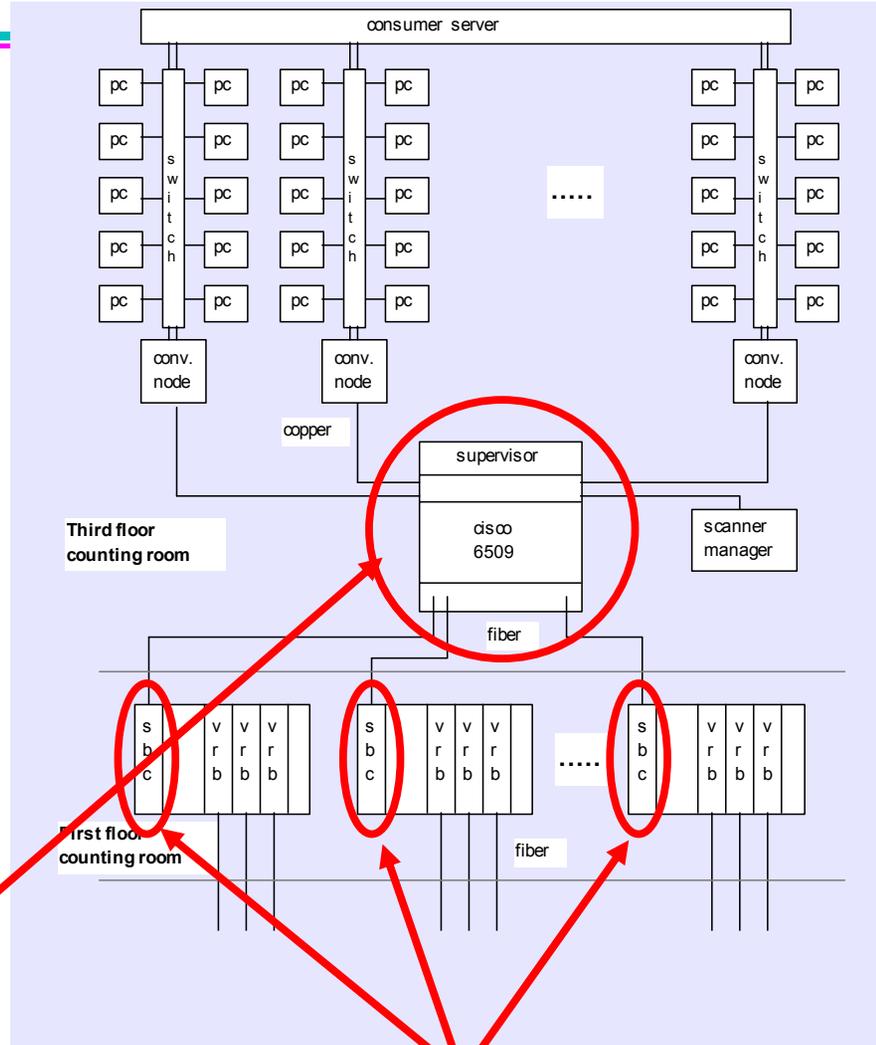
- AM++ (not on project funds) at INFN
 - Testing of new AM chips progressing - Low yield may require an additional production run. Should not be a significant project delay.
 - AM++ and LAMB mezzanine boards passed printed circuit board review Nov 3.
- Hardware for AMS/RW, HB, TF defined:
 - Quote request for 34 Pulsar boards (includes XFT) issued by Chicago
 - Design of two 2 Pulsar mezzanine boards (memory) at Chicago
 - First passed design review Nov 2, prototype parts in hand, board fabrication in progress
 - Design of second started should be ready for prototype by end of 2004
- Firmware making good progress
 - AMS/RW firmware making good progress at Pisa
 - TF firmware largely transferred from existing design to Pulsar
- Note, this installation is decoupled from collision hall access.



Run IIb Event Builder Upgrade

	RunIIa	Run IIb
Rate:	300Hz	1kHz
Event size:	250kB	500kB
Throughput:	75MB/s	500MB/s

SCPU:	MVME2600	VMIC7805
SCPU OS	VxWorks	Linux
Switch:	ATM	Cisco 6509 (gigabit ethernet)



new Cisco 6509 switch

new software (much less than IIa)

new VMIC 7805 boards (SCPUs)



Event Builder

- Hardware in hand (ahead of schedule)
- Software development and testing on schedule for installation in Aug 05
 - No collision hall access is required, but installation will require down time for the experiment.



CDF Upgrade Conclusions

- Calorimeter - **installations are complete**
- DAQ/Trigger projects are making good progress
 - New direction on TDCs – improvements in the current device and the installation risk motivate a new strategy.
 - Level 2 – entering the final integration phase
 - Track triggers (XFT and SVT) are beginning construction
 - Both have simplified their design recently
 - Event builder hardware is in hand, and software is in progress.
- All projects are targeting completion/installation by the end of FY 2005.