



DØ Upgrade Status and Plans

Mike Hildreth
University of Notre Dame

Fermilab PAC
November 12, 2004



RunIb Upgrade Status

Overview:

- Reminder of Motivation
- Trigger upgrades
 - Level 1 Calorimeter Trigger
 - Level 1 Track Trigger
 - Level 2 Silicon Track Trigger
- Fiber Tracker Electronics: AFE II
- Silicon Tracker Layer 0
- Pre-Installation Commissioning/Coordination
- Conclusions

Approved Upgrades on Schedule for 2005 installation

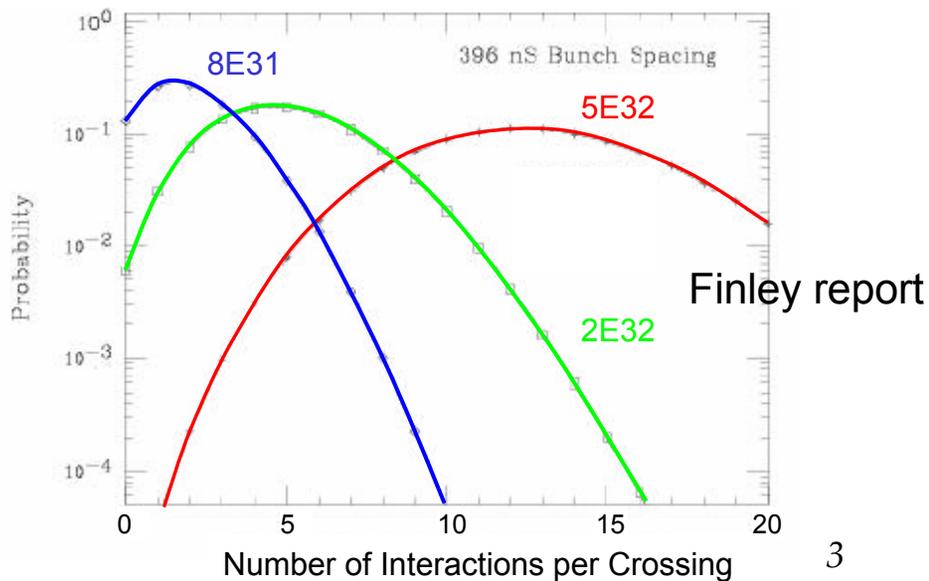
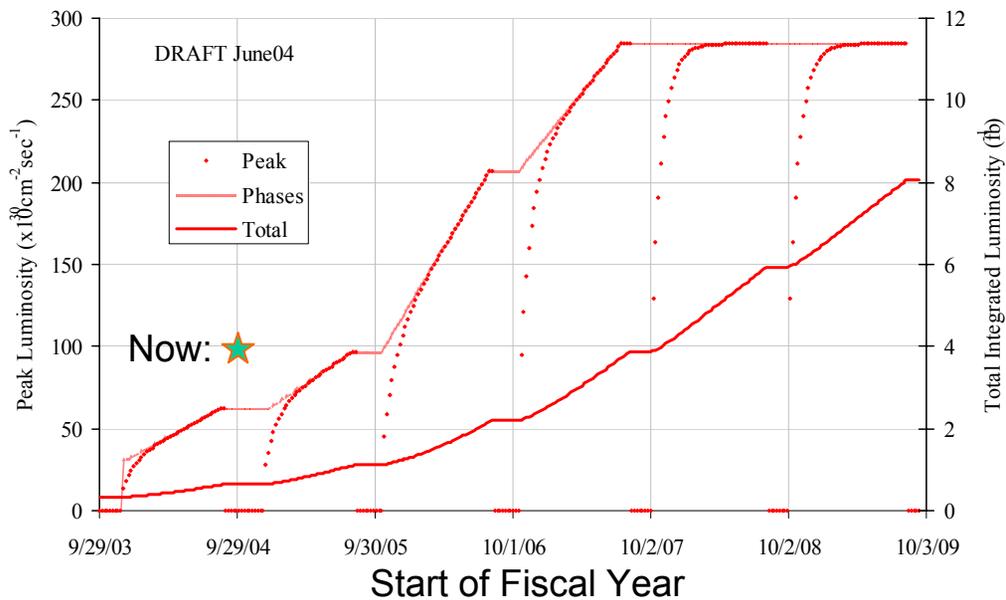


RunIIb Occupancies & Radiation

Typical peak luminosities will be three times greater than current records

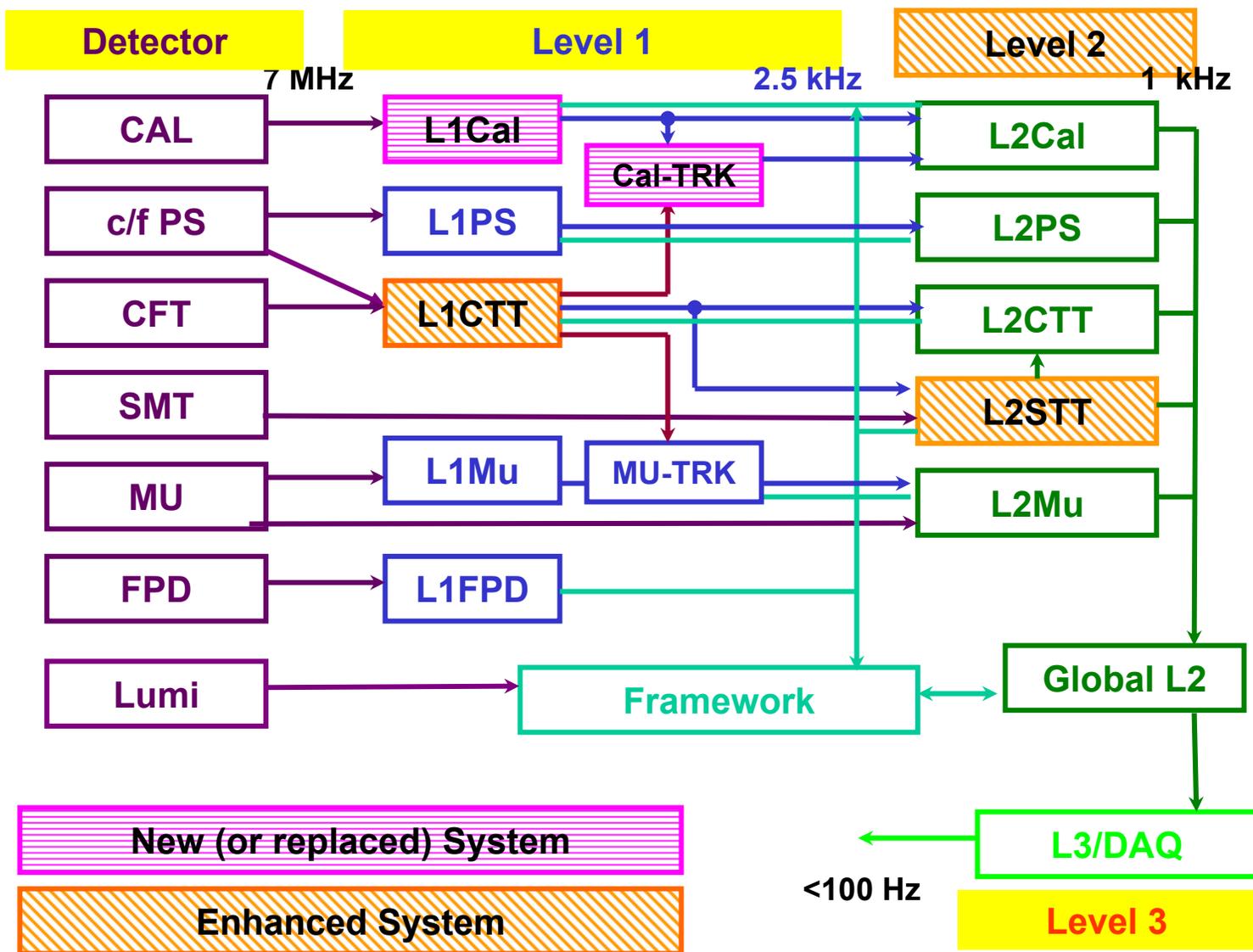
- Average of 7 interactions per crossing at 2×10^{32}
- Many trigger rates rise faster than linearly with luminosity
- Significant radiation damage to silicon inner layer expected

Upgrades designed to preserve or improve physics capabilities through the end of RunII





Trigger System Upgrades





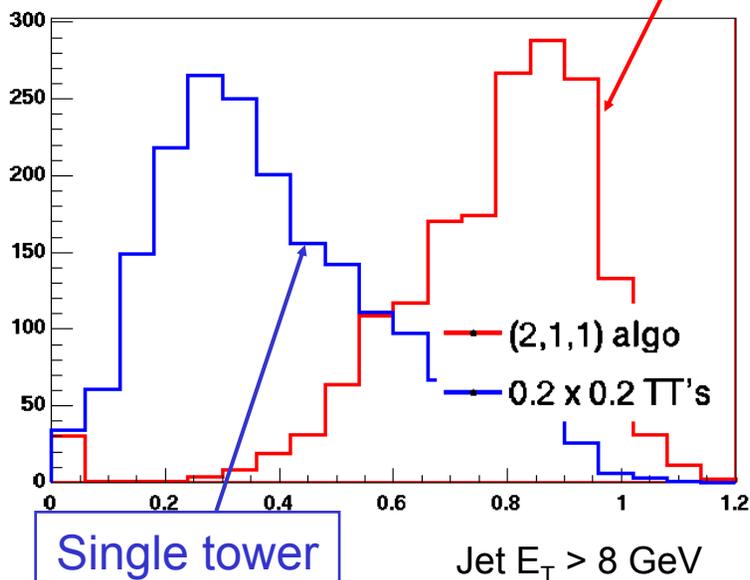
Level 1 Calorimeter Trigger

- Most extensive of trigger upgrades
 - sharpens trigger thresholds
 - more flexible: clustering, more topological cuts
- *Will require removing the existing Cal trigger*

Run IIa data

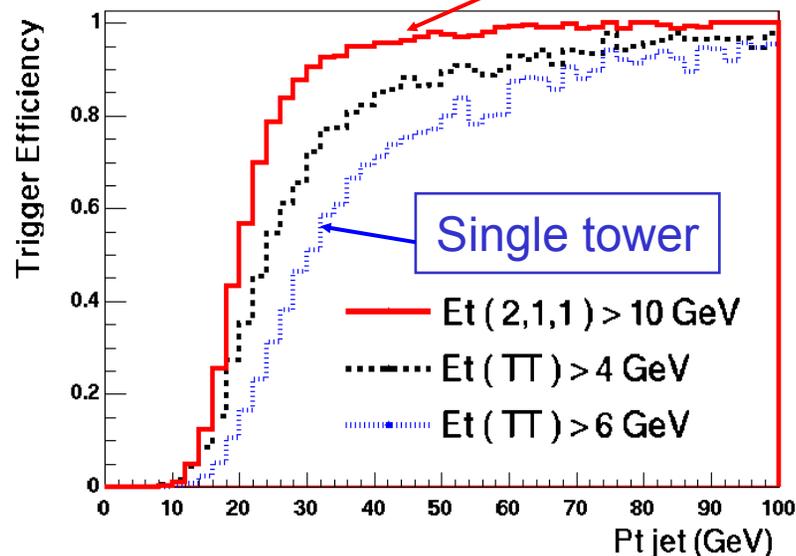
Sliding window
rms/mean = 0.2

Et (trigger) / Et (reco'd jet)



Turn-on curves : 2,1,1 algo vs current trigger

Sliding window





L1Cal Trigger Status

ADC+Digital Filtering

Finished 05/03

Clustering

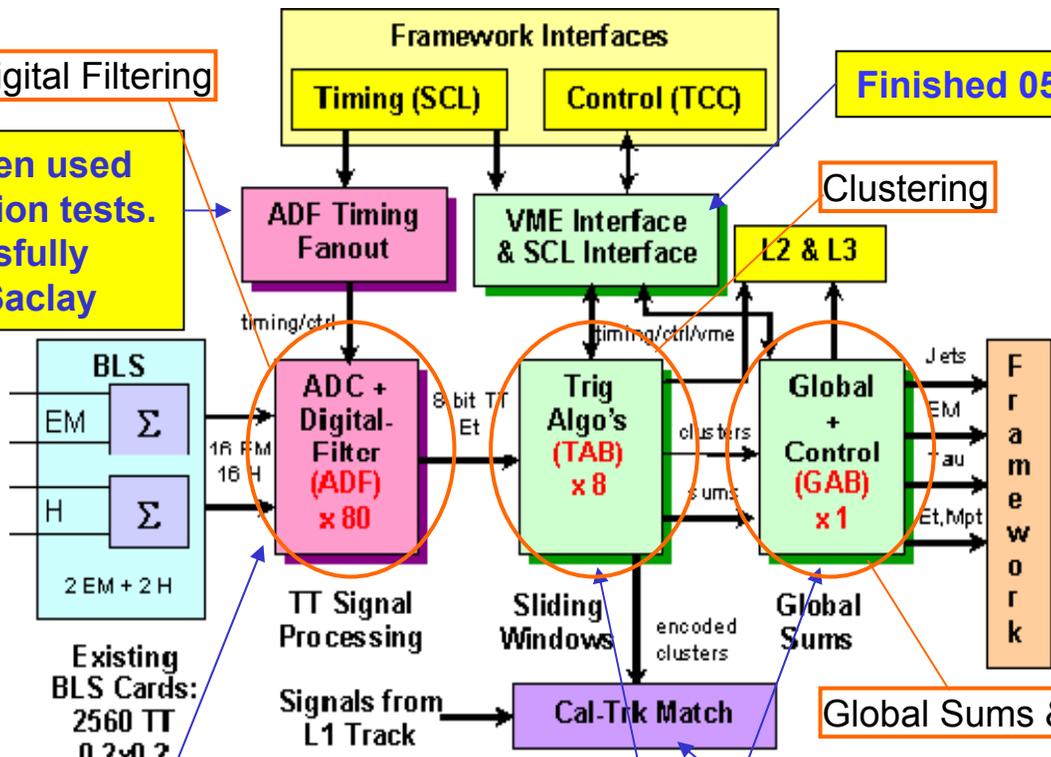
Global Sums & Topological

Production track match card fabricated and assembled, loop test established

Orders placed for all remaining TAB and GAB components. Production readiness review was October 7 – now in production

ADF v.2 layout complete, lining up vendors for pre-production run

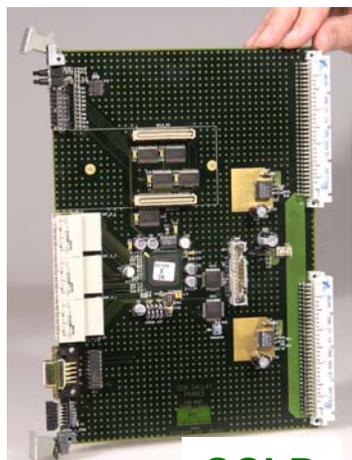
SCLD prototype has been used successfully in integration tests. Final board has successfully passed bench tests at Saclay



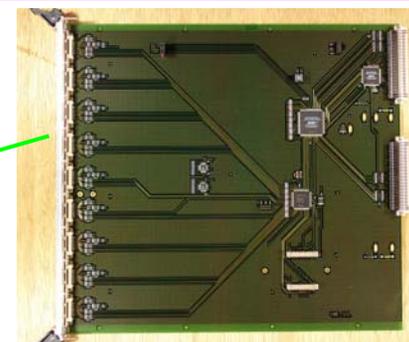
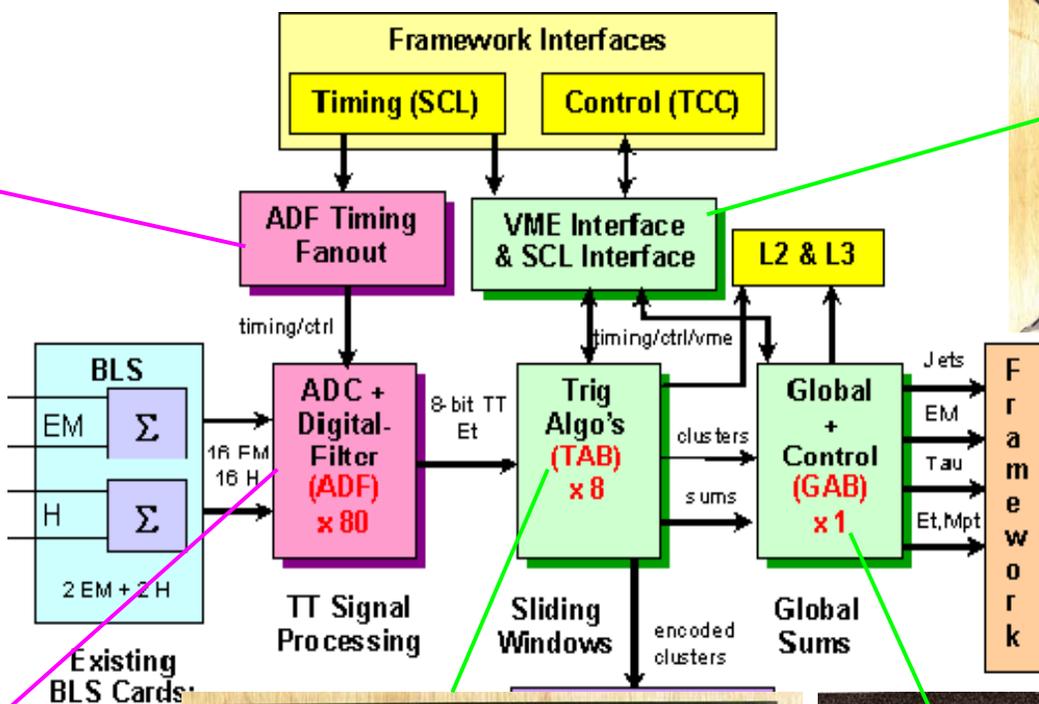
Existing BLS Cards: 2560 TT 0.2x0.2



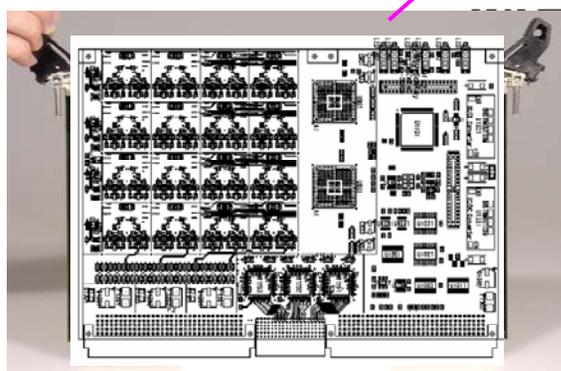
L1Cal Trigger Status



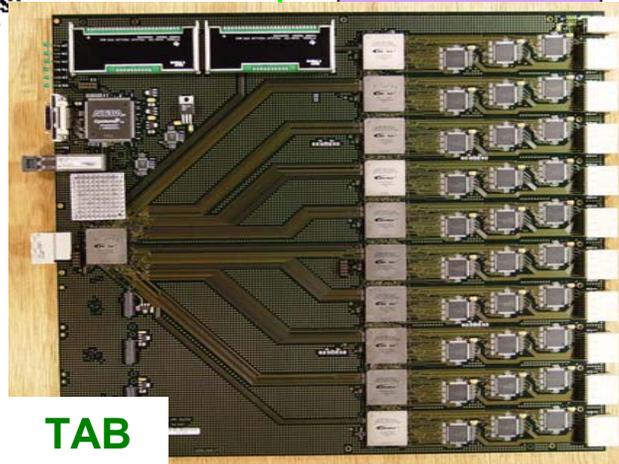
SCLD



VME/SCL



ADF v2



TAB

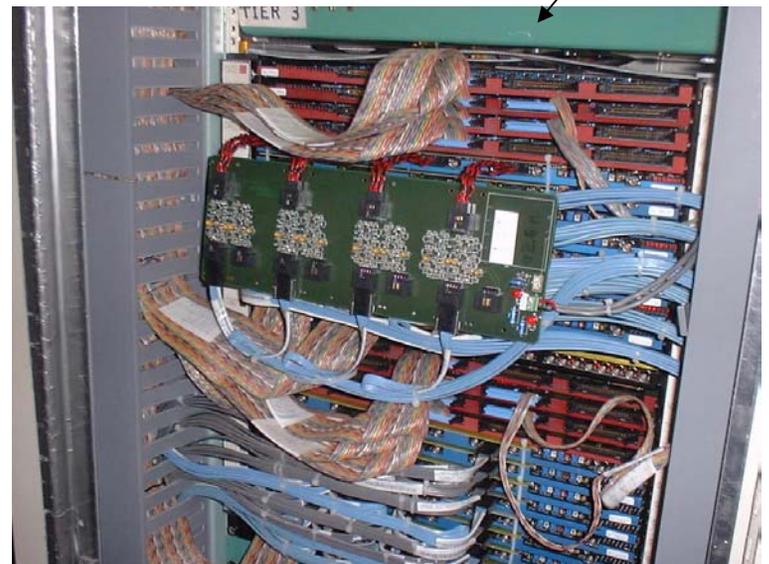
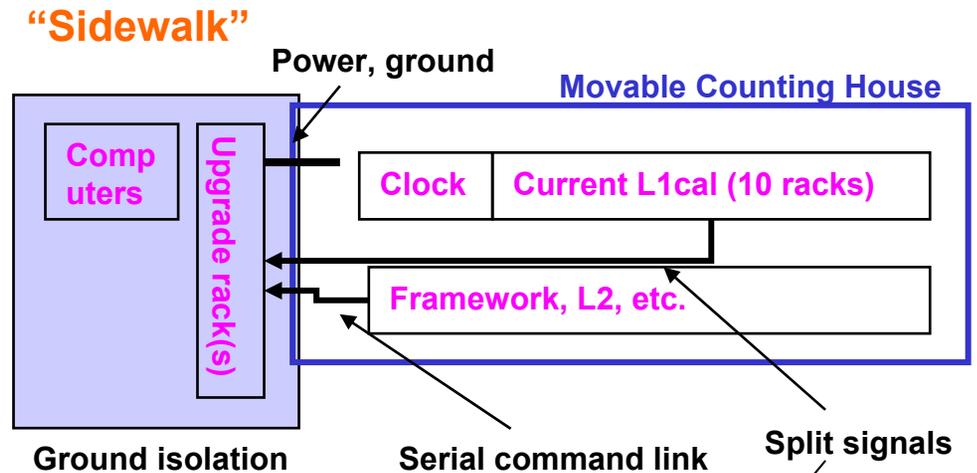


GAB



L1Cal Commissioning

- Signal splitters allow digital filter and entire readout chain to be tested with full system prior to installation
- Currently:
 - long term data integrity transmission tests between TAB and GAB
 - TAB data transmission to L2 and L3, tests of data unpacking
 - cable tests for inputs
 - patch panels/paddle cards for installation in hand
 - cable layouts defined
- Future:
 - Collect single-tower data to tune MC
 - Test trigger generation with real data
 - Full system will be installed on sidewalk





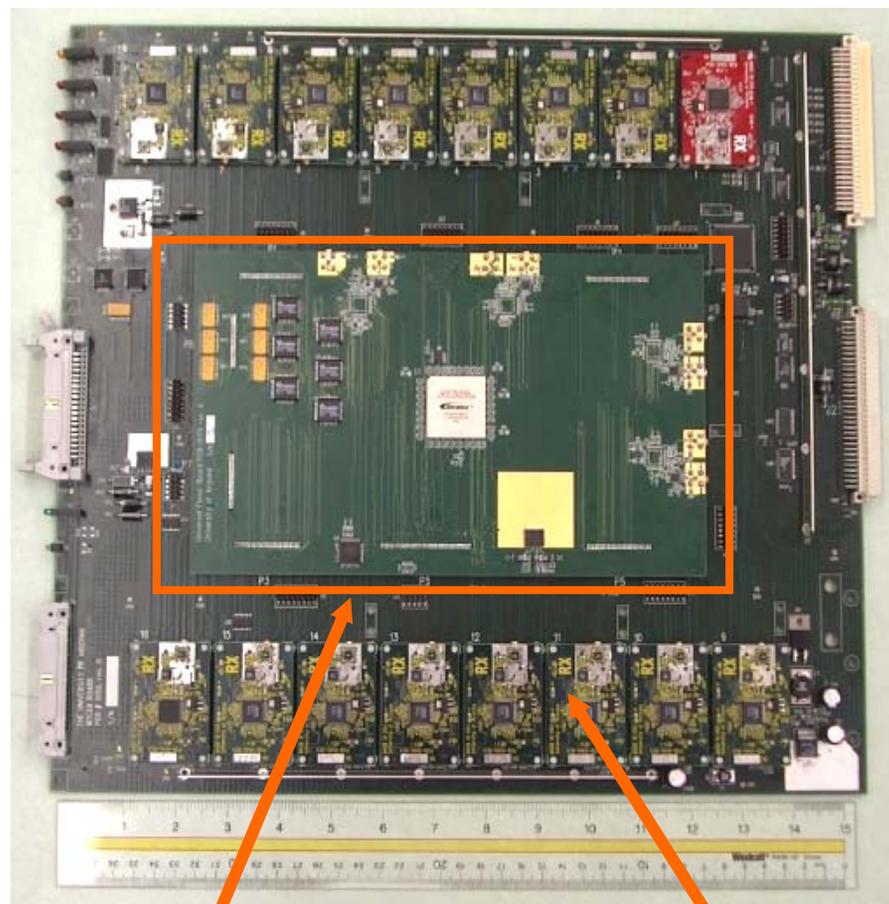
Level1 Calorimeter-Track Match

- Exploit new L1Cal trigger – early access to information
- Improve Run IIa ϕ matching granularity by a factor of 8
- Needed in triggers for Higgs searches
 - electrons in WH and $H \rightarrow W^*W$ modes
 - taus in $H \rightarrow \tau\tau$ and $H^+ \rightarrow \tau\nu$
- Fake EM rejection is improved by $\sim x2$, fake τ rejection is improved by $\sim x10$
- Modest upgrade based on existing Mu-Track match system
 - Very few changes with respect to Mu-Track



Level1 Calorimeter-Track Match

- All hardware in production or already complete
 - expect production complete by early 2005
- Commissioning:
 - VME Crates, processors already installed
 - Cables for L1CTT-L1CalTrk already installed
 - terminated during shutdown
 - System should be integrated into the experiment (test triggers, full readout chain) by the end of the shutdown
 - using spare L1Muon trigger boards for now



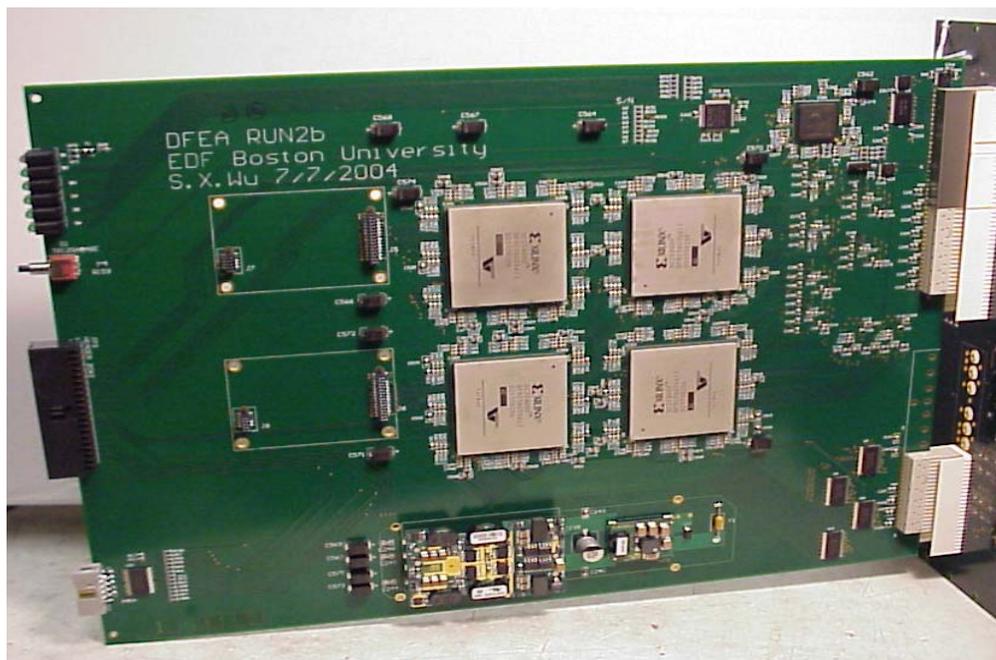
Universal Flavor board (daughter)

MTCxx (mother board)



L1 Central Track Trigger

- Level 1 Central Track Trigger (CTT) essential for electrons, muons, taus ($WH \rightarrow l\nu jj$), input for STT vertexing trigger
- Tracking trigger rates very sensitive to occupancy
- Upgrade strategy:
 - Narrow tracker roads by using individual fiber hits (singlets) rather than pairing adjacent fibers (doublets)
 - Cal-track matching



DFEA mother/daughter board redesigned as a single board (DFEB), with larger FPGA's: (Xilinx Virtex-II XC2V6000)

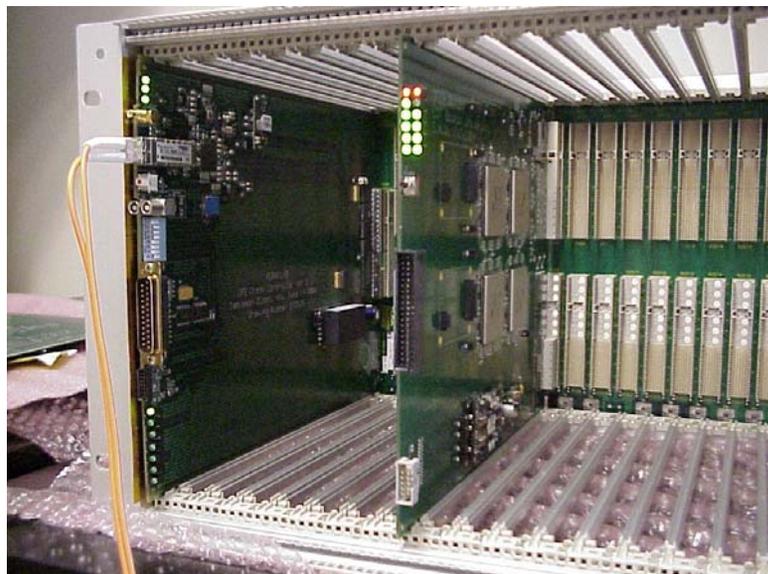


L1CTT Modifications

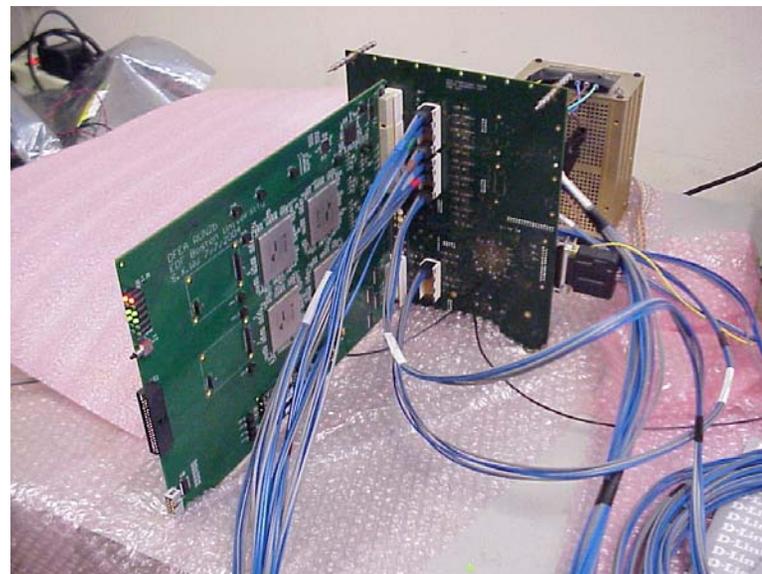
- Scope of project expanded to improve monitoring/debugging infrastructure
 - Daughtercard replaced by new mother/daughter board (DFEB)
 - additional I/O buffers for diagnostics
 - New crates/backplanes with new crate controllers (DFEC2)
 - Gbit ethernet for downloads (minutes vs. hours)
 - Minimize commissioning time (lessons from current experience)
- Status:
 - Prototypes for ALL necessary hardware in hand
 - Parallel readout chain with new crate has been installed during the shutdown to test entire trigger chain
 - splitters plus extra downstream electronics
 - will allow complete testing of algorithms/readout with real data
 - communications/readout established, testing firmware
 - On schedule for completion in Summer 05



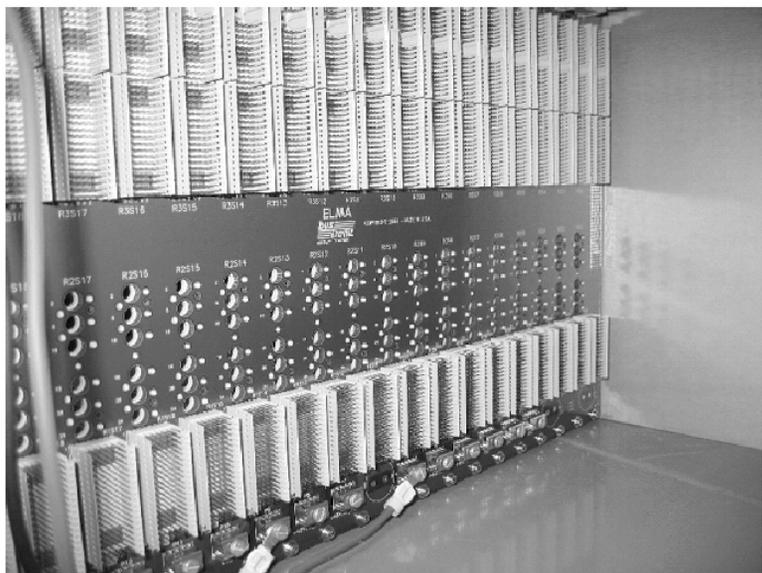
L1CTT Hardware



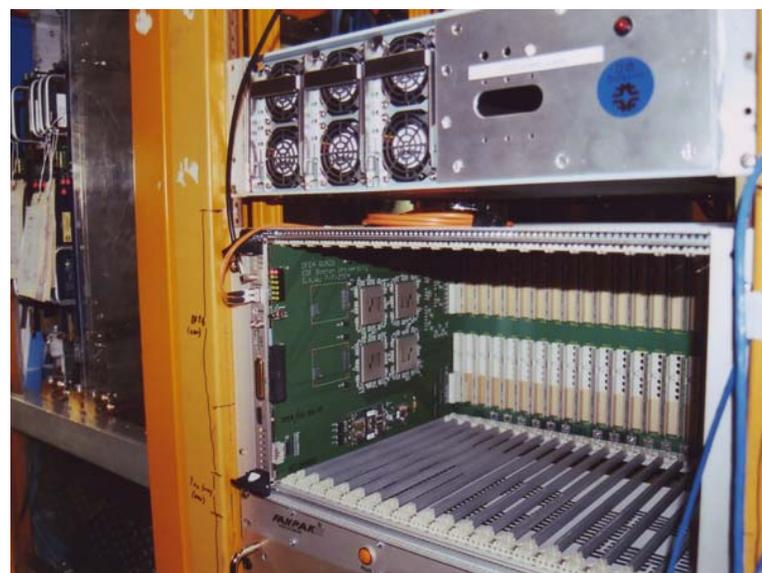
↑ New L1CTT Crate, Crate Controller, DFEB



↑ DFEB in stand-alone test setup with LVDS signals input



↑ New DFEB Crate backplane



↑ DFEB in new crate installed on the platform in DØ



STT and Level 2

- STT

- Additional production of the same boards is needed to accommodate new Layer 0 channels
- Production Readiness Review Friday Sept 10:
 - Buffer controller now in production
 - decision on building additional Track Fit Cards awaiting further study

- Level 2

- Work in July/August to get the Concurrent Tech cPCI CPU to work with the 9u motherboard
- Fallback CPU: Adlink cPCI-6860A
- upgrade to proceed adiabatically

Should be “transparent” upgrades





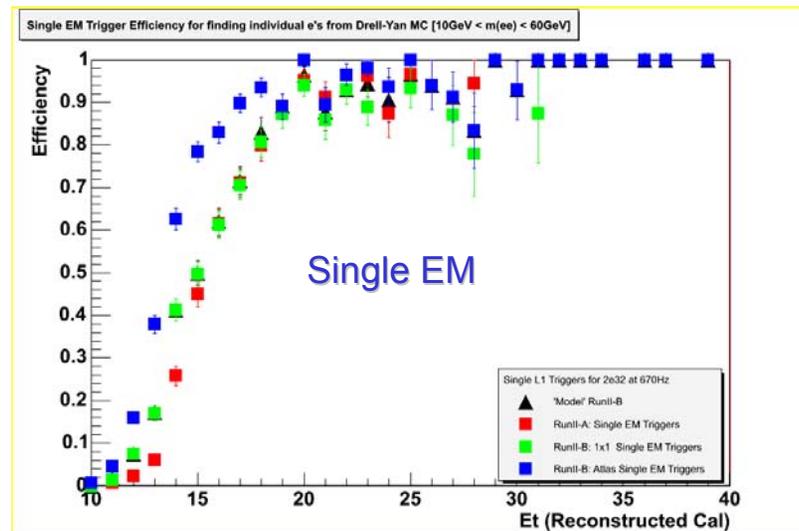
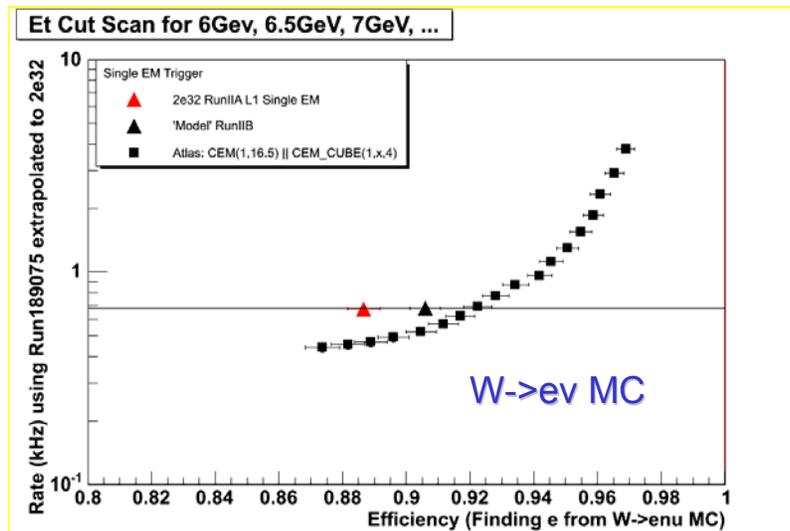
RunIb Trigger Simulation/Algorithms

- L1Cal

- variety of small variations of sliding window algorithm studied for EM triggers
- now improving upon RunIa L1+L2EM performance
- Prototype firmware versions of EM, Jet, and tau algorithms

- L1CTT

- Run Ila simulation package being restructured
 - will be much more easily adapted to Run Iib
- Firmware being tested



Greg Pawloski, Sabine Lammers



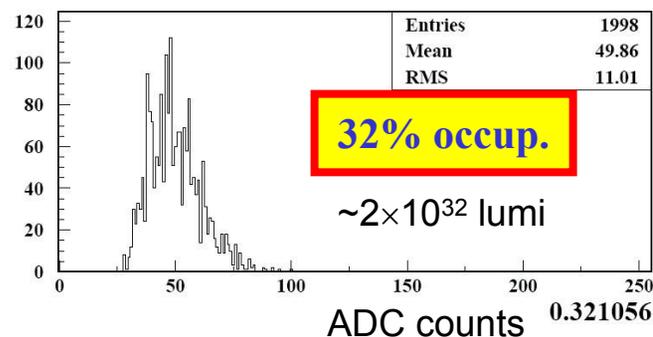
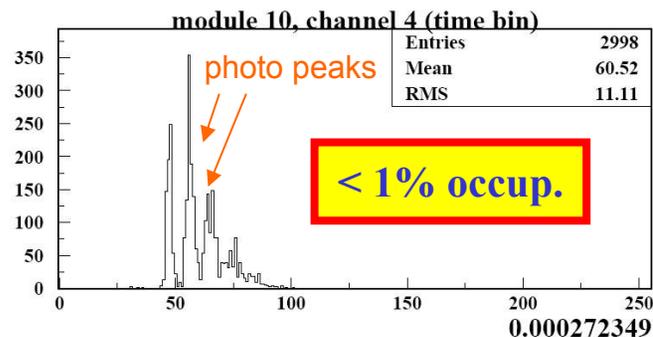
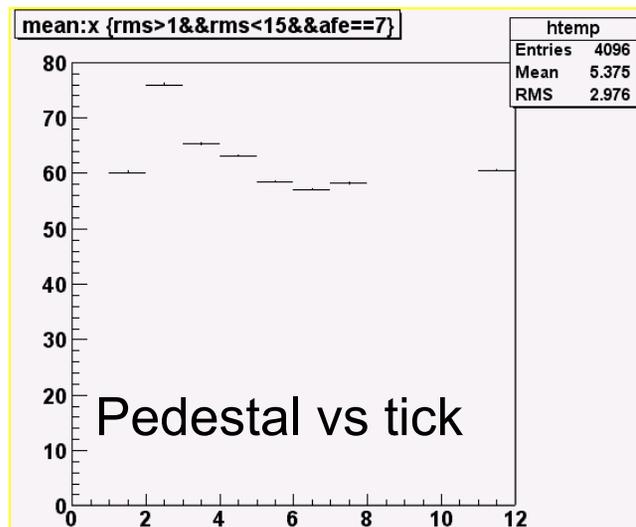
RunIb Trigger Simulation/Analysis

- Primary goal is “strawman” trigger list by early 2005 incorporating new algorithms
 - starting with current L2 trigger terms as a basis
- “trigger rate tool” adapted to implement sliding windows algorithms
 - uses real collider data as input
 - accounts for correlations and combined rates of full trigger list
- Closer coordination of effort between
 - Trigger Upgrade Project (coding new algorithms)
 - Trigger Board (policy)
 - Trigger Steering Committee (technical)
 - (new) Trigger Studies Group (physics/rate studies)
 - N. Varelas appointed Trigger Coordinator



Replacement of CFT Read-out: AFE II

- R&D is in progress for a replacement for the existing AFE CFT readout board
 - Replace SIFT/SVX II with TRiP-t + Commercial ADC
 - Gain: TRiP-t will allow timing (z information) from CFT
 - 2ns resolution → ~30cm
- Benefits
 - Lower noise → lower thresholds.
 - Stable pedestals
 - We can recover signal that would be lost at high luminosity*
 - Z information → easier pattern recognition. Decrease tracking time and maintain efficiency





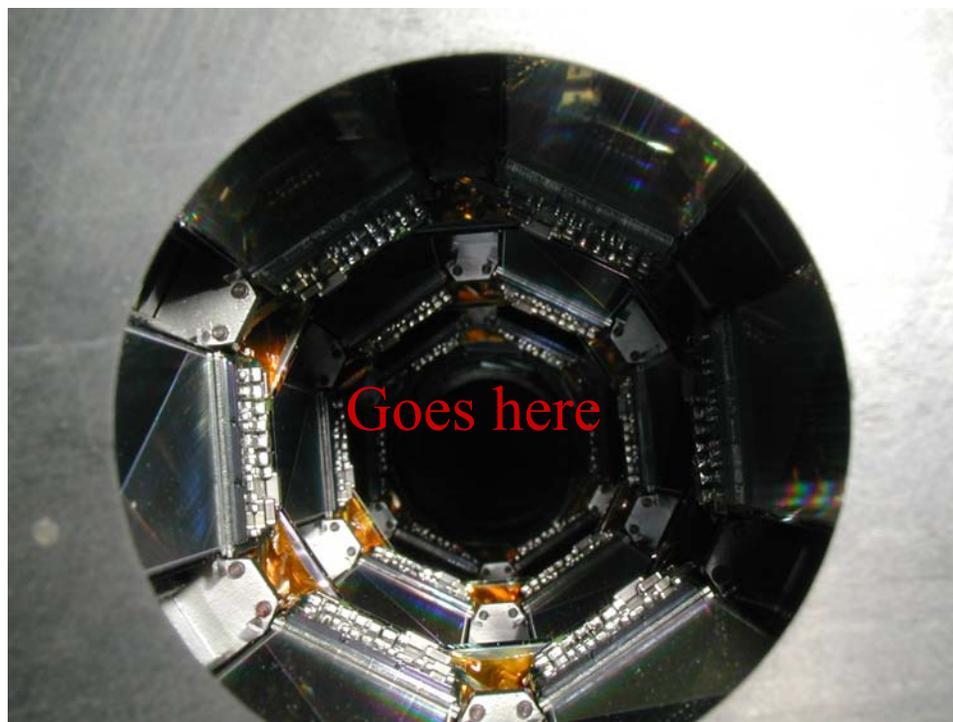
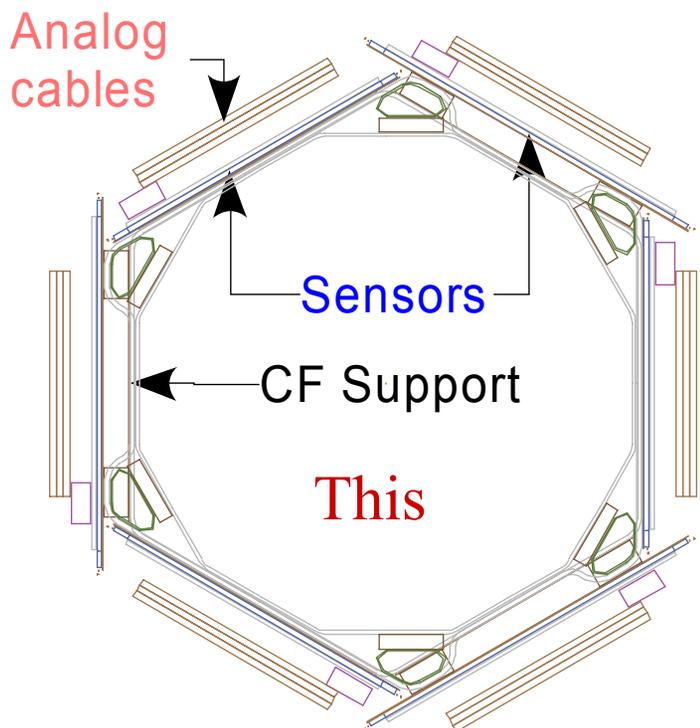
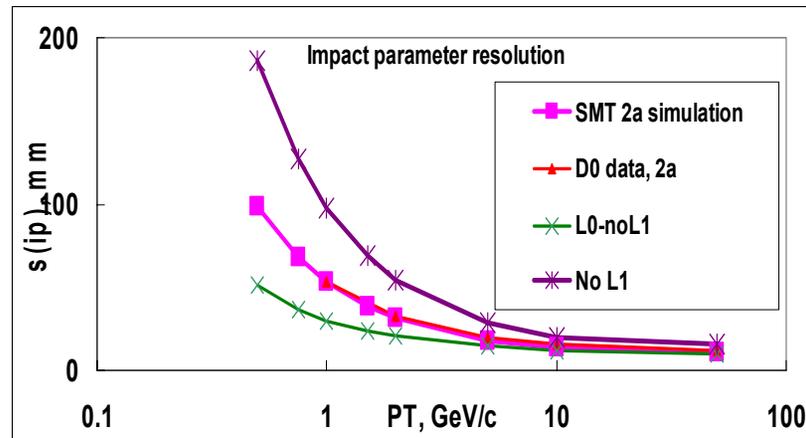
AFE II Status

- AFE II schedule has been revisited to speed things up
 - Current status:
 - AFE II prototype with TRiP (no “t”) under test
 - (same footprint as TRiP-t)
 - no major problems found
 - Mosis submission of TRiP-t is back from the foundry
 - mounted (but not packaged)
 - timing pipeline works
 - all other functions test ok
 - Fast-track decision to proceed:
 - D0 internal review 12/04 (was 1/05)
 - Laboratory review Jan/early Feb 05 (was 2/05)
(final project approval)
 - Production begins 2/05 (was 3/05)
- ⇒ Aiming for adiabatic installation starting late 2005



Silicon Tracker Layer 0

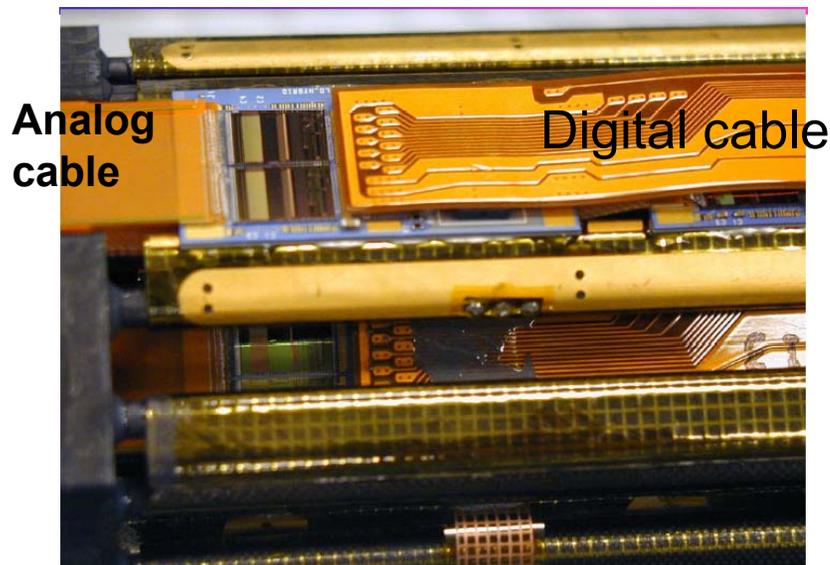
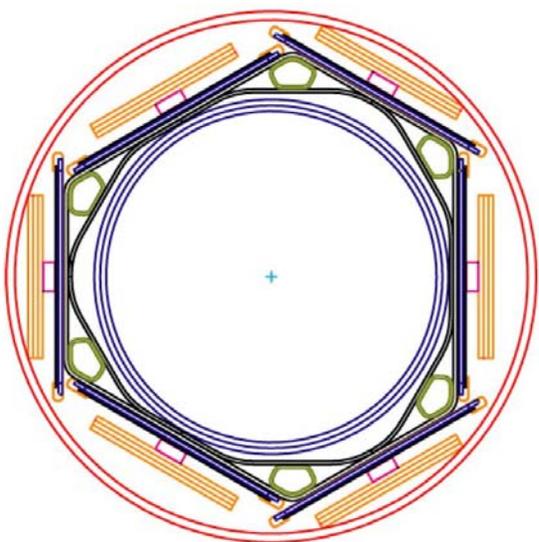
- Uses existing R&D on grounding, hybrids, sensors, supports, and cables
- Improve tracker performance even with radiation damage to other inner layers
- Difficult mechanical problem ...



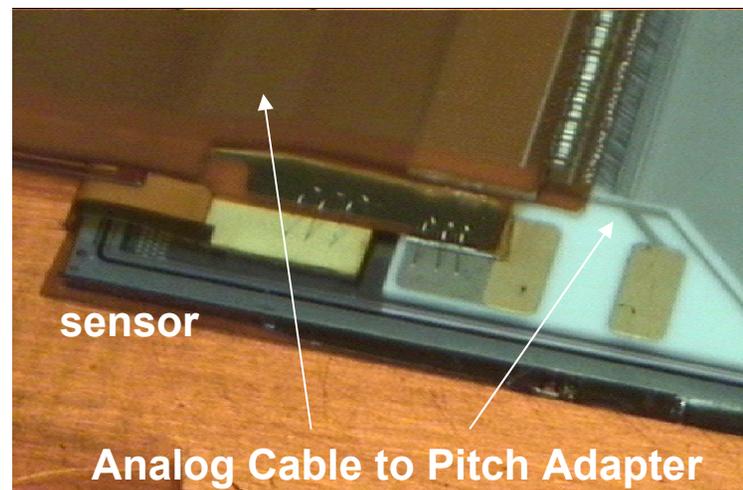


Layer 0 Geometry

- 6-fold symmetry
- 4 sensors /z half (2x7cm, 2x12cm)
- 71 μm readout pitch (inner) and 81 μm (outer)
- 98.4% ϕ acceptance
- 48 hybrids
- SVX4 chip
- extensive study of grounding issues to minimize noise



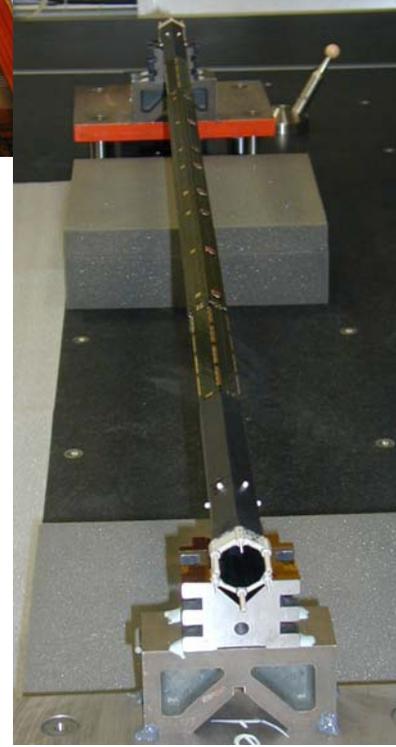
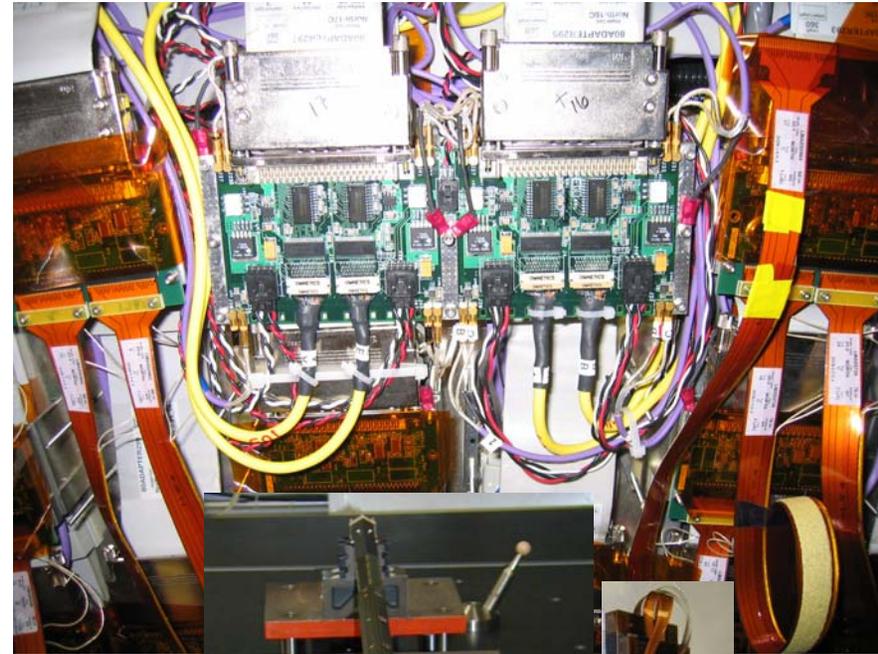
Hybrid region with co-cured kapton circuit





Layer 0 Status

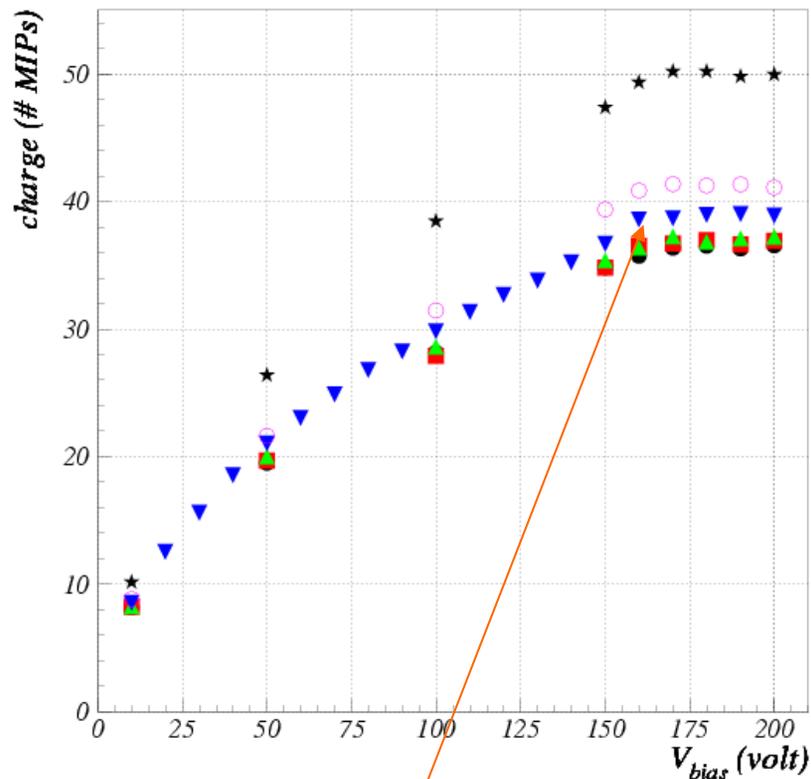
- All parts in hand
- Prototypes of each of the 8 different modules are done
- Hybrid stuffing 25% finished
- Prod. Readiness Review before Thanksgiving
- During this shutdown
 - Surveyed installation space
 - within 2 mils of expectation
 - good experience working in gap
 - Installed 4 SVX4 readout strings with two L0 modules and hybrids
 - Rearranged some of H disk cabling
 - installed upgrade LV power supplies
- Electrically and Mechanically complete support structure being measured at SiDet





Sensor Characterization

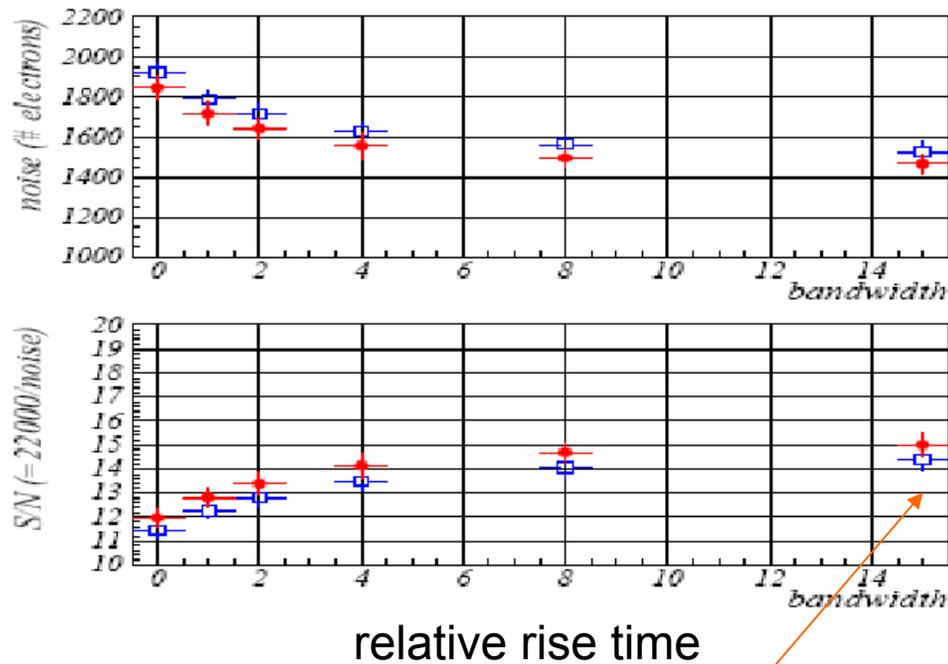
Sensors behave as expected:



Depletion at ~ 160 V

Kazu Hanagaki
Daekwang Kau

Noise (cont'd)



relative rise time

Signal/noise ~15:1

➤ also, essentially *no* dead channels



Installation/Commissioning

- SC-IPC Committee formed to quantify installation and commissioning needs
 - “Standing Committee on Upgrade Installation-to-Physics Commissioning”
 - Attempts to minimize loss of data for installation/commissioning by studying resources/schedules and making recommendations
 - First Report produced 10/12/04
 - survey of projects, task lists/schedule for completion of ancillary components/software and manpower needs to do this
 - try to make sure nothing falls through the cracks
 - First three recommendations already accepted:
 - Trigger Coordinator (N. Varelas), L0 Software, L1Cal manpower
- “Installation Readiness” reviews will be conducted
 - include software, diagnostics, additional infrastructure, and manpower



Conclusions

- Hardware for the Trigger and Layer 0 projects is progressing nicely
 - on schedule for installation in 2005 shutdown
- All systems must be running reliably on parallel readout chains before they are installed
 - much of this already in place
 - will work on this continually over the next year
- Software and integration work beginning – SC-IPC committee is a crucial part of planning for physics integration
 - software efforts progressing well
 - other infrastructure needs now coming into focus
- Installation plans are being refined