The Silicon Detector Concept

Norman Graf (SLAC)
(on behalf of the SiD Concept Group)
ILC PAC, Taipei
May 19, 2011

The Path to 2012: SiD Work Plan

- Focus and Goal for SiD is the Detailed Baseline Design of the detector.
- Continuing essential detector R&D, both specific to SiD and as partners in the “horizontal” detector working groups.
- Collaborating with CLiC physics and detector working groups in preparation of the CDR.
- Waiting for LHC results…

Detailed Baseline Design Deliverables

1. Demonstrate proof of principle on critical components.

   When there are options, at least one option for each subsystem will reach a level of maturity which verifies feasibility.

2. Define a feasible baseline design.

   While a baseline will be specified, options may also be considered.

3. Complete basic mechanical integration of the baseline design accounting for insensitive zones such as the beam holes, support structure, cables, gaps or inner detector material.
4. Develop a realistic simulation model of the baseline design, including the identified faults and limitations.
5. Develop a push-pull mechanism, working out the movement procedure, time scale, alignment and calibration schemes in cooperation with relevant groups.
6. Develop a realistic concept of integration with the accelerator including the IR design.
7. Simulate and analyze updated benchmark reactions with the realistic detector model. Include the impact of detector dead zones and updated background conditions.
8. Simulate and study some reactions at 1 TeV, including realistic higher-energy backgrounds, demonstrating the detector performance.
9. Develop an improved cost estimate.

Detailed Baseline Design Scope

"…doesn't attempt to produce full engineering designs of all the detector components, nor does it include production and testing of full detector prototypes. These are not imaginable with the present level of support. Rather it attempts to establish technical feasibility for key detector systems, conceptually engineered designs of detector subsystems, and proofs of principle of key engineering assumptions, in addition to an accurate rendition of detector and physics performance with a level of simulation detail previously unmatched in high energy physics proposals. "

1 Proof of Principle for Components

- NOT a complete summary of all SiD activities.
  - Not possible in time allotted.
  - Some projects are SiD-specific, others are pursued within the context of the “horizontal” detector R&D efforts, others are technology options.
- A snapshot of selected areas with significant changes relative to the 2010 PAC presentation.
  - Projects move at different rates.
- See the Interim Report (due out soon) for full details on all of the SiD activities related to the DBD and beyond 2012.

1 Vertex Sensor R&D: ChronoPixel

- Tests of the first chronopixel prototypes are now completed.
- Tests show that general concept is working.
- Noise figure is within specifications.
- Sensors leakage currents is not a problem.
- Sensors timestamp maximum recording speed (7.27 MHz) exceeds required 3.3 MHz.
- No problems with pulsing analog power.
- Next prototype will address issues found, and incorporate new design featuring all-NMOS transistors.
- Expect next round of prototype chips mid-year, with testing completed by end of 2011.

1 Vertex Sensor R&D: ChronoPixel

- We have good prospects of developing time stamping pixel detector for use in the future linear colliders, either ILC or CLIC
- We have developed software package allowing detailed simulation of such detector performance
- In the process of detector development we came up with solution allowing simpler (and cheaper) manufacturing of such detectors (no need for deep p-well).
- Simulation shows, that 20 μ pixel size even without analog readout can provide point resolution adequate for ILC physics (3.5 μ).
- This means, that we can get pixel detector for ILC using 90 nm feature size technology – no need for 45 nm technology as we originally anticipated.

1 Vertex Sensor R&D: 3D Multiproject

- HEP consortium for 3D circuit design formed in late 2008
  - 17 member groups from 6 countries (Italy, France, Germany, Poland, Canada, USA)
  - First Meeting Dec 2008
  - Began working on 3D MPW run to Chartered/Tezzaron -First MPW run for outside customers
  - Two tiers
  - Identical wafers with face to face bond
  - Single set of masks for both tiers
- HEP MPW run - more than 25 two tier designs (circuits and test devices)
  - CMS strips, ATLAS pixels
  - ILC pixels
  - B factory pixels
  - X-ray imaging
  - Test circuits
- Frame divided into 12 subreticles for each tier

1 Vertex Sensor R&D: SOI

SOI detectors utilize the “handle wafer” of an Silicon-on-Insulator
device as a detector, with electronics mounted in the thin device layer on top of the “buried oxide”

- A truly monolithic device … however:
  - The fields in the handle can act as a “back gate” to the topside transistors, shifting the characteristics and limiting the practical applied voltage.
  - The topside digital signals are in close proximity (200nm) to the sensor, causing unacceptable noise coupling.
- Possible solutions
  - Dual gated transistors with intrinsic shielding (American Semiconductor FLEXFET)
  - 3D assembly with minimal circuitry on sensor tier
  - Buried well structure to shield transistors and pixel

1 VTX 3D and SOI

Lot of effort, not just SiD. Substantial progress and some real breakthroughs

- 3D multiproject chips being tested
- 3D process commercialized
- SOI process developed which is robust against backgate effects and digital to analog coupling.
- First detector test with electronics integrated with float zone silicon

- have functional 3D chips from MIT-LL and tested
- front-ends of the 2D versions of the 3D chips from Tezzaron.
- SOI work has led to functional technology including the demonstration of a concept that can avoid the backgate effect (patent being discussed with OKI) and backside processing (with Cornell) that can be developed into a ILC vertex sensor when appropriate.
- also applying the ILC work to the CMS track trigger project and are developing techniques for fabricating large area arrays which could be applied to ILC.

Would be ready to proceed to full-sized fully functional devices in either SOI or 3D. Both the circuit design and chip/sensor technology has become mature enough for full scale prototypes.

There is no funding and no pressing need to do this – intend to proceed with technology development with x-ray, LHC and perhaps B factory applications. Intend to turn back to ILC/CLIC/muon collider applications when the time scales become clearer.

Digital Hadron Calorimetry: DHCAL

Role of PFA Hadron calorimeter

→ identify energy deposits belonging to neutral hadrons
→ measure the energy of neutral hadrons

Favored HCAL technology

Resistive Plate Chambers (RPCs) with very fine readout

Development of RPCs for calorimetry

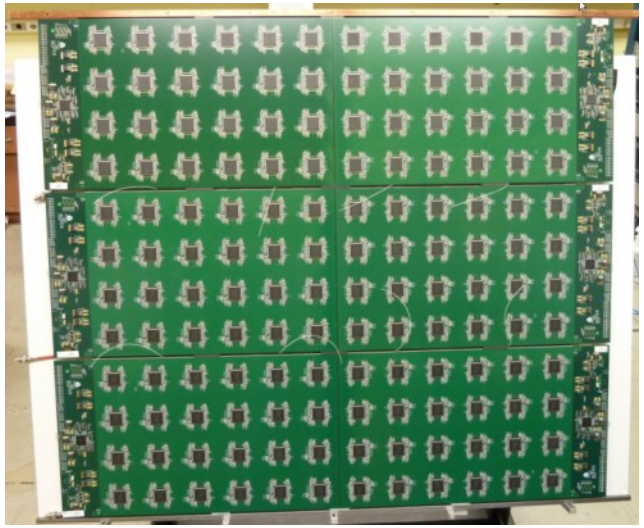
Evaluated various chamber designs
Detailed measurements with 14-bit ADC and multiple pads
Results published in NIM paper

Small scale prototype built and tested in test beam

Up to 10 layers, 20 x 20 cm^2 RPCs with 1 x 1 cm^2 readout pads
Results published in 5 JINST papers

Technology for large scale prototype developed

Large RPCs (32 x 96 cm^2) with minimal edges (very challenging!)
Digital (=1-bit) readout based on DCAL chip (2 iterations)



Large scale prototype built

Produced	~10,000 DCAL III chips (not a single design fault!!!)
	205 RPCs
	337 Readout boards
	56 cassettes (with protective covers)
	Low Voltage system (with 384 channels)
	Gas system (with 28 separate lines)
Borrowed	High Voltage system (with 64 channels)

Large effort involving a total of 39 people

DCHAL stack

38 layers with 350,000 readout channels
Inserted into CALICE AHCAL structure

TCMT stack

14 layers with 130,00 readout channels
Inserted into CALICE TCMT structure

1 Testbeam activities

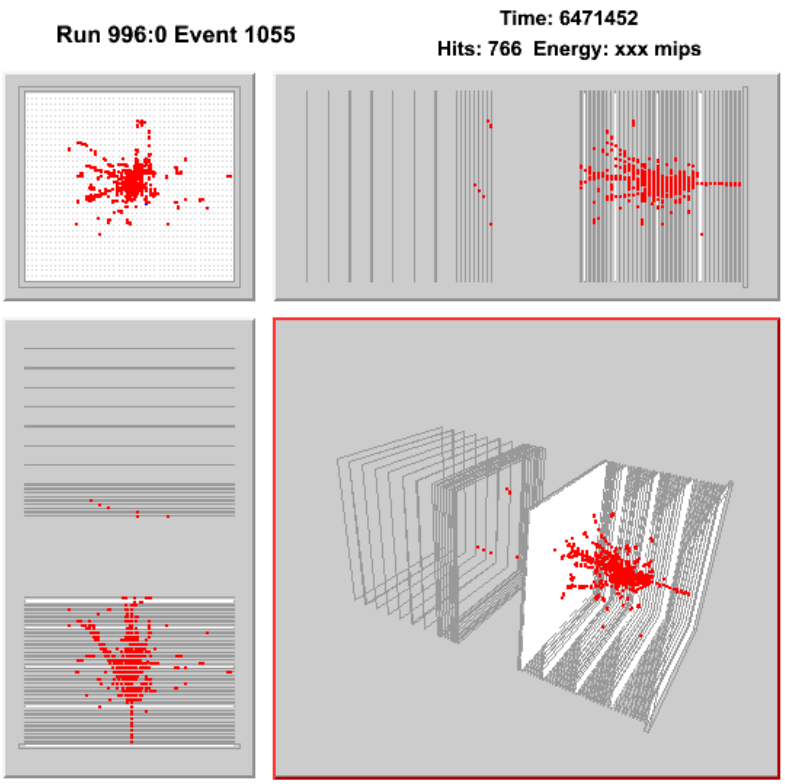
Run period	Date	Configuration	Muon events [10^6]	Secondary beam events [10^6]	Secondary beam momenta [GeV/c]
1	Oct 2010	**DHCAL**	1.4	1.5	2,4,8,10,12,16, 20,25,32
2	Jan 2011	DHCAL **+ partial TCMT**	1.6	3.6	2,4,6,8,10,60
3	Apr 2011	**ECAL** + DHCAL + **TCMT**	3.5	4.8	4,8,12,16,20,25, 32,40,50,60,120
4	Jun 2011	DHCAL + TCMT			32,40,50,60,120
5	Fall 2011	DHCAL with **Tungsten** + TCMT			4,8,12,16,20,25, 32,40,50,60,120
6	Later	DHCAL **w/o absorber**			0.50,0.75,1.00, 1.25,1.50,2.00
TOTAL			**6.5**	**+ 9.9**	**= 16.4M**

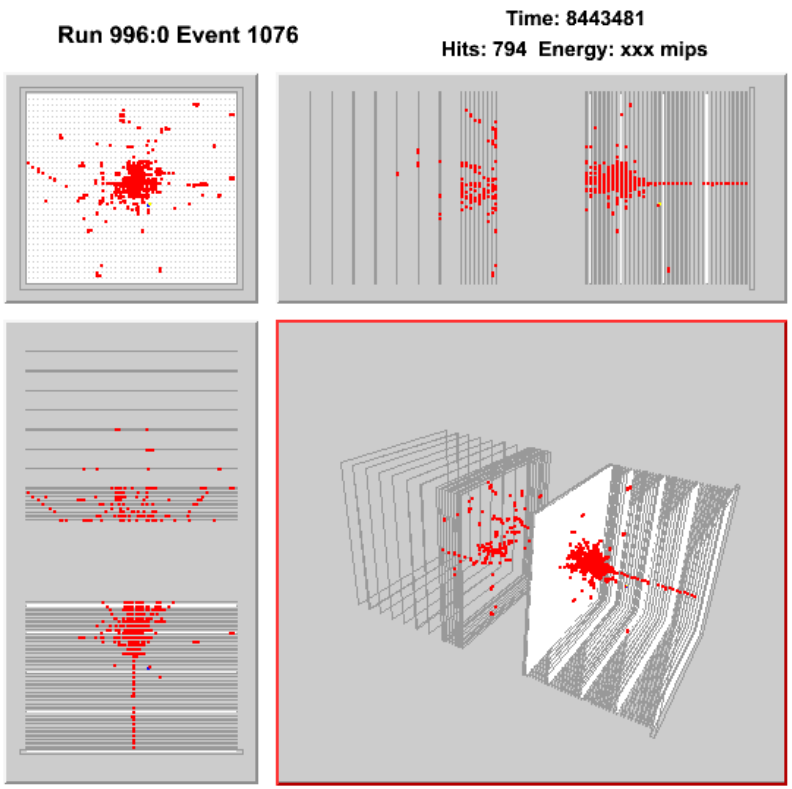
Typical pion events at 60 GeV/c

Note:

These are typical events, not (too) carefully selected

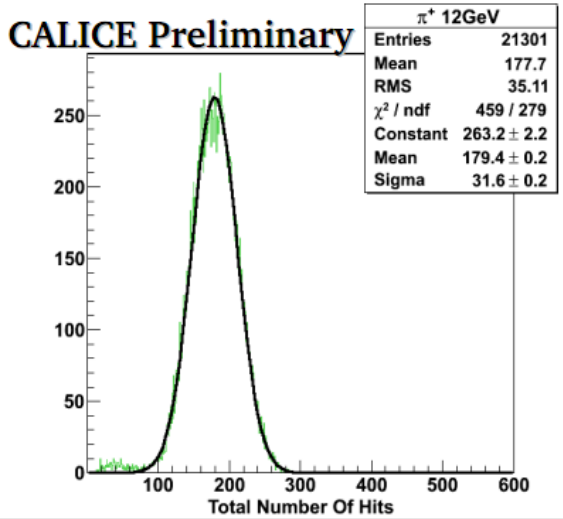
Isolated hits are **not** noise!

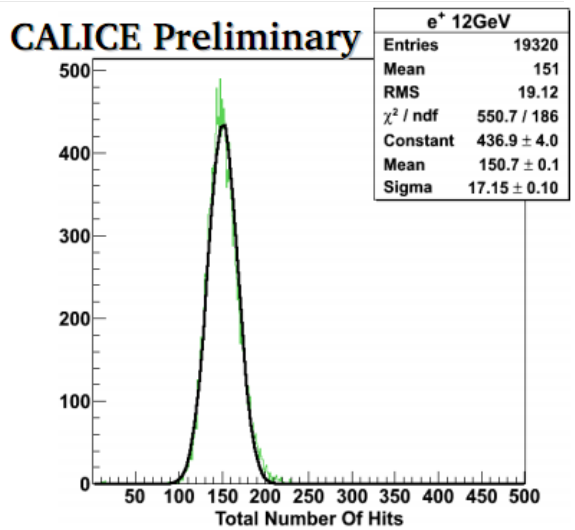


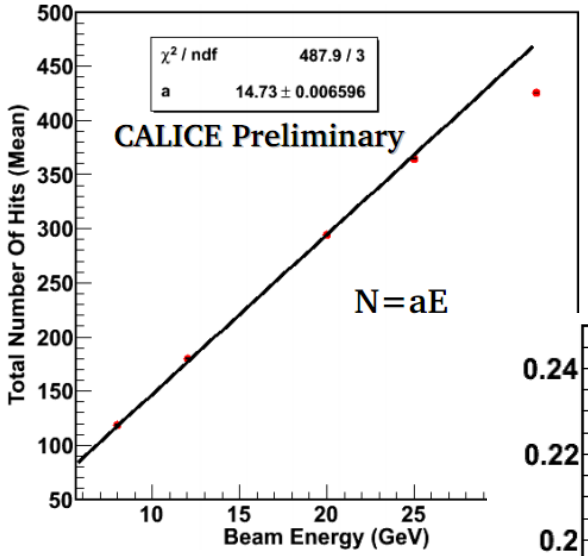


Results from Analysis of Secondary Beam Events

Example - p = 12 GeV/c





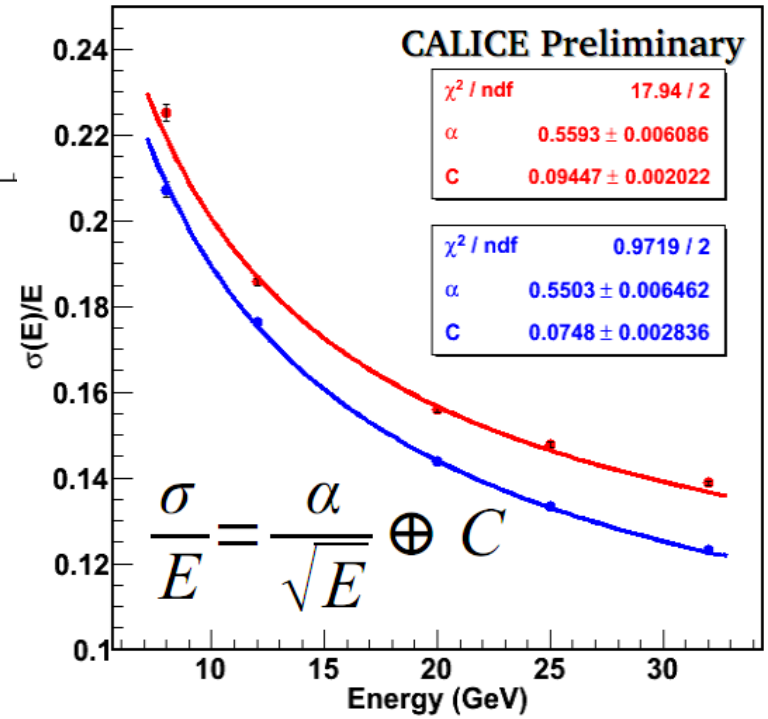


Response to pions

32 GeV/c not included in fit

Without cut on containment

With cut on containment

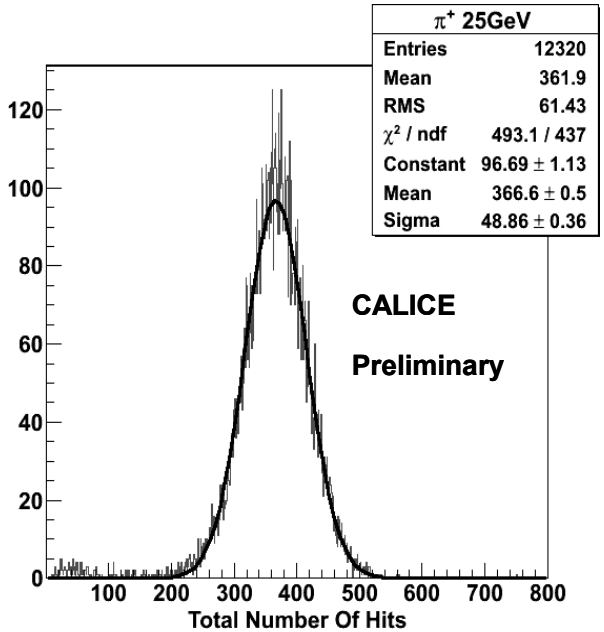


$$\frac{\sigma}{E} = \frac{\alpha}{\sqrt{E}} \oplus C$$

Preliminary results from test beam

Noise rate

Higher than anticipated, due to elevated temperature
Noise rate corresponds to 0.1 Hits/(triggered event) in the DHCAL +TCMT
Still ~negligible



Muon calibration

Many analysis ongoing…
Average efficiency = 93.6%, pad multiplicity = 1.56, as expected
Alignment of layers, calibration and simulation of response in progress

Positron/pion analyses

Many topics to be covered…
Response to both positrons and pions similar to expectation from previous simulation work

The concept of a DHCAL with RPCs is close to being validated

1 Electronics R&D: KPiX

KPiX readout for SiD subsystems except VTX.

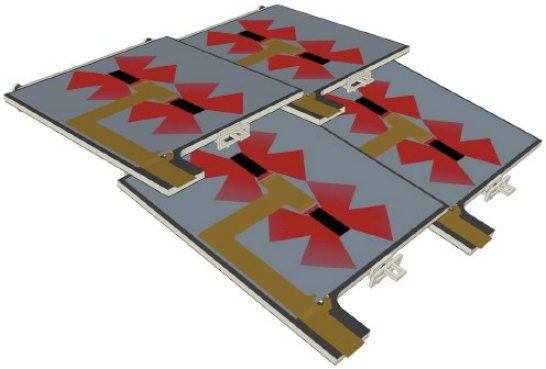
Tracker

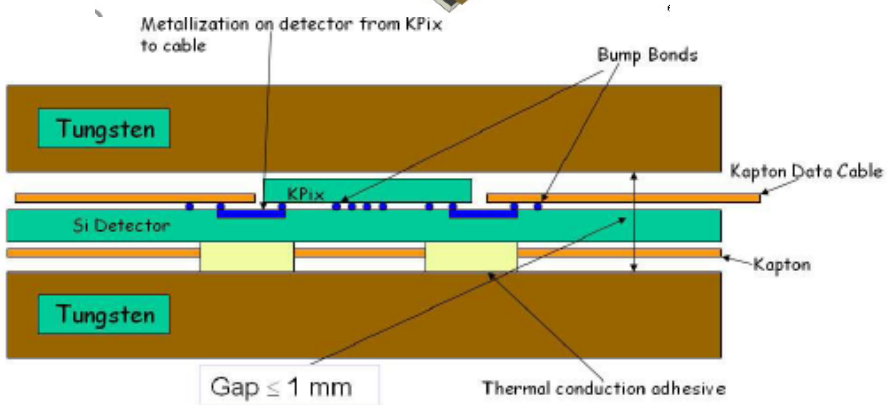
ECal

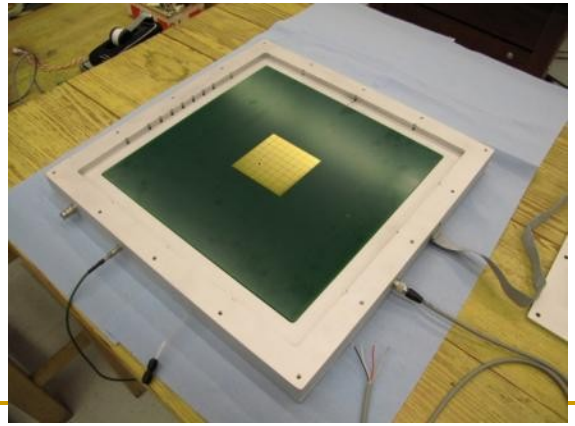
HCal (GEM version)

…and Muon!

+ working on an FCal version





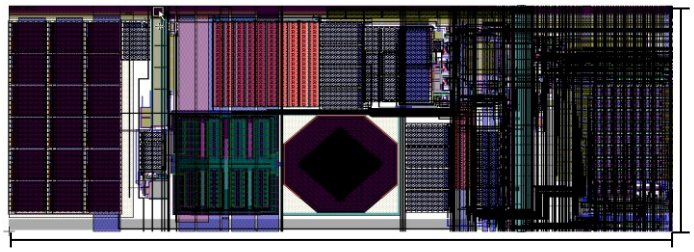


1 Electronics R&D: KPiX

- KPiX is a multi-channel system-on-chip, for self triggered detection and processing of low level charge signals.
- A digital core controls all operations according to parameters stored during set-up. This allows to match the chip to signals from a variety of sources. A variety of options, selectable by register settings, have been added over several prototype cycles.
- The only external control signals are system clock, reset and command. Data output is serial.
- Low average power consumption (<20 μW per channel) for ILC operation is obtained by powering down between beam spills. Power is reduced by lowering currents by a factor 100 while keeping the supply voltage stable. The current drop is controlled, with a decay time-constant ~10 us, to limit voltage spikes caused by the cable impedance.
- The chip is designed to be bump bonded to a Si-sensor, or to a hybrid for large area detectors (RPC's, GEM's). This avoids an extensive signal level cable plant (or headers) for the detector signals, resulting in significant reductions in mass (multiple scattering) and cost.
- Range- and Noise-Specifications:
  - Peak Signal (Dual Range) 10 pC.
  - Range Switching (selectable) ~400 fC.
  - Noise Floor 0.15 fC (1000 electrons).

1 KPiX Status

- 1024 pixel KPiX now being tested.
- Working on bump bonding KPiX to prototype ECal and tracker detectors.
- Working on bump bonded cable attachment to ECal and tracker detectors.
- Developing 32 KPiX Ethernet interface to replace 3 KPiX USB interface.



1 Pixel layout

2 Silicon Detector Baseline Design

A compact, performance- & cost-optimized detector designed to make precision measurements and be sensitive to a wide range of new phenomena.

"Imaging calorimeters", optimized for dijet invariant mass resolution, based on a Particle Flow approach, compact showers in ECal, highly segmented (longitudinally and transversely) ECal and HCal.

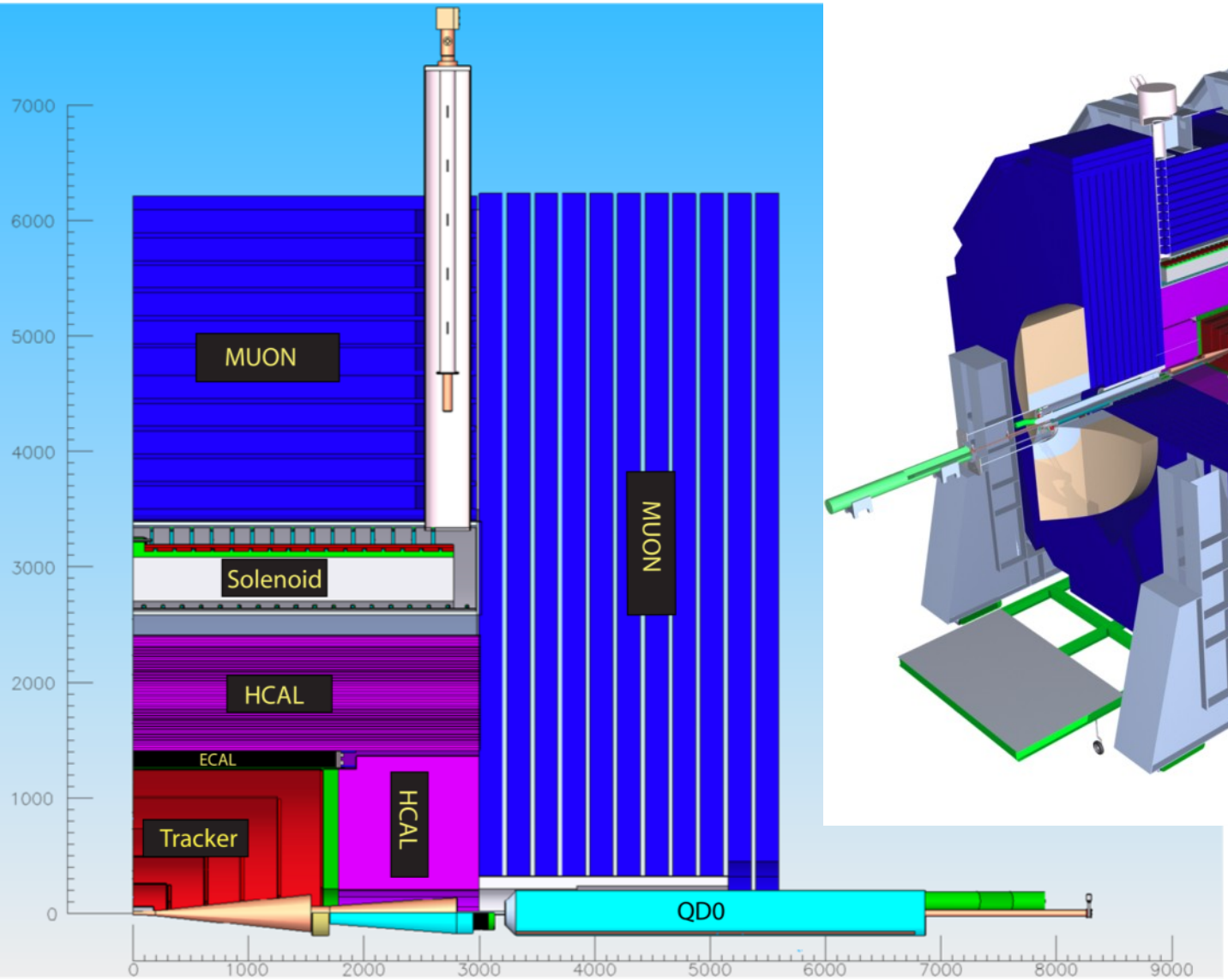
Compact design with 5T field.

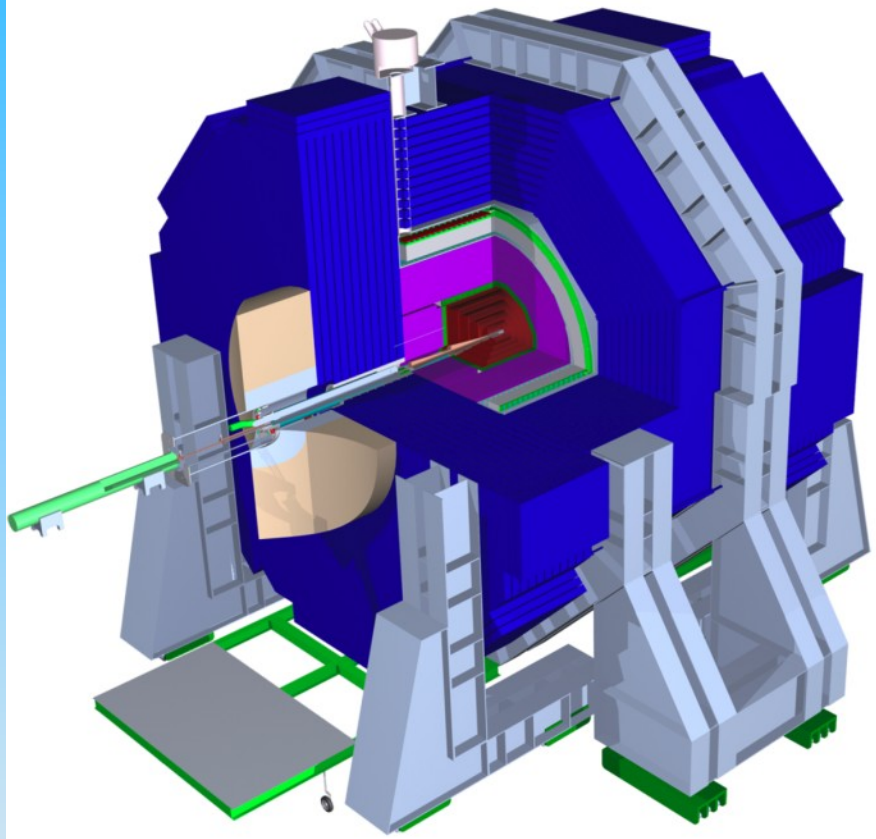
Robust silicon vertexing and tracking system – excellent momentum resolution, live for single bunch crossings.

Iron flux return/muon identifier – component of SiD self-shielding.

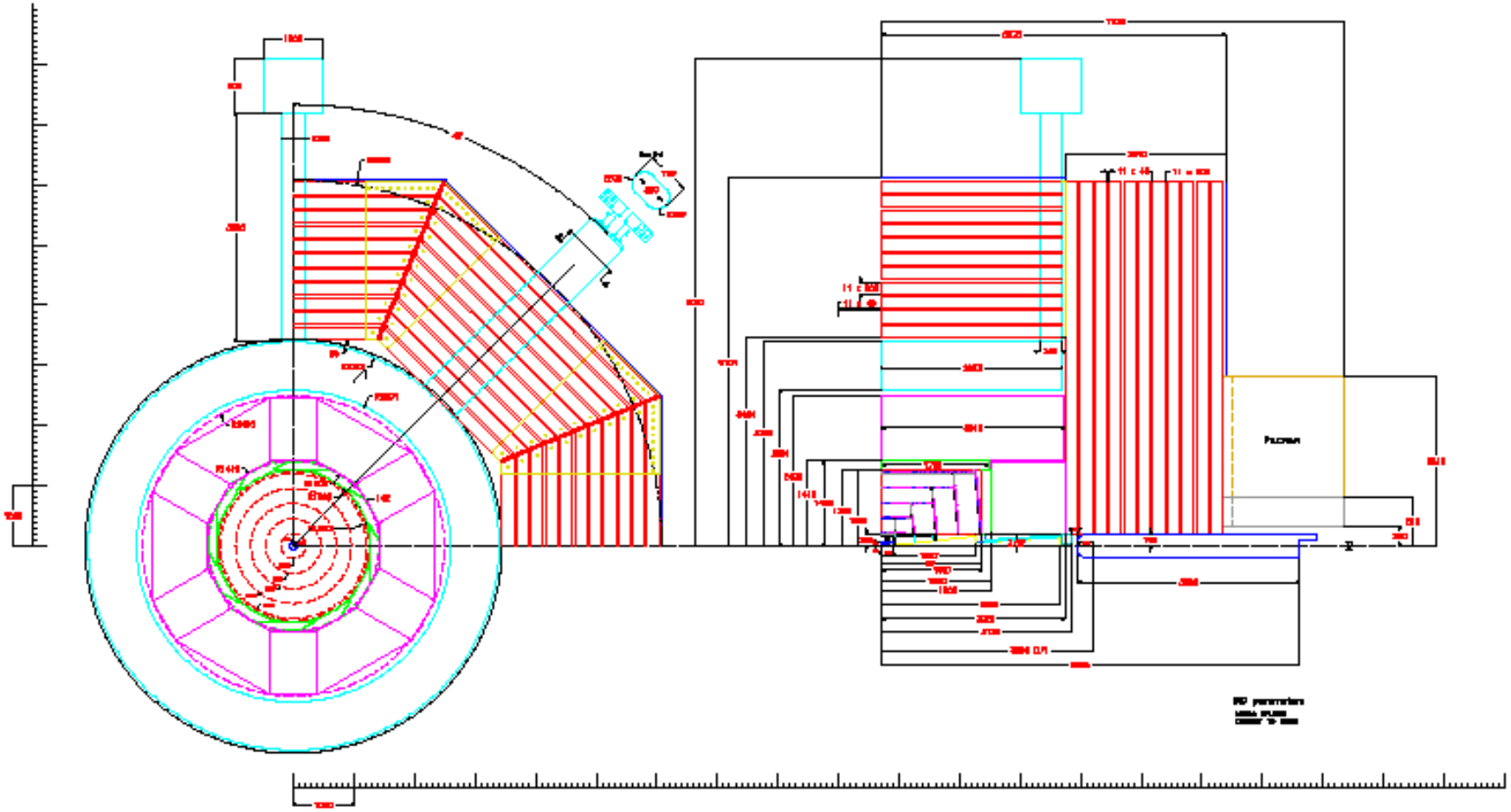
Designed for rapid push-pull operation.

2 The Silicon Detector Concept



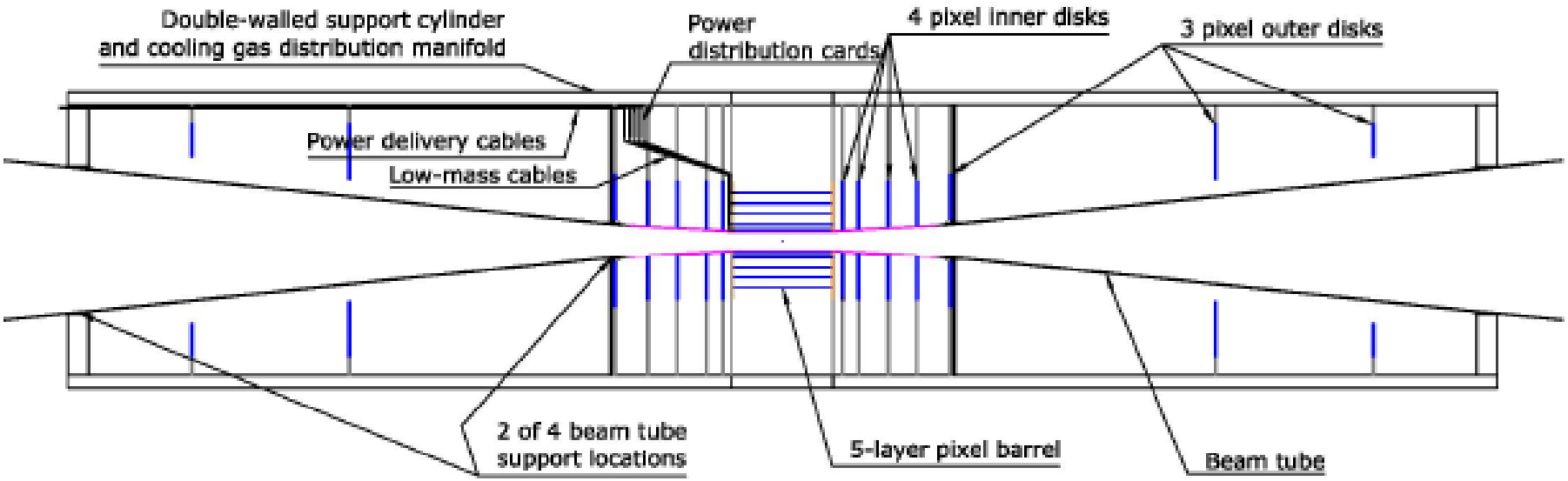


3 Basic Mechanical Integration

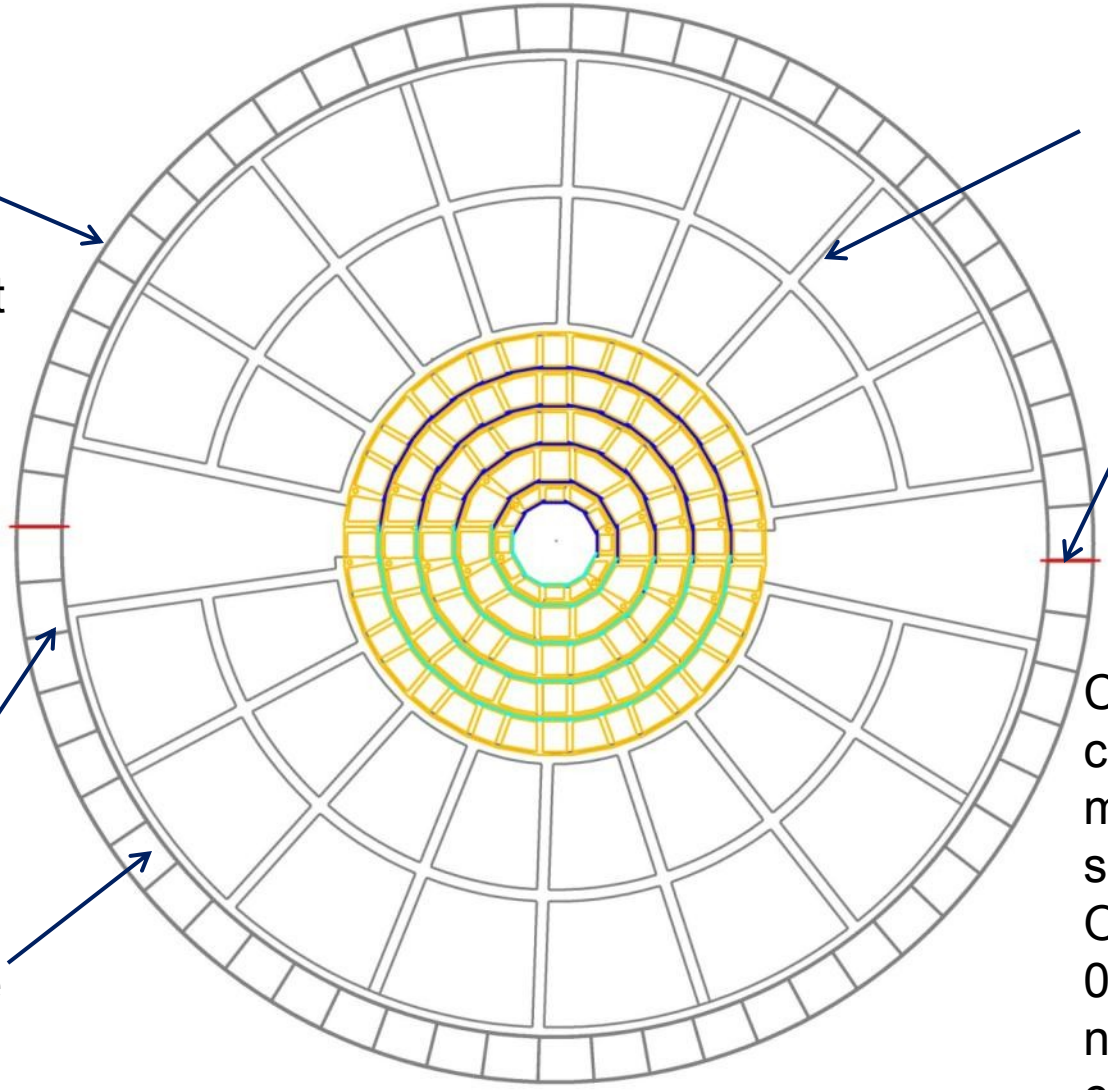


3 Basic Mechanical Integration Example

- Sensors glued on edges to form cylinders
- Gas cooled, power pulsed, low mass
- Pixel outer disks match coverage of outer tracker



3 Vertex Barrel and Supports



Double-walled, carbon fiber, outer support cylinder

Web structure would probably be conical to improve Z-stiffness

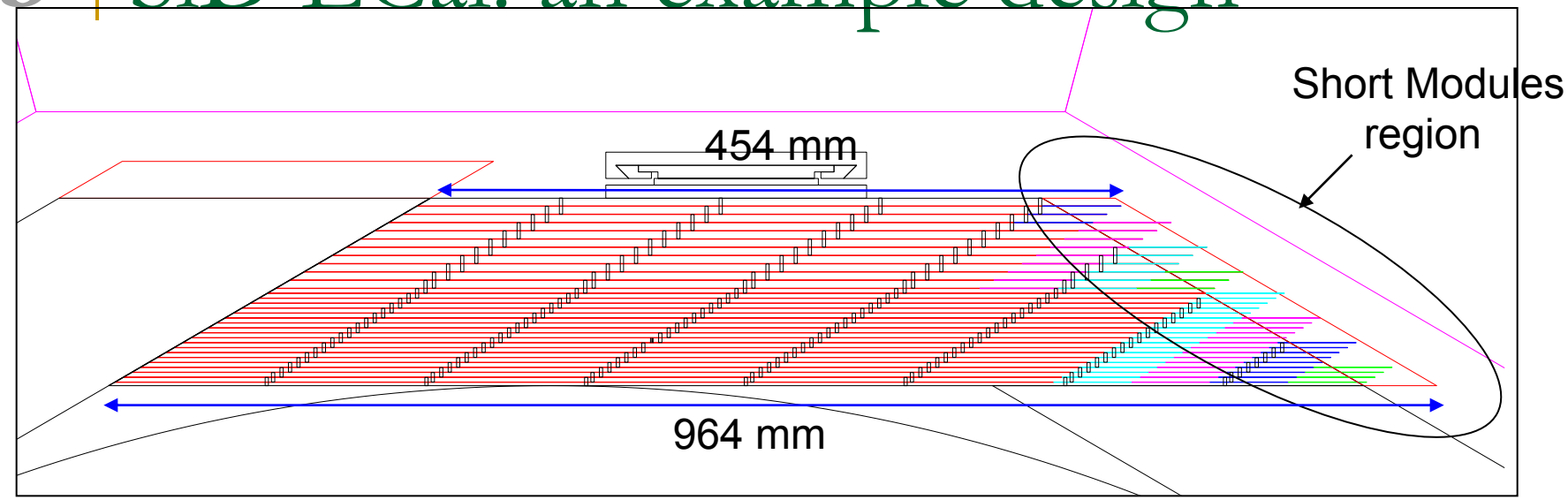
Separation line between upper and lower half-cylinders

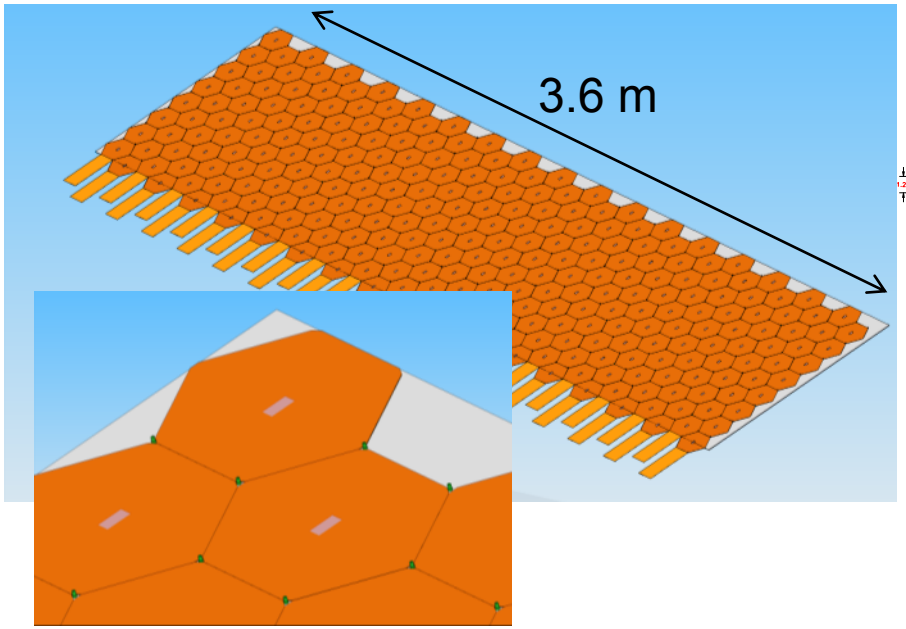
Longitudinal strips ("ribs") separate the walls

Cooling gas flow passage (60 total)

Cable contributions to material is significant. Original goal of 0.1% X0/layer did not include cables.

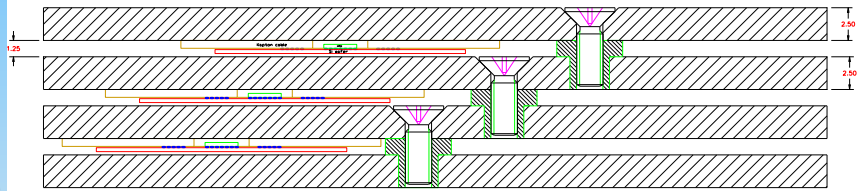
3 SiD ECal: an example design

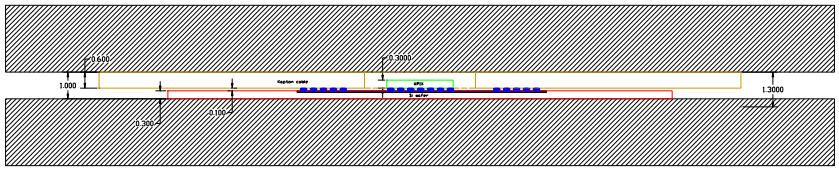




Staggered layout

Only 2 masks for the wafer and 8 for the kapton





4 Realistic Simulation Model

- The detector model for the LOI was a necessary compromise between the desire to include all the details of the engineering designs and the need to complete the large-scale physics benchmarking simulations in a timely fashion.
- Since then have developed a detector model which includes more realistic detectors.
  - Benefits from engineering work done for the LOI.
  - Allows much more realistic subdetector performance studies to be undertaken.
- Improvements continue to be made as optimization proceeds.

4 Reconstruction: Tracking Performance

LOI showed excellent performance for baseline SiD tracker

- >99% track finding efficiency over most of the solid angle
  - ~98% in core of 500 GeV light quark jets
- Momentum resolution typically ~0.2% for $|\cos(\theta)| < 0.65$
  - $\sigma(p_T) / p_T < 0.5\%$ over most of solid angle for 1 GeV < p_T < 100 GeV
- DCA resolution typically ~15μm for p_T = 1 GeV, $|\cos(\theta)| < 0.65$
  - Most tracks multiple scattering limited – resolution approaches ~4μm at high p_T
- >99% of tracks have ≤1 mis-assigned hits
  - Fake track rate is 0.07% for tt events

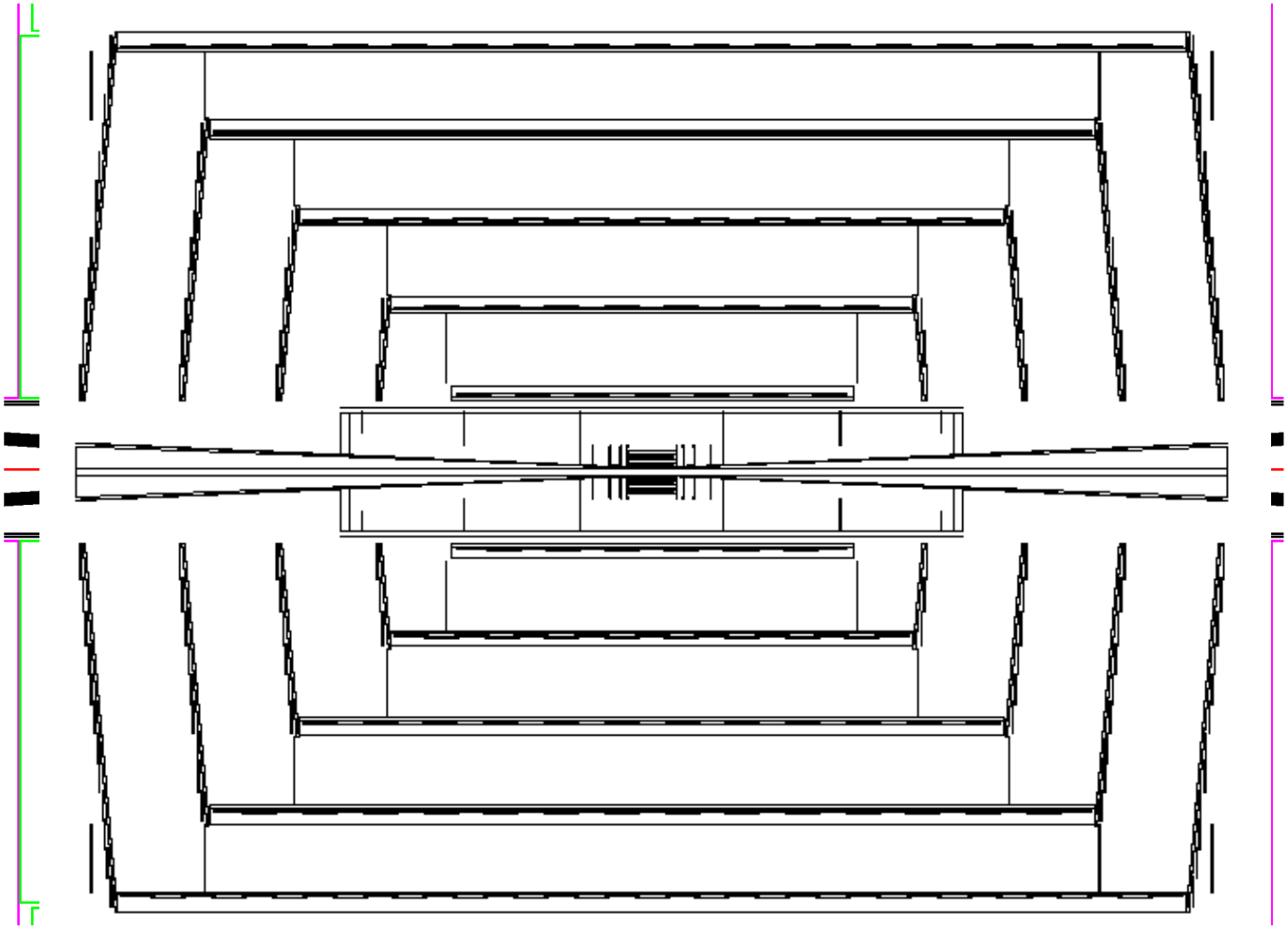
Post-LOI Challenges:

- Increase detail/realism in modeling of the tracker
- Efficient tracking simulations with beam backgrounds, higher E_{cm}
- Address deficiencies in LOI tracking

4 Tracking Improvements

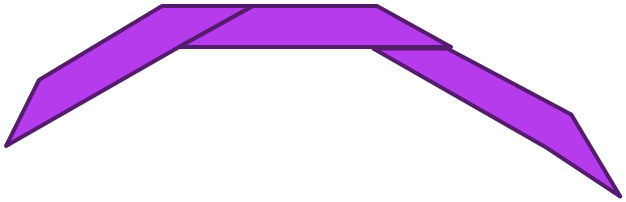
- Planar detector geometry with individual sensors simulated
  - Fully overlapping rectangular sensors in barrel detectors
  - Overlapping trapezoidal sensors on conical supports for endcap detectors
- Realistic charge deposition model for strips and pixels
  - For strips, track segment is divided into pieces and drifted/diffused to strips
  - For pixels, can either use strip model or PixSim package that provides detailed modeling of various types of pixel detectors
- Nearest neighbor clustering of hit strips/pixels
- Hits are formed with realistic hit position and uncertainties
- Memory footprint and reconstruction time both improved as result of application to CLiC environment.
- Tested in 3TeV environment and in the presence of complete bunch train overlay.

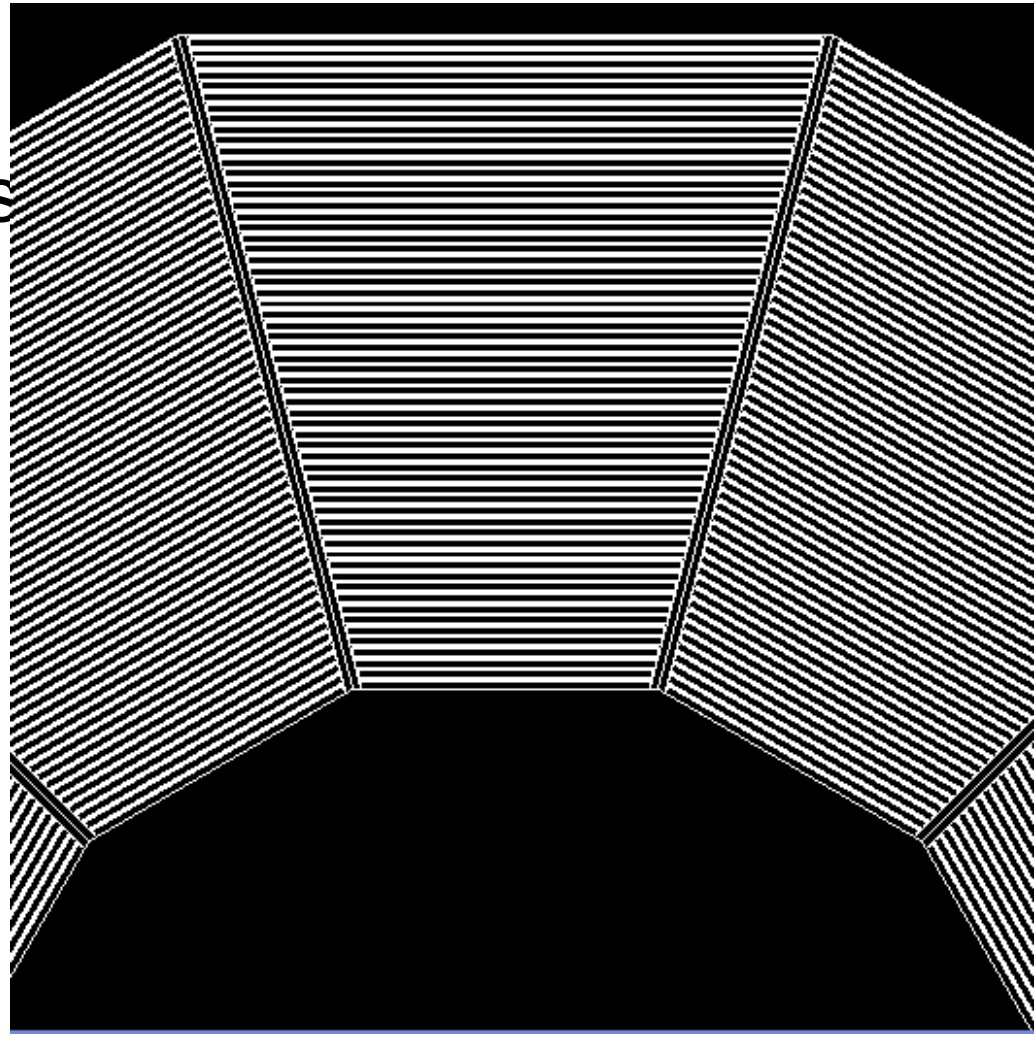
4 SiD Tracker Model (sidloi3)



4 Calorimeter Model with Staves & Gaps

- Polygonal stave geometry
- Gaps between staves for supports and services
- Projective model shown for HCal
- Overlapping staves for ECal.





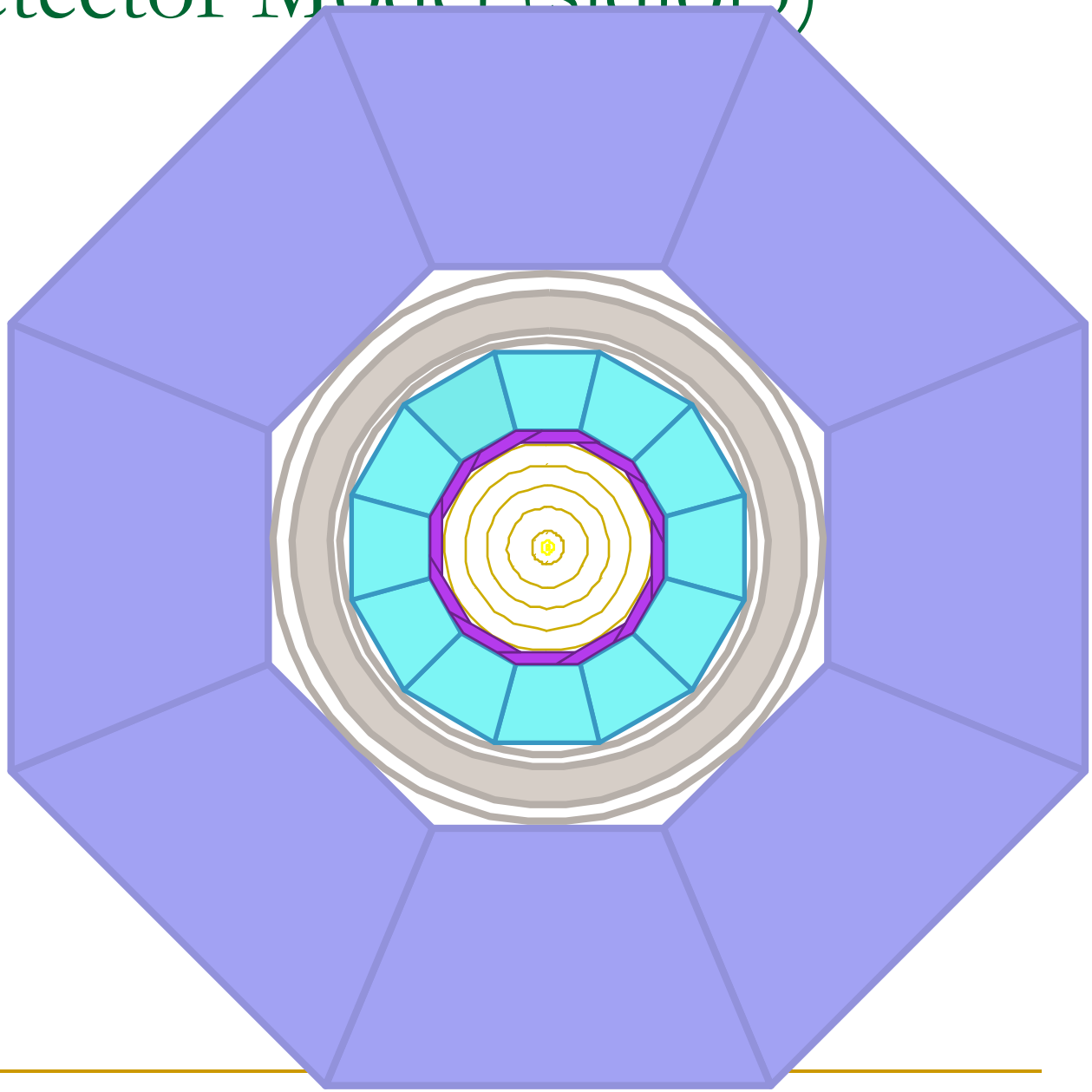
4 Silicon Detector Model (sidloi3)

Dodecagonal, overlapping stave EMCal

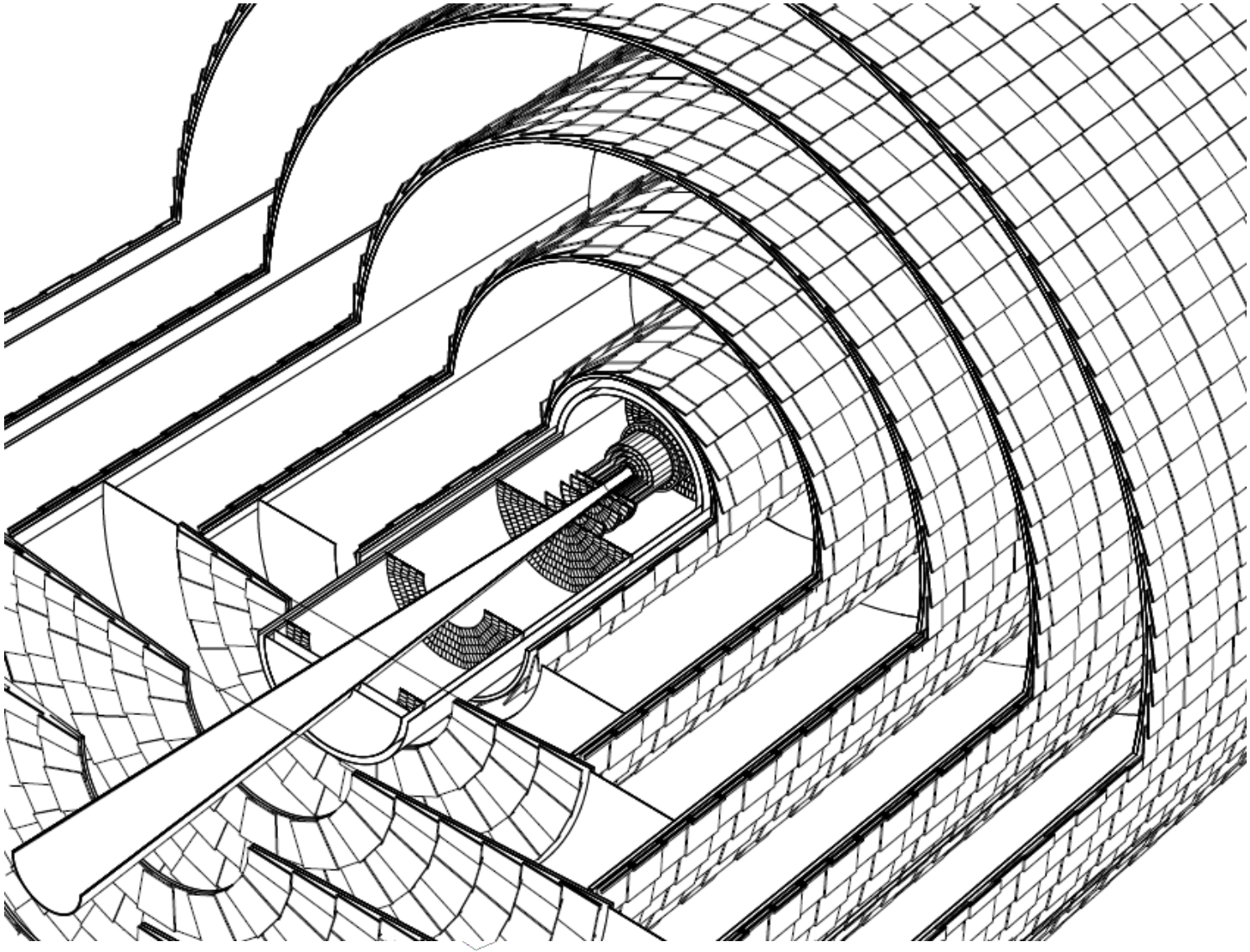
Dodecagonal, wedge HCal

Cylindrical Solenoid with substructure

Octagonal, wedge Muon

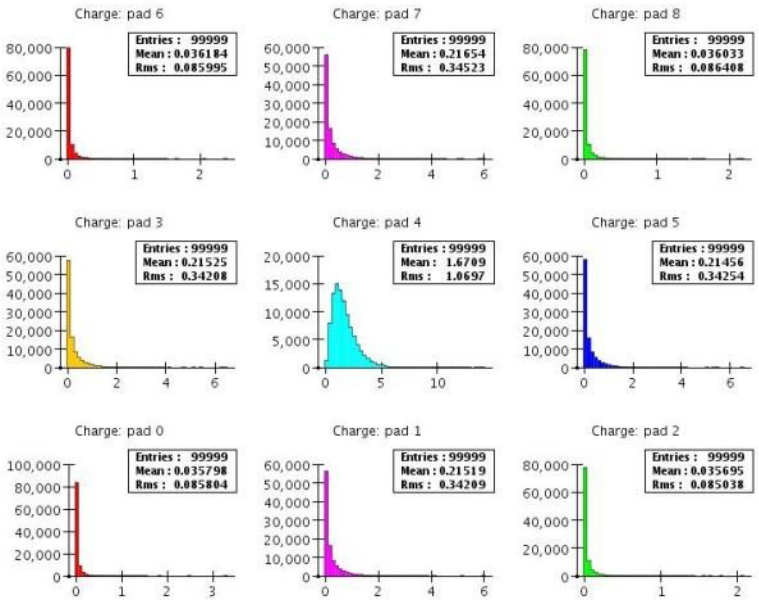


4 Silicon Detector Model (sidloi3)

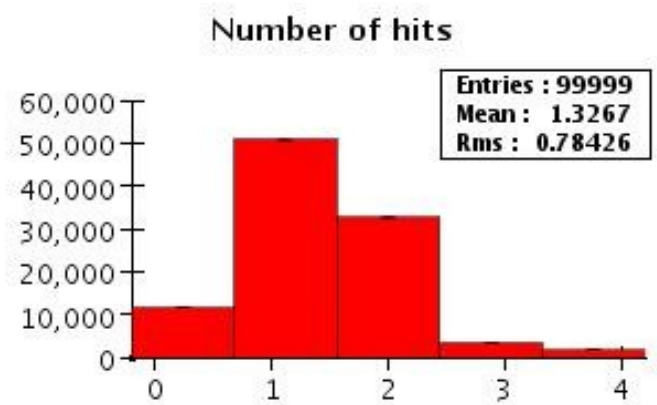


4 Improving RPC response simulations

- Simplified response in LOI assumed no charge sharing, cross-talk or inefficiencies.
- Improving code to simulate charge distribution on pads to emulate hit multiplicities seen in data.



Charge distribution [pC] on 3x3 pads
(6.3kV, E_{dep} randomly generated on central pad)

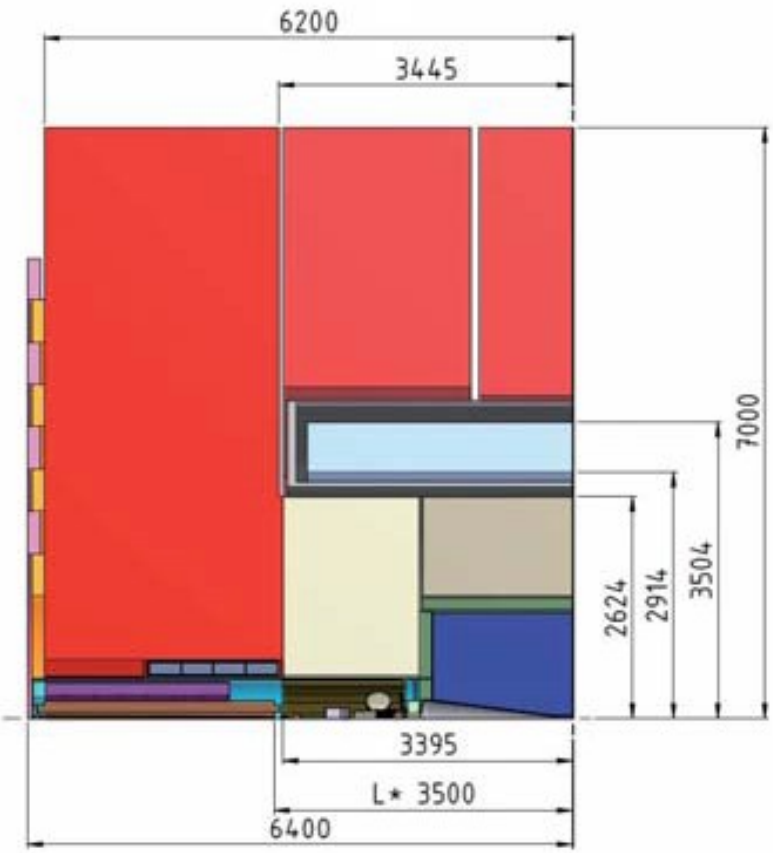


N(hit) distribution (thr = 0.6pC)
Efficiency ~ 89%
Multiplicity ~ 1.33

4 PFA Reconstruction: slicPandora

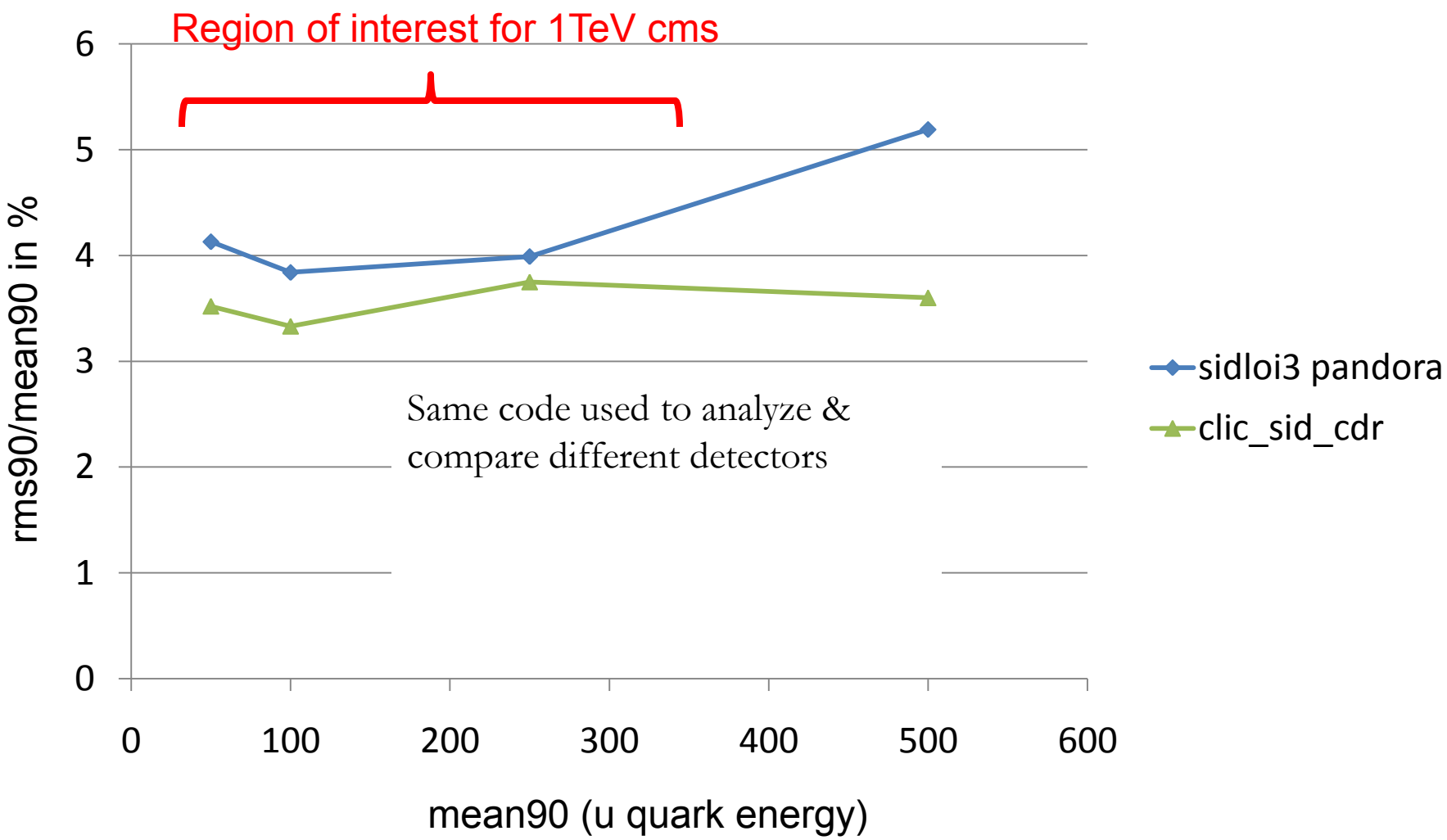
- Frontend to the PandoraPFA project.
  - LCIO binding, Geometry format, Sampling Fractions
  - Reads input LCIO file with simulated events, tracks, and track states.
  - Outputs LCIO file with Reconstructed Particles.
- Uses standard XML configuration file for PandoraPFA algorithm settings.
- Common event data model and persistency (LCIO) allows code sharing between concepts.
  - Similar to LCFI vertexing and flavor-tagging package.

clic_sid_cdr & sidloi3



clic_sid_cdr:
modified tracker layout to accommodate different crossing angle and backgrounds
deeper HCal, Tungsten in Barrel, Steel in endcap, Scintillator readout, short barrel plus capping endcap.

single u quark rms90/mean90 in %



Same code used to analyze & compare different detectors

4 Sim/Reco Future Work

- Further optimization of the detector layout
  - Number and position of tracking layers
  - Strip and pixel size and layout
  - HCal depth and segmentation
- Additional studies of calorimeter assisted tracking
  - Assist in kink finding and identification
  - Identification of long-lived resonance decays & γ conversions
- Systematic studies of the impact of:
  - hit inefficiencies / dead channels,
  - non-uniform magnetic field,
  - beam backgrounds, …

4 Sim/Reco Summary

- Simulation infrastructure essentially done.
  - Geometry system supports realistic detectors.
- Reconstruction code adapted and improved.
  - Tracking reconstruction now features planar silicon wafers, full hit digitization, clustering to form hits (with hit-size dependent uncertainties).
  - Interface to PandoraPFA has been implemented.
  - Improvements have been made to event overlays
- Additional detector optimization studies being conducted before major event production.
  - First set of detectors defined, and large set of diagnostic events available for analysis.
- Performance and timing have been improved
  - Found and fixed bug in forward tracking.
  - Stressed with 3TeV events for CLiC CDR.

5 Push-Pull Mechanism

- SiD has agreed to a platform for Push-Pull detector interchange.
  - Producing functional specifications for the platform, but is not intending to do a conceptual design. It is understood that the Conventional Facilities group has taken on this role.
- SiD is studying functional requirements for the interaction region, associated access shafts, and significant surface facilities for a deep vertical access site; and is beginning studies for a horizontal access site.

6 Integration with the Accelerator

Please see the Machine Detector Interface talk presented by Toshiaki Tauchi on behalf of the MDI Common Task Group and Beam Delivery System.

7 Updated Benchmarks @ 500GeV

- SiD will repeat the $e^+e^- \rightarrow \tau^+\tau^-$ analysis.
- Event generation will begin once the detector optimizations have been completed.
- Do not expect any problems with either resources or manpower.

8 Benchmark Reactions @ 1 TeV

- The list of benchmark reactions has been agreed on.
- Waiting on GDE-approved machine parameters.
- Event generation will be distributed between KEK*, DESY and SLAC.
  - Signal events for 1 ab^{-1} sample (all four polarizations)
  - Additional signal events for algorithm development, statistics smoothing, etc.
  - Physics backgrounds
  - Machine backgrounds
    - GuineaPig pairs,
    - $\gamma\gamma \rightarrow$hadrons,
    - upstream muons, etc.

*may be modified in light of the earthquake

8 Benchmarking Next Steps

- Optimize and finalize detector design to be used in the DBD simulation.
- Simulate response to DBD input events.
  - Need “official” machine parameters right away.
  - Have generated small samples of all physics signal processes using interim machine parameters. Are using these for testing purposes.
- Overlay backgrounds.
- Run reconstruction.
- Prepare analysis algorithms.

8 Benchmark Production

- SiD members are actively involved with the CLiC CDR physics analyses.
- Machinery and infrastructure has been developed to automate many of the generation, simulation, reconstruction steps, especially those related to cataloging, storing and Grid job submission and monitoring.
- Expect that the same tools will be used for the DBD Monte carlo challenge.

9 Costing

- Costing and a parametric cost model have been included in the SiD design since the beginning.
- Analyze physics performance (uncertainties in measurements) vs cost.
- SiD is actively participating in the costing panel exercises.
  - Represented by M. Breidenbach and K. Krempetz.
- Please see the talk presented by Sakue Yamada.

CLiC CDR & clic_sid

- Very successful collaboration between SiD and the CLiC physics and detector CDR effort
  - SiD design modified for CLiC machine parameters
    - modified tracker layout
    - deeper HCal: W in Barrel, Steel in endcap, Scintillator readout
  - Development of an SiD version of PandoraPFA
  - Co-development of SiD tracking
    - Hit digitization & track finding improved
    - All improvements are fed back to the same software base
  - Background event overlay improved and made robust
  - Several SiD members are serving as CDR editors, engaged in simulation, reconstruction and analysis efforts
  - CLiC LCD group will reciprocate on DBD

Summary

- SiD has invested a lot of time and effort, and has made a lot of progress towards the Detailed Baseline Design.
- Ongoing R&D in all subsystems.
  - both specific to SiD and in collaboration with others.
- Baseline technologies identified and alternatives being considered.
- Major improvements in realism of simulations.
- Comprehensive Work Plan defined
  - manpower and financial resources limited

    "if we had more, we'd do more"

The Future

- Would appreciate comments on our DBD strategy.
- The large body of work, done with limited resources, is in jeopardy without focus and funding beyond 2012.
- Endorsement of the work, and an acknowledgement of the value which has resulted, not only to ILC, but to the wider community, would be helpful.

  e.g. pixel sensor development, calorimeter R&D
- This effort must continue in order to be positioned to react to LHC discoveries, whether those lead to ILC or CLIC
  - we are preparing for either
  - Note - reaction to new physics will likely take time beyond 2012