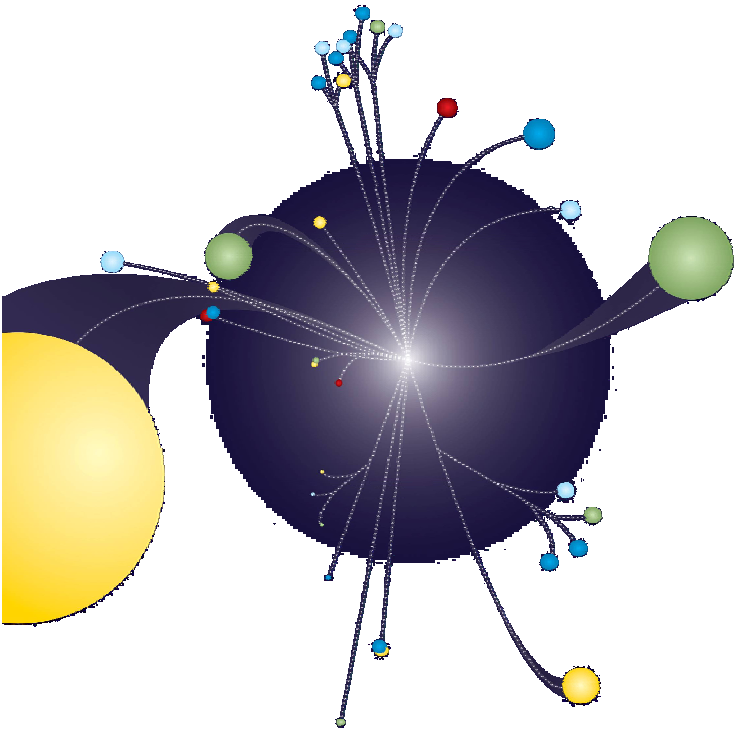
Generic Detector R&D
and
Test Beams



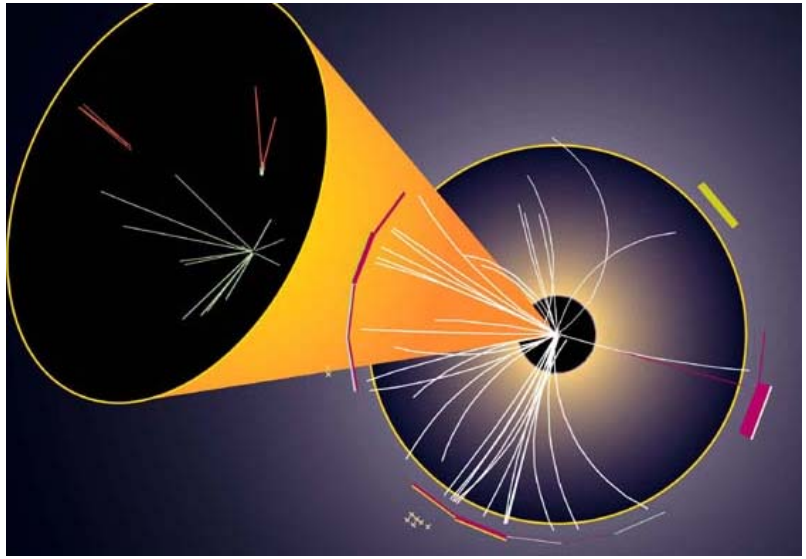
Marcel Demarteau

For the Fermilab Detector & Physics R&D Group

FRA Physics Visiting Committee
April 25-26, 2008

The Next Generation

- The next generation detectors will emphasize precision
  - Collider experiments: results from the LHC will be the guide
  - Fixed target experiments: deep probes of (possible deviations of) the Standard Model
- Precision detectors fully reconstruct the final state over the full angular region
- Their performance is required to go about one order of magnitude beyond what has been achieved to date



- Approach taken at Fermilab for detector R&D:
  - We pursue those technologies that we believe are the most promising, despite (or because of) the fact that some seem very challenging
  - Work with a long time horizon within the base of existing strengths
  - Pursue those technologies that have a broad range of applicability, that is, a balanced approach between generic "Horizontal" detector R&D versus concept driven "Vertical" detector R&D
  - Establish collaborative efforts as much as possible and support the user community through the support of many test-beam experiments

Foci at Fermilab

- ***Development of the silicon 3D vertical integration technology with application to pixel detectors and the study of the SOI technology for particle detectors***
  Establish the silicon 3D vertical integration technology and study the feasibility of the SOI technology for particle physics detectors. Apply the technology for the development of new pixel technologies and their associated readout.

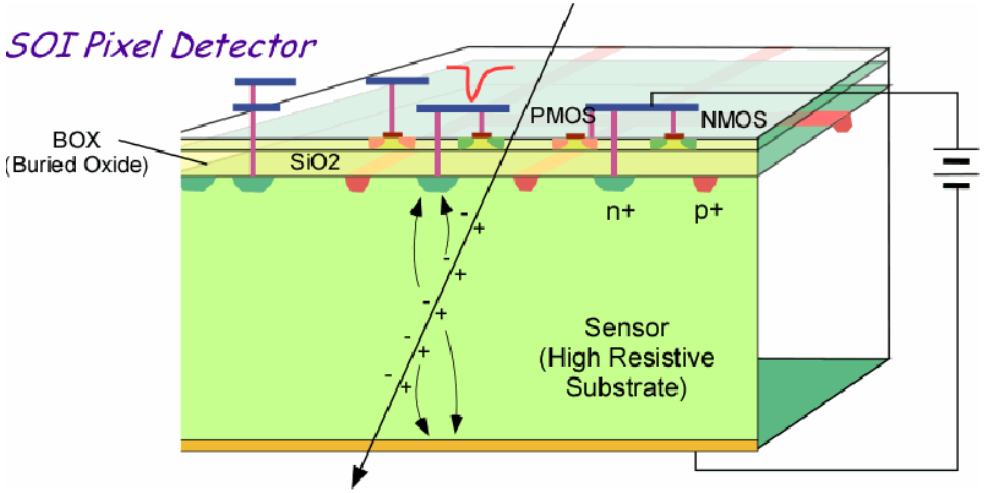
- ***Development of low-mass silicon vertex detectors and trackers***
  Develop designs of low mass mechanical support structures for vertex detectors and trackers with special emphasis on the forward regions. Concurrently develop the tracking software enabling optimization of the detector design

- ***Characterization of Geiger-mode Avalanche Photo Diodes and their application in the development of total absorption dual readout calorimetry***
  Geiger-mode Avalanche Photo Diodes for the detector of photons, hold excellent promise for many different applications. Device characterization is pursued together with the development of readout technology and their application in scintillator-based detector readout for scintillator and crystal based total absorption dual readout calorimetry and muon detection.

- ***Test Beam***
  Support test beam activities to test new detector technologies. The beam line at Mtest has been redesigned to accommodate the needs of the community and improvements to the beam line instrumentation and data acquisition are being implemented.

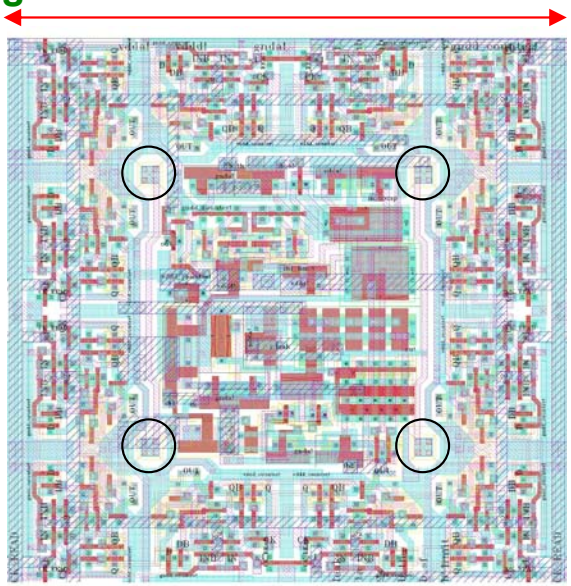
- ***Physics Community Outreach***
  Organize and host many workshops with broad reach

SOI Detectors



- **Bonded SOI Wafer**
  - low resistive top layer; standard CMOS Electronics (NMOS, PMOS)
  - separated through a Buried OXide (BOX) layer to
  - Bottom substrate layer which forms detector volume; diode implants are formed beneath the BOX and connected by vias

- **Designed MAMBO Chip in the OKI (Japan/KEK) 150 nm process**
  - MAMBO: Monolithic Active pixel Matrix with Binary cOunters
  - A wide dynamic range counting pixel detector plus readout circuitry, sensitive to 100-400 keV electrons, high energy X-rays, and mips
  - OKI process incorporates diode formation by implantation through the BOX
- **Design submitted Dec. 15, '06 received June '07**
- **Chip characterized**
  - Significant differences with simulation
- **Submitted new design March '08 in the OKI (Japan/KEK) 200 nm process**



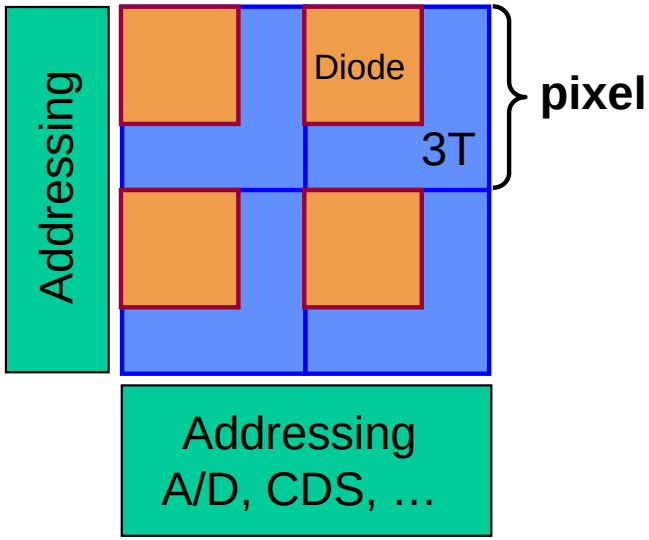
Vertical Integrated Circuits – 3D

- "Conventional MAPS"
  - Pixel electronics and detectors share area
  - Fill factor loss
  - Co-optimized fabrication
  - Control and support electronics placed outside of imaging area

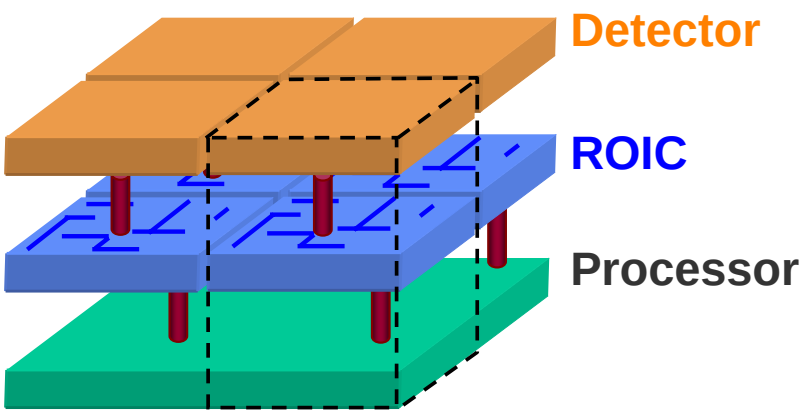
- 3D Vertical Integrated System
  - Fully active sensor area
  - Independent control of substrate materials for each of the tiers
  - Fabrication optimized by layer function
  - Local data processing
  - Increased circuit density due to multiple tiers of electronics
  - 4-side abuttable

- Technology driven by industry
  - Reduce R, L, C for higher speed
  - Reduce chip I/O pads
  - Provide increased functionality
  - Reduce interconnect power, crosstalk

Conventional MAPS

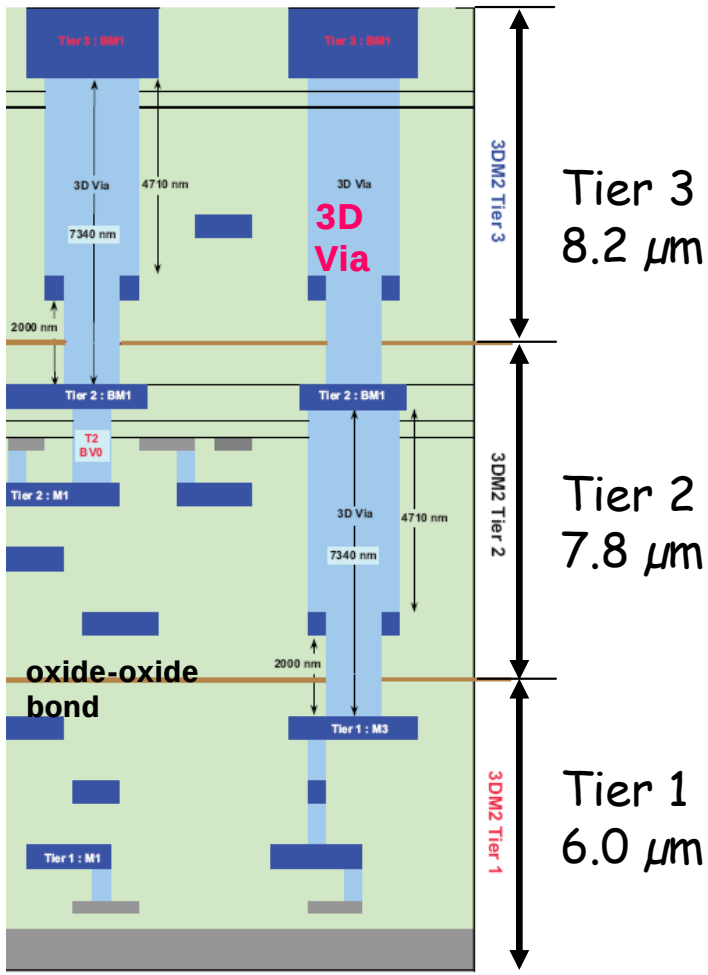


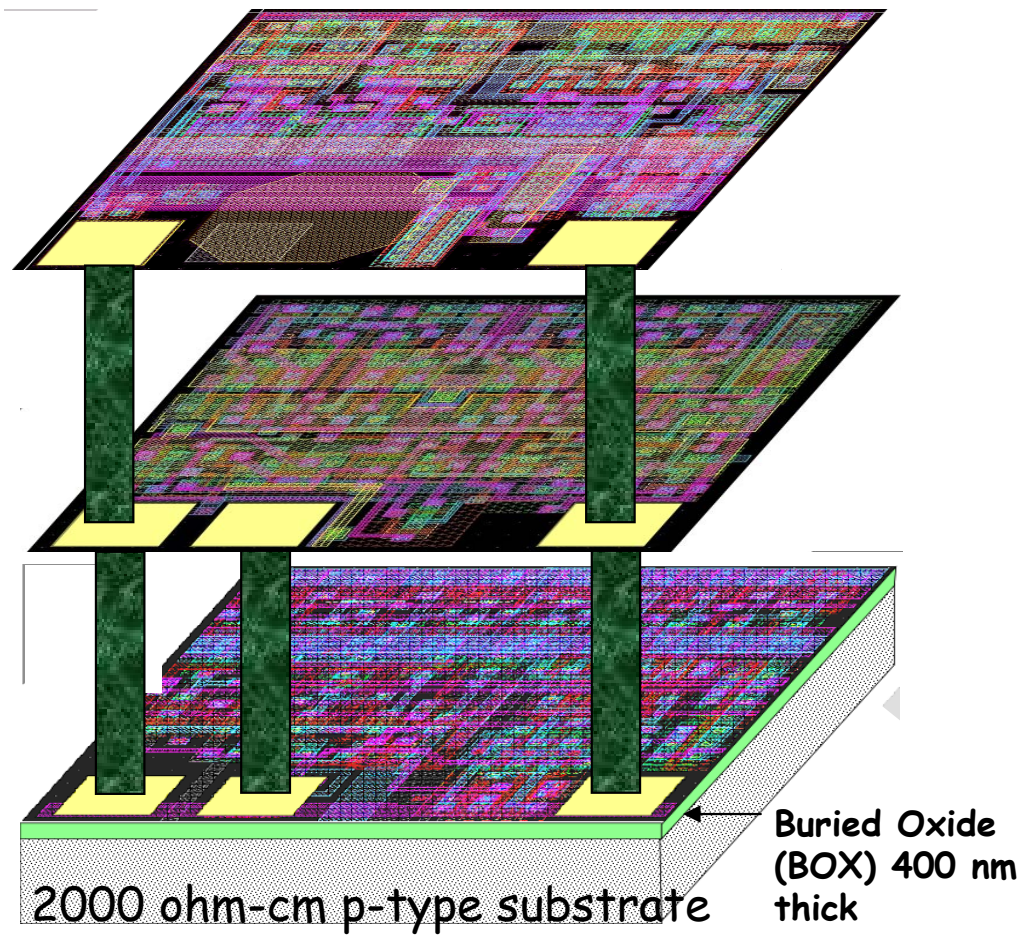
3-D Pixel



VIP Chip

- **3D chip Vertical Integrated Pixel (VIP) chip submitted by Fermilab to DARPA funded MIT-LL 0.18 μm 3D SOI process on Oct. 15, 2006**
  - **Chips received back early 2008; key features:**
    - Analog pulse height, sparse readout, high resolution time stamp, front-end power ~ 1875 μW/mm^2 (before cycling), 175 transistors in 20x20 μm^2 pixel

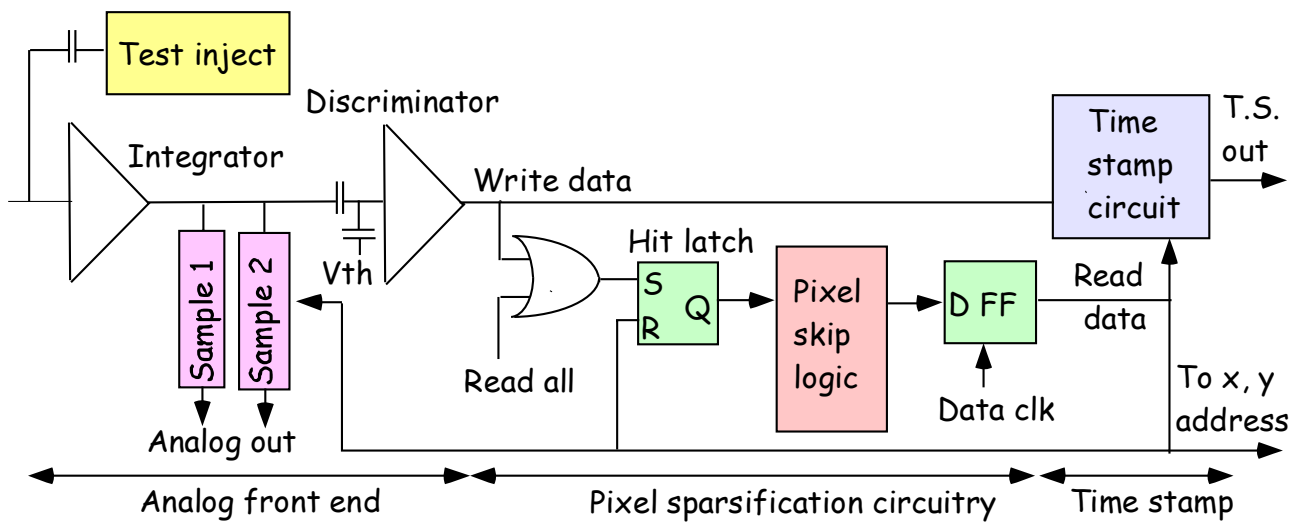




Architecture of Demonstrator Chip

- **Design:**
  - **Analog and binary readout information**
  - **Time stamping of pixel hit for ILC environment**
    - Divide bunch train into 32 (5 bit) time slices
  - **Sparsification to reduce data rate**
    - Use token passing scheme with look-ahead to reduce data output
      - During acquisition, a hit sets a latch
      - Sparse readout performed row by row with x- and y-address stored at end of row and column
  - **Chip divided into 3 tiers**
    - Design for 1000 x 1000 array but layout only for 64 x 64 array.
  - **Chip received Nov. 20, 2007**

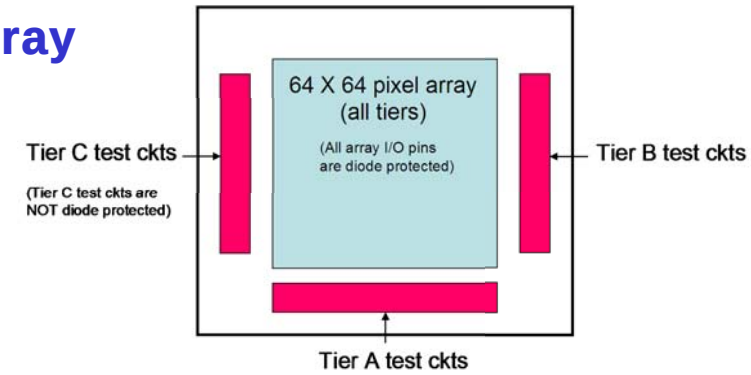
- **First design which, in principle meets 'all' of the ILC requirements for thickness, resolution, power dissipation, time stamping**
  - **Power is 0.75 microwatt/pixel ~ 18.75 microwatts/mm² (after pulsing)**
  - **Noise is ~30-40 e^-**
  - **S/N = 100-200:1**



Schematic pixel cell block diagram

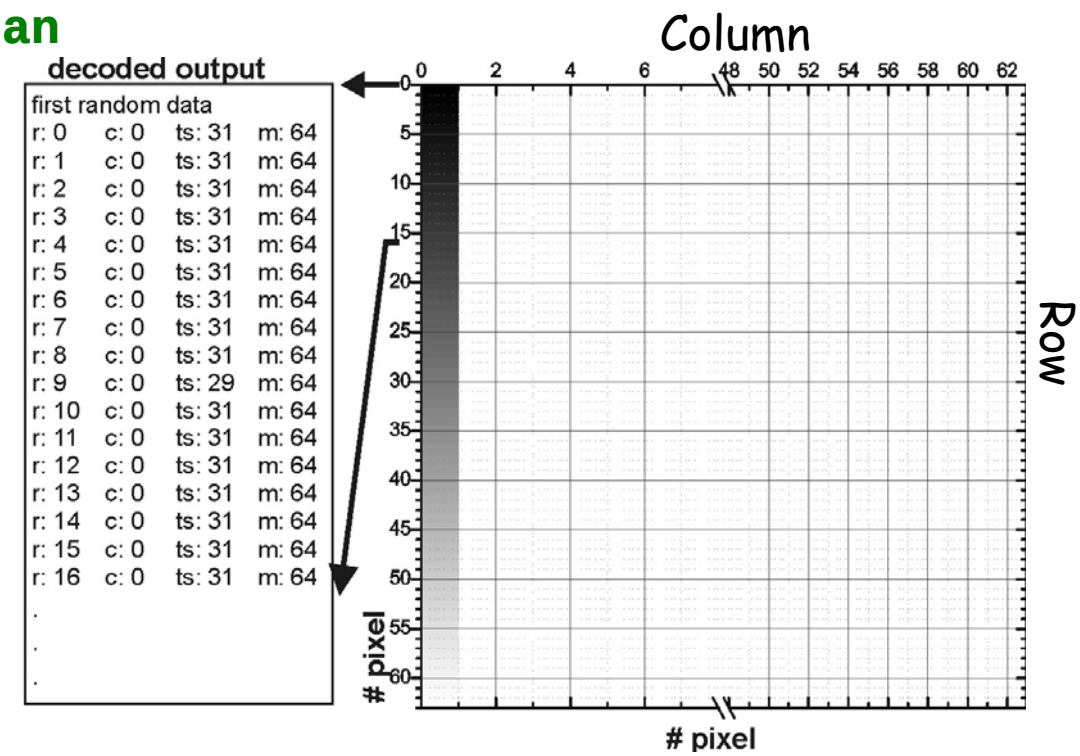
VIP Test Results

- Received ~6 functioning chips
- Chip is divided into test structures and 64 x 64 array



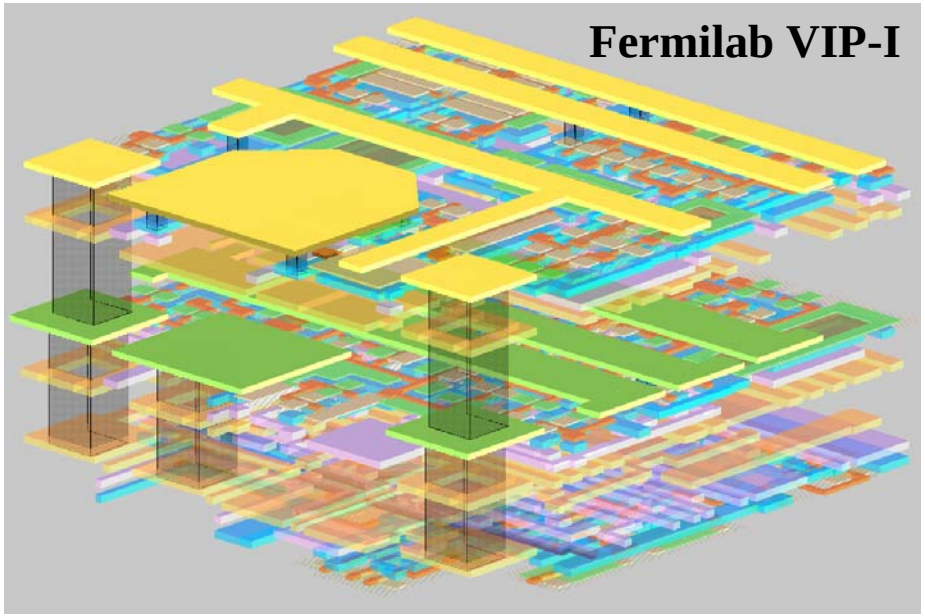
- Test structure results for individual tiers
  - Chip does not operate at nominal voltages
  - Ramp circuit jitter from chip to chip
  - Some parts work on some chips
  - Noise causes jitter in ramp timing
  - Performance is a little faster than simulations on some tiers

- Full array tests
  - Digital test results
    - Serial readout for address partially working on some
  - Analog test results
    - Analog pedestals measured for full array



Next Steps with MIT-LL

- **MIT-LL VIP process has some shortcomings**
  - **Processing problems**
    - Trapped charge between tiers 2 and 3 during fabrication
  - **Other design problems**
    - ESD protection diodes are very leaky; serious problems for circuits with analog inputs
    - Current mirrors not working properly
  - **Significant chip-to-chip variations**
  - **Yield is poor, reasons not understood**
  - **Measurements disagree with simulations**
  - **Long turn-around time**
  - **Not a commercial process**
  - **Discussions are ongoing with other users**



- **MIT-LL has new DARPA sponsored 3D run in September '08 – feature size 130nm, SOI, 3 tiers**
  - **Fermilab will submit version 2 of the VIP chip addressing all known shortcomings**

3D Initiative with Commercial Vendor

- Fermilab started an initiative with a local vendor who is one of the leaders in 3D: Tezzaron, based in Naperville (and Singapore) http://www.tezzaron.com/
- Tezzaron has fabricated a number of 3D chips for commercial customers
  - Memory devices and CMOS sensors

- Process Characteristics/Flow
  - Wafers with "Via First" process are made at a commercial foundry: Chartered Semiconductor in Singapore
  - Wafers bonded in Singapore by Tezzaron
    - Facility can handle up to 1000 wafers/month
  - Bonded wafers are finished by Tezzaron
    - (Bump) Bond pads

- Potential Advantages
  - Lower cost and faster turn around
  - One stop shopping
  - Process is available to customers from all countries

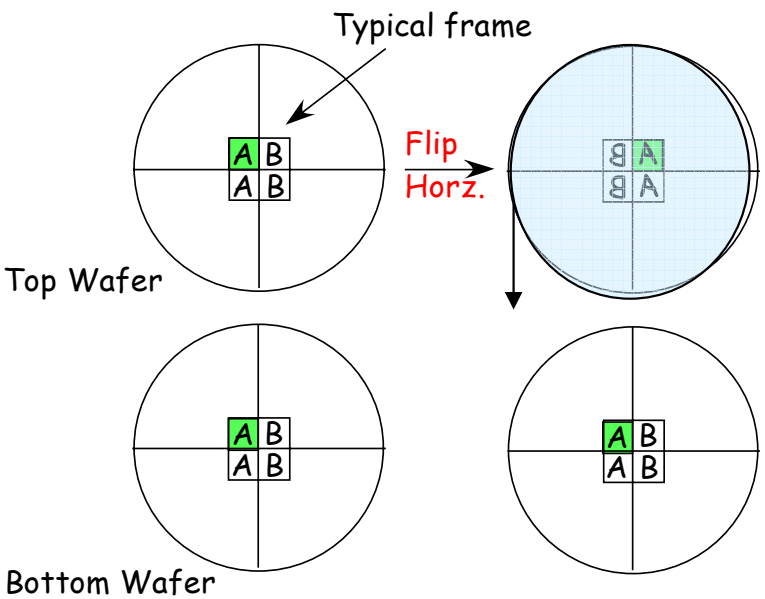
Chartered Semiconductor Manufacturing

- Chartered Semiconductor Manufacturing fourth largest dedicated independent commercial semiconductor foundry, located in Singapore
  - Extensive line of CMOS and SOI processes from 500 nm down to 45 nm
  - Common Chartered-IBM platform for processes at 90 nm and below
  - Chartered 130 nm process is similar to the IBM 130 nm process but has different layer arrangement and transistor thresholds
  - Commercial tool support for Chartered Semiconductor
  - Chartered produced nearly 1,000,000 eight inch wafers in the 130 nm process

- Chartered 130 nm mixed signal CMOS process for 3D integration
  - 8 inch wafers
  - Reticle size 24 x 32 mm
  - Features:
    - Deep N-well
    - MiM capacitors – 1 fF/um2
    - Single poly
    - 8 levels of metal

Fermilab 3D Multi-Project Run

- Fermilab will be submitting a 3D multi project run to Tezzaron
- There will be only 2 layers of electronics fabricated in the Chartered 130 nm process, using only one set of masks. (Useful reticle size is 16 x 24 mm)
- The wafers will be bonded face to face
- Bond pads will be fabricated for bump bonding to be done later at Ziptronix
- Open invitation offered to community to participate
  - Interested parties
    - Received LOI from CNRS/IN2P3
      - Strasbourg
      - Orsay – LAL
      - Paris 6/7 - LPNHE
      - Marseille – CPPM
    - Received LOI from INFN, Bergamo
    - Other groups have expressed interest



Note: top and bottom wafers are identical.

UNIVERSITÀ DEGLI STUDI DI BERGAMO
FACOLTÀ DI INGEGNERIA

Bergamo, April 18th, 2008

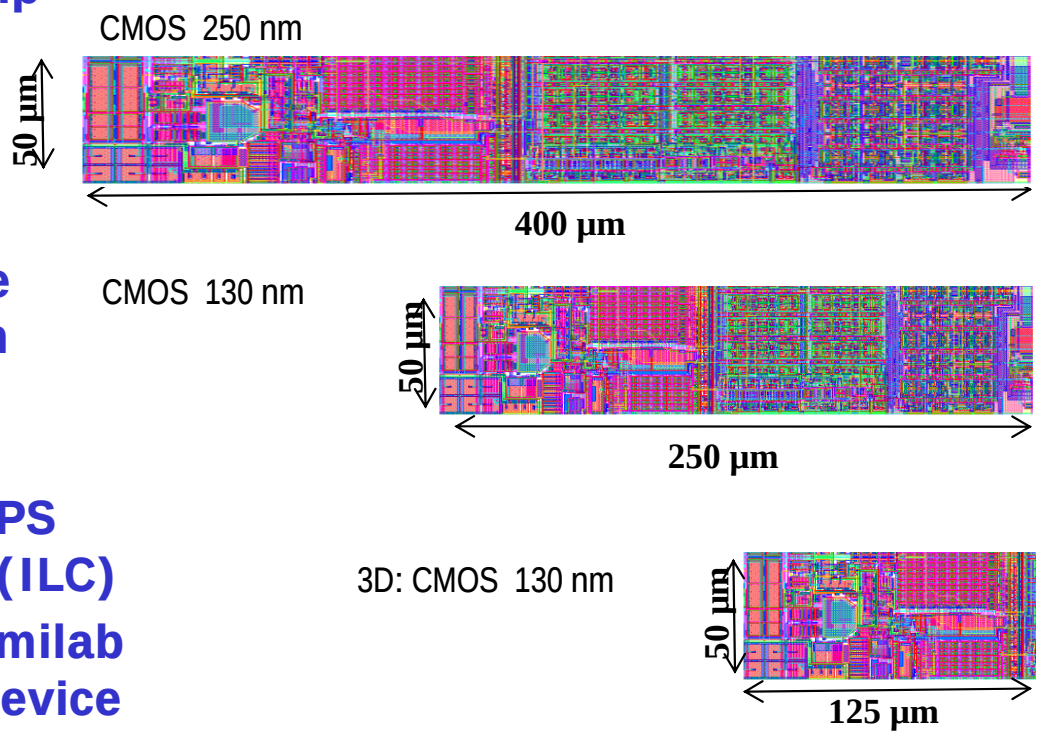
Ray Yarema
Head of the Electrical Engineering Department
Fermi National Accelerator Laboratory
Batavia, IL

Participation to Multiproject Engineering Run with Tezzaron

Candidate Projects for 3D MPW Run

- Fermilab intents to submit a redesign of the VIP chip, adopted to 2 tiers
- Fermilab intends to develop a 3D chip to explore the advantages of 3D for the sCMS pixel detector (LHC)
- CPPM has expressed interest in converting the current 0.25 um ATLAS pixel design to a 3D structure with 2 tiers in the Chartered 130 nm process (LHC)
- Strasbourg proposes to work with Fermilab to develop a simple 3D MAPS device with 7 bits of time stamping (ILC)
- Bergamo proposes to work with Fermilab to develop a 3D version of a MAPS device using deep n-well with sparsification and time stamping (ILC/Super b-factory)

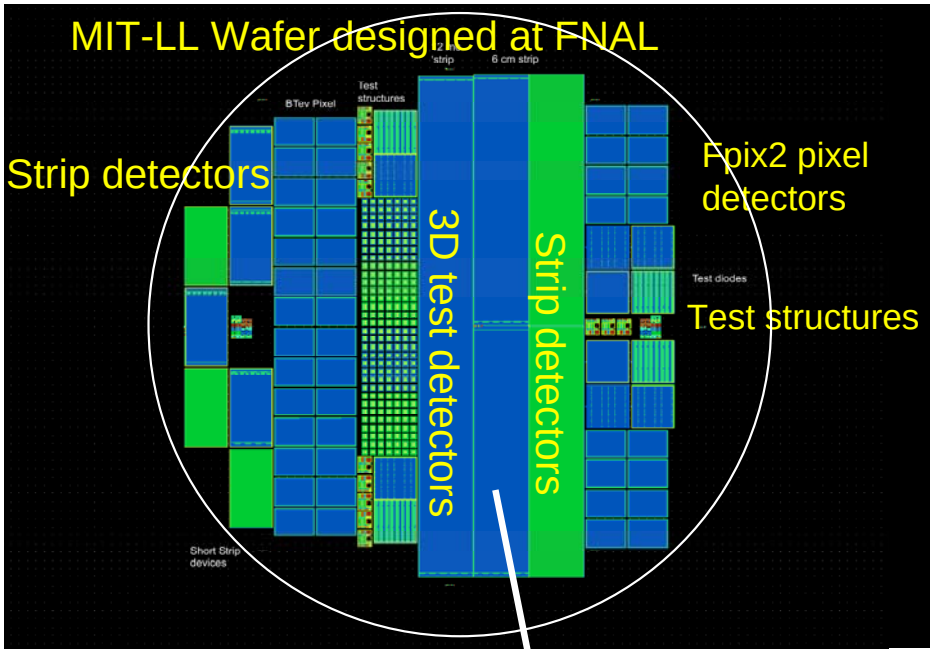
ATLAS Example



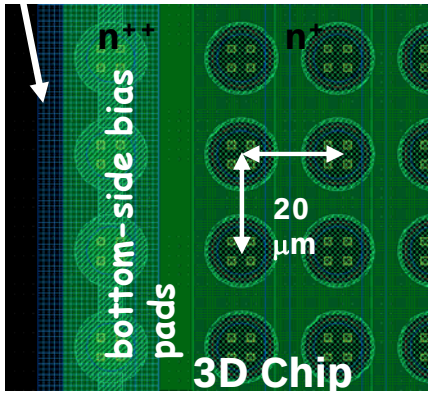
- Truly generic detector development with international base

Towards Integrated Detectors

- Ultimate goal is to have integrated unit of front-end electronics and thin (~50μm thick) fully depleted detectors with very fine pitch
- Concurrent with 3D readout development, developing thin sensors with fine-pitch readout to be bonded to 3D readout devices
- Sensor Issues:
  - Development of edgeless sensors
  - Sensor thinning and laser annealing
  - Device bonding

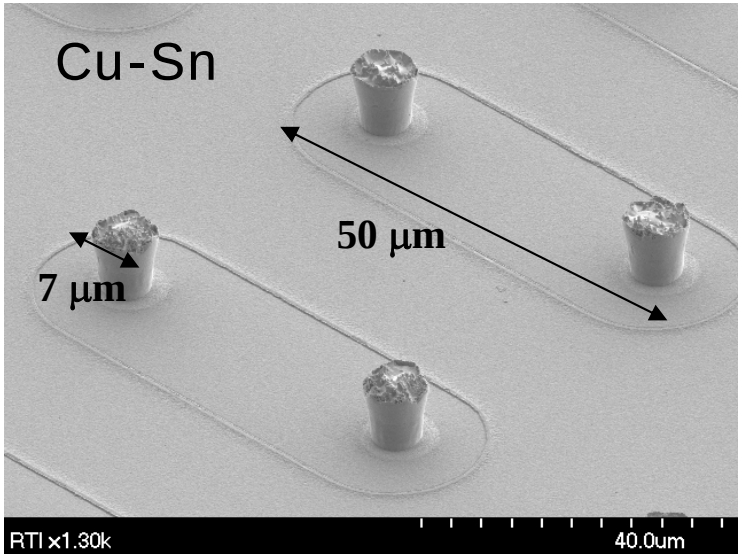


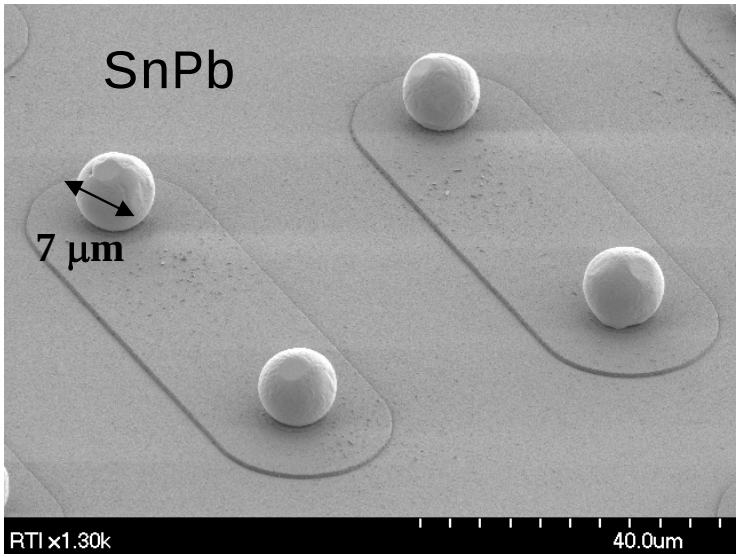
- Thin edgeless sensors
  - Designed sensors on 6" n-type wafers to be bonded to 3D chips
  - Sensors fabricated at MIT-LL
  - Thinned to 50, 75, 100 μm, implanted and laser annealed
  - Deep trench etch, n doped poly-silicon fill provides edge doping
  - Sensors sensitive to the edge, 4-side abuttable, i.e. no dead space

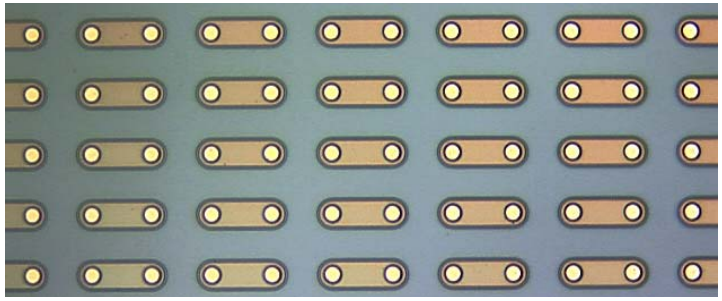


Device Bonding

- **Developed, in collaboration with RTI (NC), bump bonding process compatible with pixilated devices having a 20 μm pitch**
- **Completed design and fabrication of passive test structures based on 50 μm pitch, but using bumps compatible with 20 μm pitch**
- **Two test structures designed for testing**
  - **CuSn bonded to Cu**
    - Cu-Sn: 7 μm diameter bump
    - Cu: 11 & 15 μm diameter bumps
    - 176 x 128 bump array (22528 bumps) 50 μm pitch in x and y
  - **SnPb bonded to Ni/Au**
    - SnPb: 7 μm diameter bump base
    - Ni/Au: 7 μm diameter bond pads
    - Daisy chains connecting 22 bumps

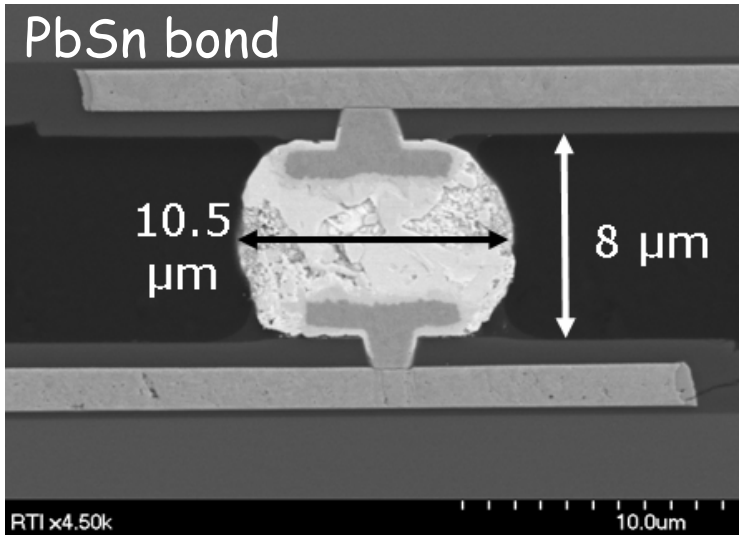




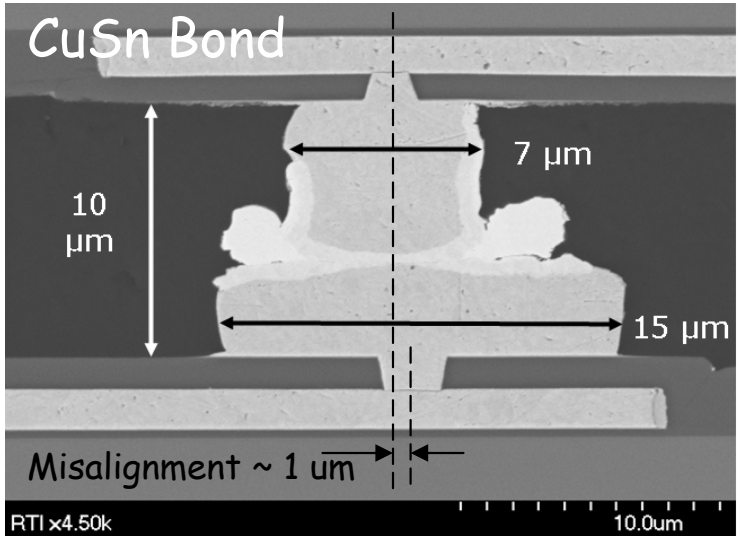


Fine Pitch Bump Bond Feasibility

- **Results from tests**
  - **Bond yield of 10 μm PbSn balls poor**
  - **Bond yield of 7 μm CuSn on 11/15 mm Cu pad was 99.995%**
  - **All CuSn bonded chips had die shear strengths greater than the strongest PbSn bonded chip**
  - **Interconnect resistance 10~27 mΩ**



- **Established feasibility of CuSn bonding for fine pitch (20 um) assembly of 3D circuits and could apply these processes to functional 20 μm pitch devices that we have in hand**
  - **Both PbSn and CuSn bonds can represent a high X_o for fine pitch assemblies or high density interconnects**

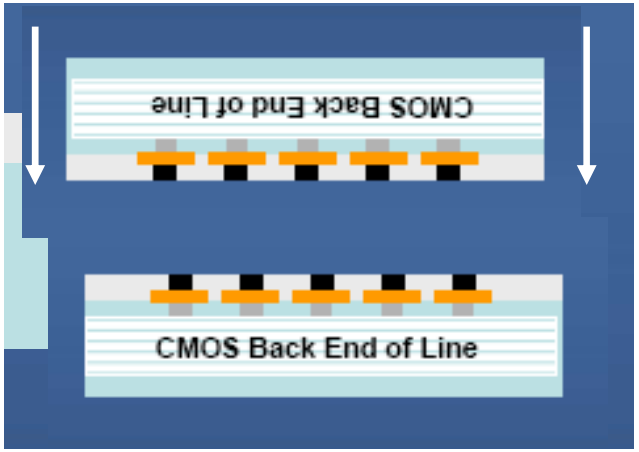


- **As next step pursuing different technology that constitutes lower mass**

Direct Bond Interconnect

- **CuSn bump bonds pose a problem for low mass fine pitch assemblies**

- **Pursuing IC bonding to a detector with Ziptronix (NC) using the Direct Bond Interconnect (DBI) process**
  - **Significantly reduces material budget**
  - **Tezzaron and Ziptronix are industrial partners**
  - **Understood bond yields for 10 μm pitch with 1Mbonds/cm^2**



- **Work plan with Ziptronix:**
  - **DBI process sensor and readout wafers**
    - Including MIT-LL wafers and FPIX wafers
    - Thin the sensor chips to 50 microns and polish thin readout wafer to 100 microns
    - Dice the bonded pairs

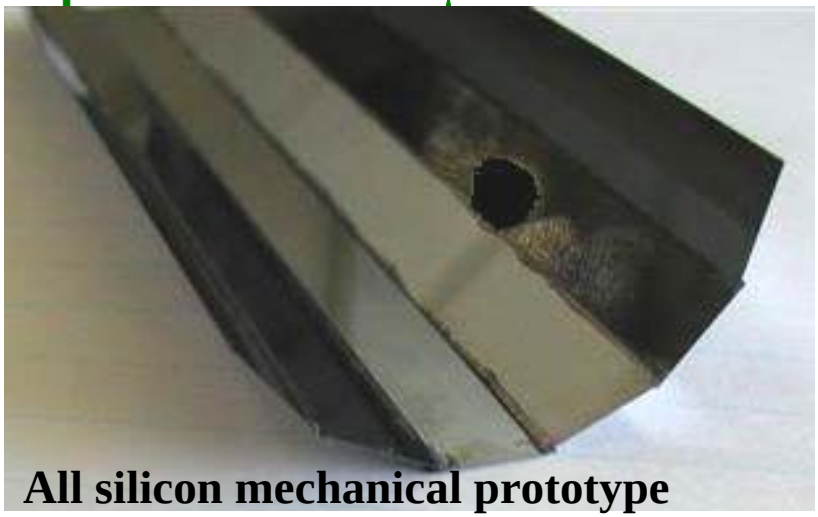
- **Deliverable: >25 bonded pairs for further processing and testing**

DBI:
- **Plate DBI (magic) metal**
- **Deposit oxide, terminate surface with amine group**
- **Bring surfaces in contact**
  - $Si–NH_2 + Si–NH_2 \rightarrow Si\text{-}N\text{-}N\text{-}Si + 2H_2$
  - Bonding occurs at RT
  - Bond strength increase with t
- **After oxide bond is strong enough, wafers are heated to form thermo compression bond between Magic Metal implants.**

Pixel Detectors Mechanical Design

- **Multi-layered, high precision, very thin, low mass detectors**
  - **Goal: layer thickness of 0.1% X_0 per layer, equivalent of 100 μm of Si**

- **Carbon-fiber Supports**
  - **Collaborating with the UW on thin-walled carbon-fiber support structures**
    - Three prototype half-shell structures fabricated for evaluation and testing
    - Significant CTE issues below T ^{0}C


All silicon mechanical prototype

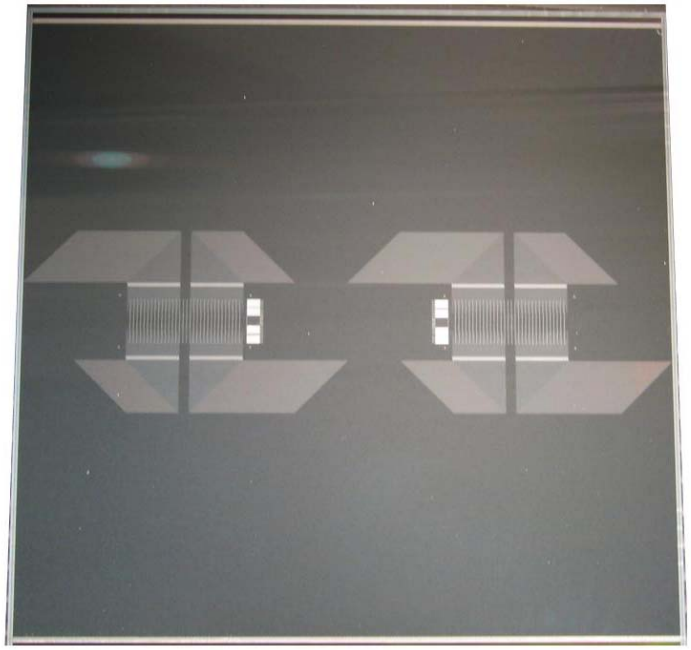
- **All Silicon Structures**
  - **Collaboration with Rutherford on all silicon structures, proposed to mitigate CTE issues**
  - **Sensors glued to one another along edges by thin beads of epoxy and supported by thin, flat carbon fiber/epoxy end membranes**

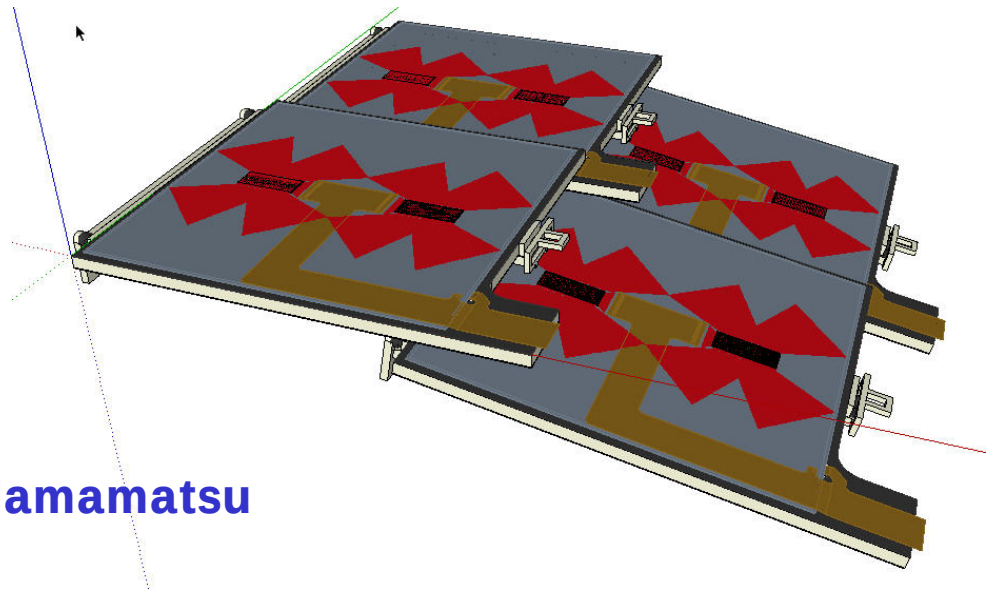
Layer	Gravity (μm)	Δx (μm)	Δy (μm)	Δz (μm)
1	0.1	0.9	1.8	5.3
2	0.1	1.0	3.0	5.6
3	0.3	1.6	4.0	5.8
4	0.6	2.6	5.7	6.2
5	1.4	4.4	8.1	6.6

- **Table shows FEA study of gravitational sag and maximal displacements for a ΔT of 10 ^{0}C**

Low Mass Tracker Design

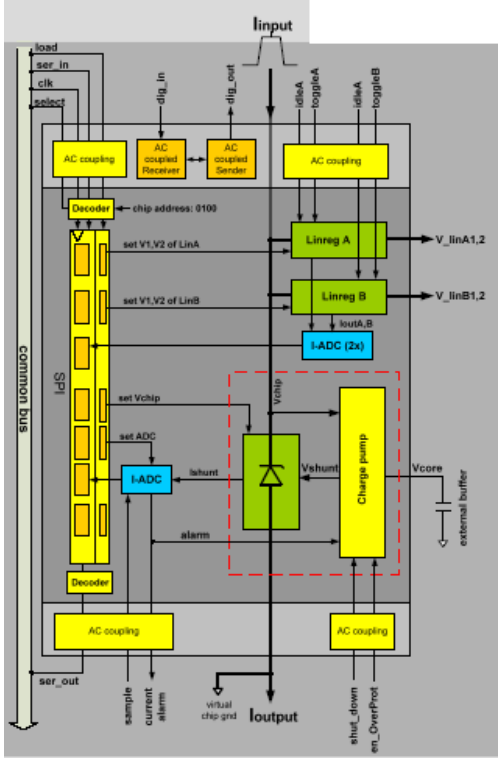
- In collaboration with SLAC, developed:
  - Low mass design for an outer tracker
  - Low mass module design for tracker
  - Hybrid-less sensor
- Sensor design uses bump-bonded readout chip
  - Sensor size 93.5mm x 93.5mm
  - Strip/Readout pitch 25 / 50 μm
  - Number of RO (IM) strips 1840 (3679)
    - Need two readout chips (kPix)
  - Double metal layer optimized for strip geometry
    - Minimize capacitance and balance with trace resistance
  - S/N goal of 25
- Module design
  - CF/Rohacell/CF frame: ~50% void
- Sensors delivered March 28, '08 from Hamamatsu





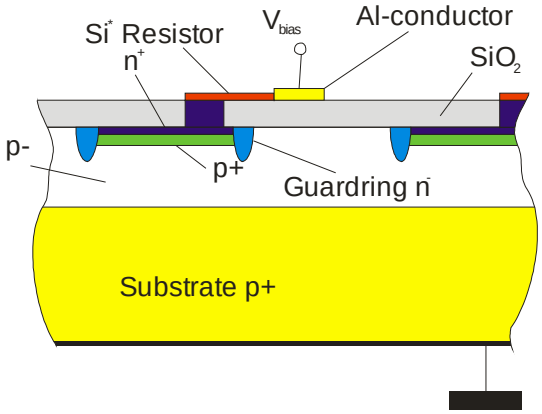
Power Issues

- LHC experiment suffer (dramatically) from ‘ cable pollution’
  - Large number of channels / detector modules
  - Long power cables (50-110 m)
  - Power (~50kW) only 20-50% efficient
  - Large contribution to material budget
- SLHC trackers will have 5 - 10 times more channels than today’s
- Peak and average power are crucial issues for the next generation of particle detectors; serial powering (current recycling) can lower instantaneous current
  - Reduction of cable volume by factor 10-20
  - Increase of power efficiency by factor 2-5
- Fermilab has designed a serial powering chip (SPi)
  - Collaboration with Penn/RAL (to be submitted May ’08)
  - Architecture:
    - External shunt regulator + External shunt transistor
    - External shunt Reg + parallel shunt transistors in ROIC
    - Shunt regulator being capable of regulating up to 1A between 1.5V and 2.5V
    - Two linear regulators (analog and digital) switchable between downloadable voltages ~ 1.2 to ~2.5V @ 500mA each
    - 6 bit flash ADCs to monitor shunt and LR current
    - Core voltage for chip control (1.5 to 2.5V)
    - TSMC 0.25 micron (radiation tolerant design)

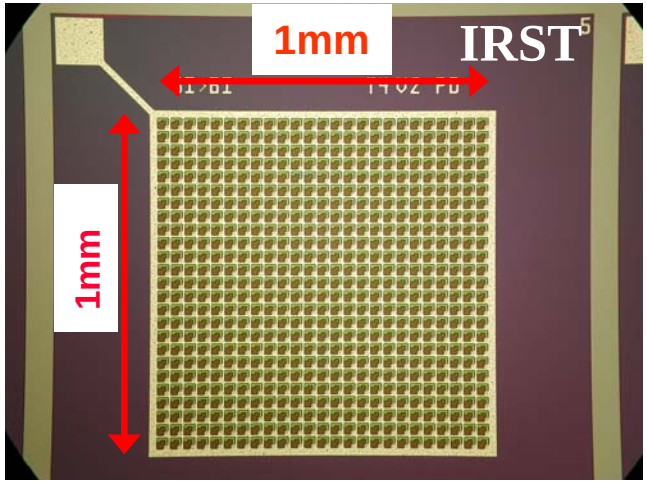


Geiger-Mode Avalanche Photo Diodes

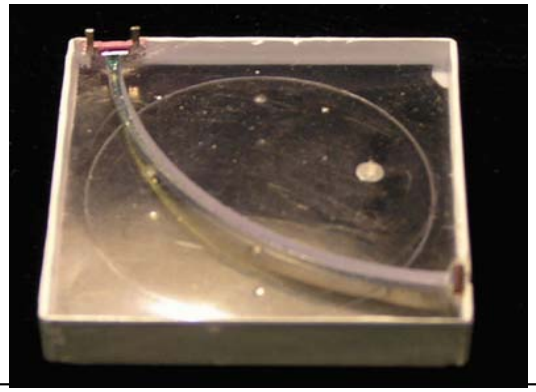
- **Avalanche photodiode operating in Geiger mode, also called Multi-Pixel Photon Counter (MPPC) or Silicon photo-multiplier (SiPM), PPD, …**
  - **Array of pixels connected to a single output**
  - **Signal = Sum of all cells fired**
  - **If probability to hit a single cell < 1 => Signal proportional to # photons**



- **Characteristics:**
  - **Pros**
    - Very compact, High PDE (15~20% for 1600 pix)
    - Insensitive to magnetic field
    - High gain (10^5~10^6), good timing resolution
    - Operational at V_{bias}=70~80 V
  - **Cons**
    - Thermal noise rate (100kHz~300kHz @ 0.5 pe)
    - Response is non-linear due to limited number of pixels (saturation effect)
    - Sensitive to temperature change
    - Cross-talk and after-pulsing



- **Multiple applications**
  - **Dual readout, lead-glass – scintillator sampling calorimetry**
  - **Analog scintillator tile hadron calorimeter**
  - **Muon detector based on scintillator strips**

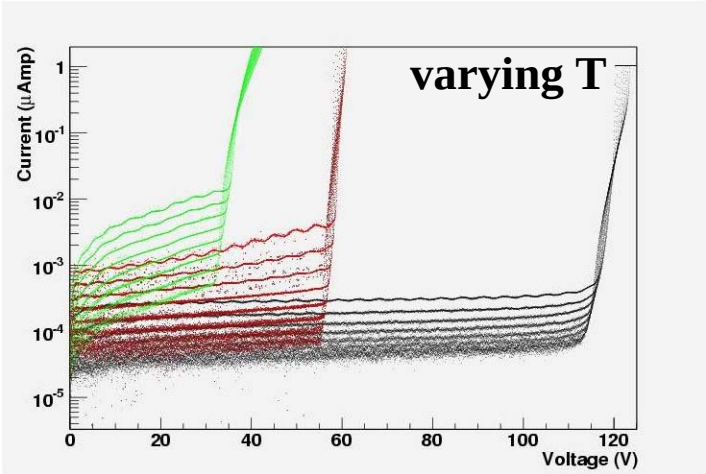


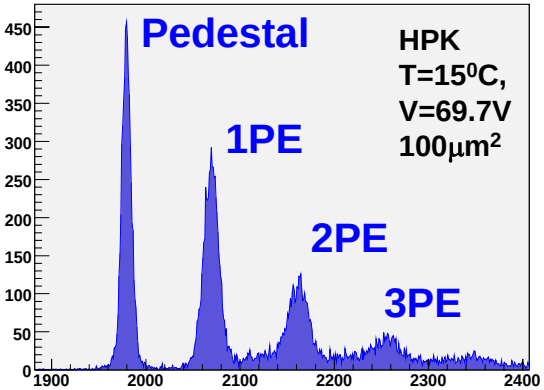
3x3x0.5 cm^3
UNIPLAST
1 mm WLS
Kuraray fiber
Y11(300)

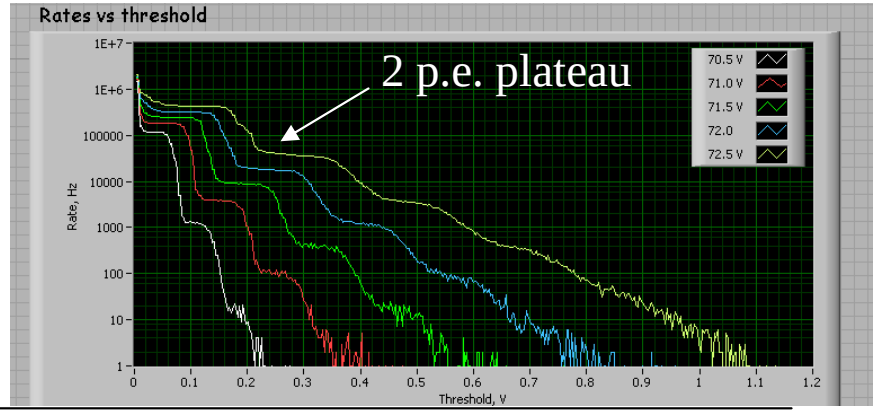
PPD Characterization and Plans

- Developing tools for complete characterization of the detector response
- Four step program envisioned
  - Characterize and understand the detector response
  - Develop a method for selection of the operating conditions and the effective calibration of the detectors
  - Develop an integrated read-out chip
  - Work with industry on their development

- Develop strategies and calibration procedures for multiple applications and synergies
  - Use the detectors for measurement of light yield and timing characteristics for dual readout calorimetry
  - Muon detection
  - CMS interest as potential replacement of HPD's
  - MPPC's are baseline for T2K for which Fermilab provides the readout
  - (Medical imaging)

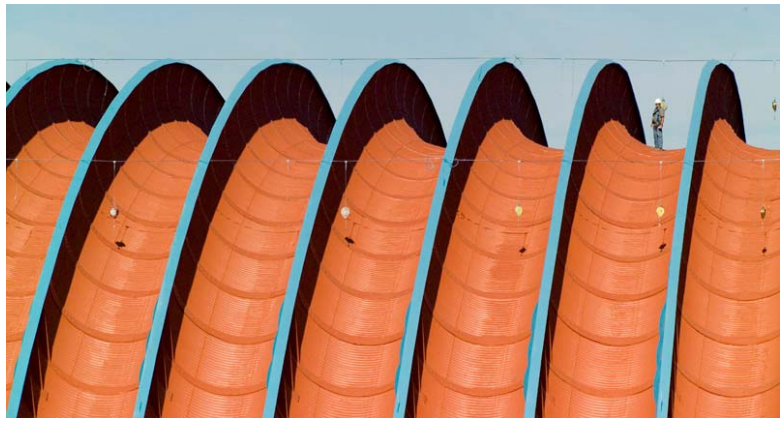


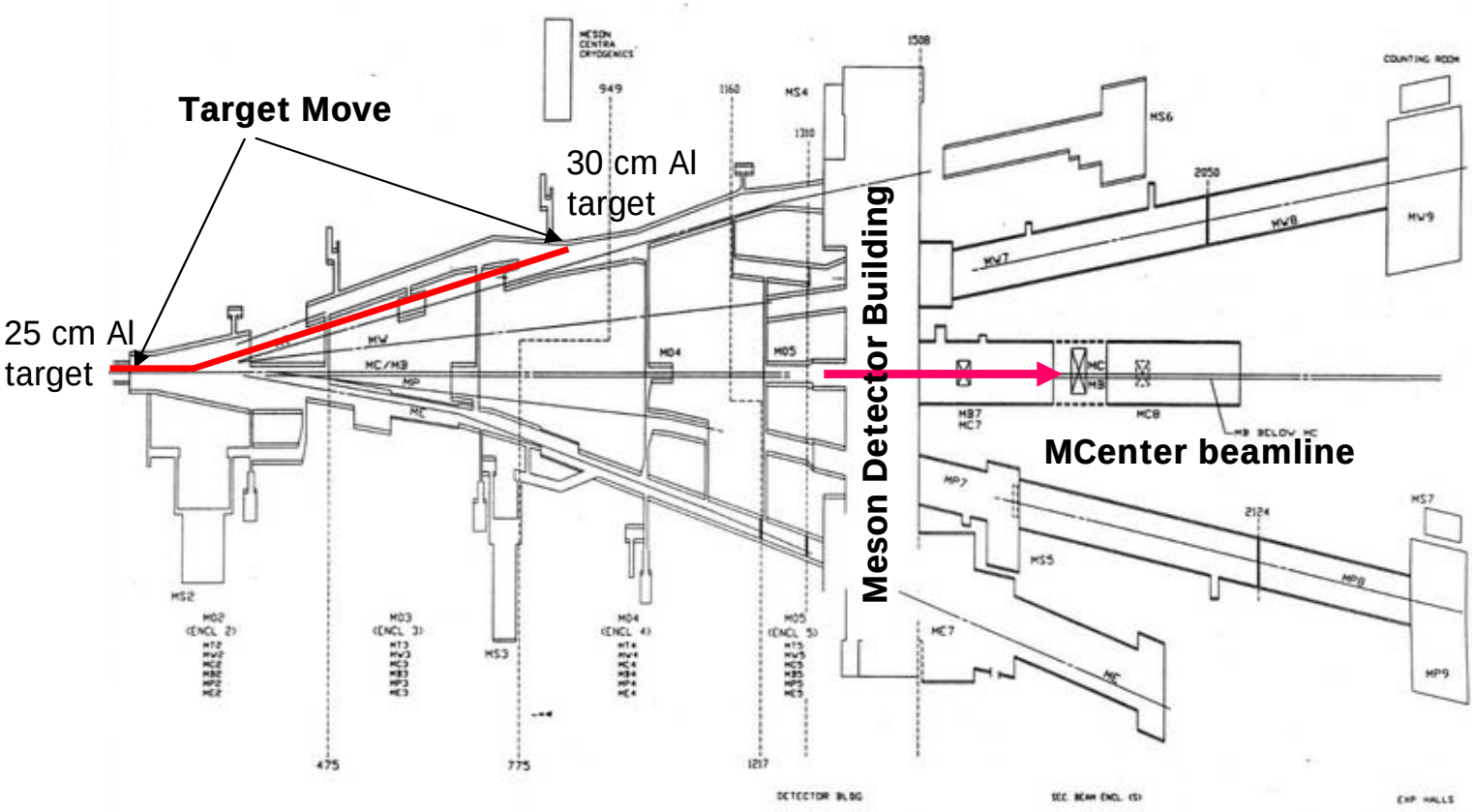




Test Beam Facility

- The old Fermilab Meson Test Beam Facility (MTBF)
  - Could not deliver a pion beam lower than 4 GeV
  - Electrons had a low flux because of significant material in the beam
- We recognized the scarcity of test beams, which will be the lynchpin for new detector development
- We should support the community by providing the infrastructure for beam tests





Proton Mode:
120 GeV protons transmitted through upstrm target

Pion Mode:
8-66 GeV beam tuned for secondrs from upstrm target

Low Energy Pion Mode: 1-32 GeV beam tuned for secondrs from new dwnstrm target

Current Performance

- **Moving the target to MT3 (L=1273-1388' goes to L= 451-566') reduces the decay length for pions and reduction of the material in the beamline**

Tune (GeV)	Old Rate for 1E12 PPS from MI	New Rate for 1E11 PPS from MI	e- fraction	Energy Resolution
1	---	~60K	>90%	~10%
2	---	~60K	90%	~7%
3	~150			
4	~500	~55k	67%	2.4%
8	~5K	~80k	45%	5%
16	~20K	~130k	13%	1.2%
33	~30K			1.0%
66	~100K			
120	~800K			

Blue = proton mode

Green = pion mode

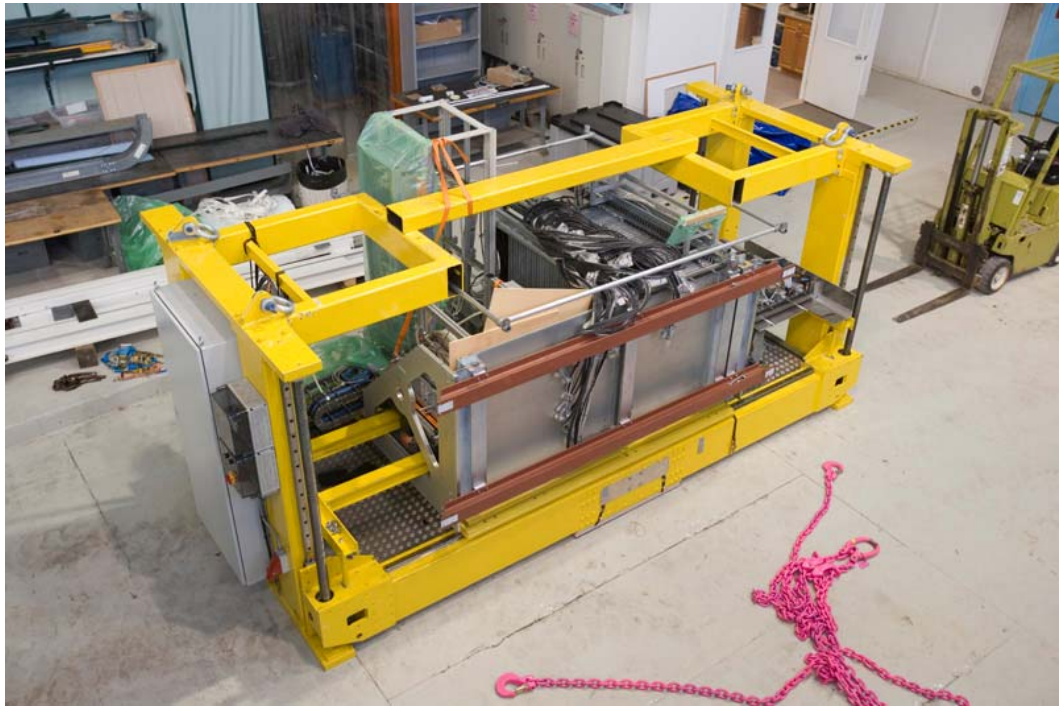
Red = low E mode

	Beam Composition	
	16 GeV	8 GeV
Positrons	20%	30%
Muons	2-5%	10-15%
Pions	45-50%	15-20%
Protons	30%	30-40%

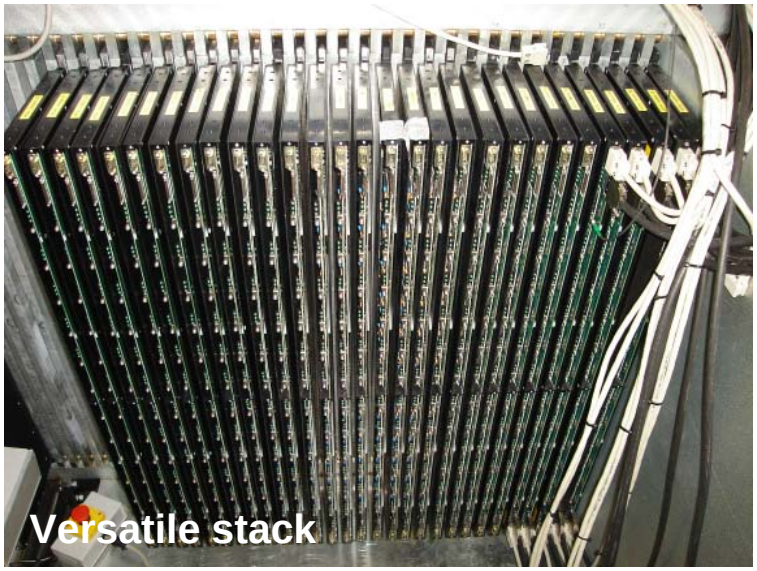
- **Note:**
  - **Upstream target moved out of the beamline for the Low Energy mode. Flux improved orders of magnitude**
- **Very positive feedback received from community on refurbishing beam line**
- **Many users lined up to use the facility long term, notably CALICE collaboration**

Test Beam Users

- April 7-25 CALICE installation
- May 7-27 CALICE running
- June 2-10 LHCb
- June 2-10 MINERVA installation
- June 11-17 Ultra-fast timing
- July 7-29 CALICE running
- August 15-25 Monolithic pixels
- September CALICE running
- September MINERVA running

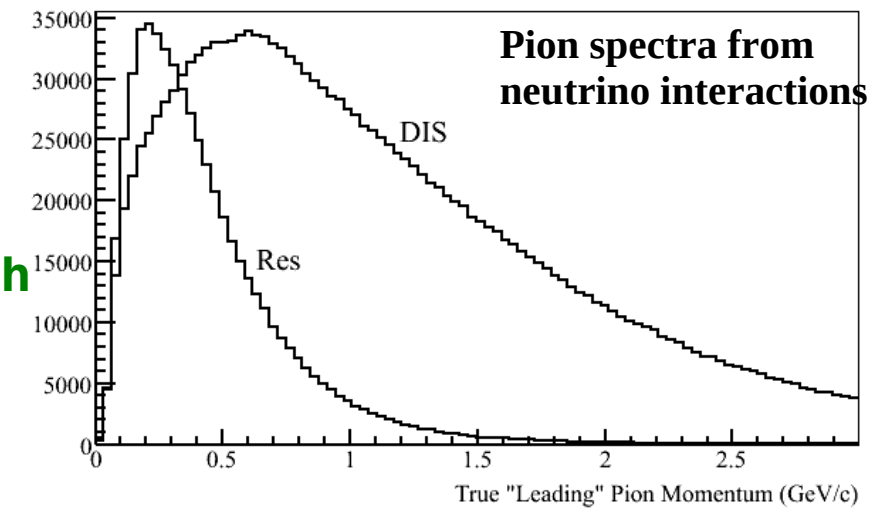


- CALICE
  - currently setting up in Mtest
    - ECAL: Si/W
    - HCAL: scintillator / Fe
    - Tailcatcher
  - CALICE beam test will be of critical importance in establishing the concept of particle flow calorimetry with various technologies (scintillator, RPC, GEM) and readout architectures (analog, digital)

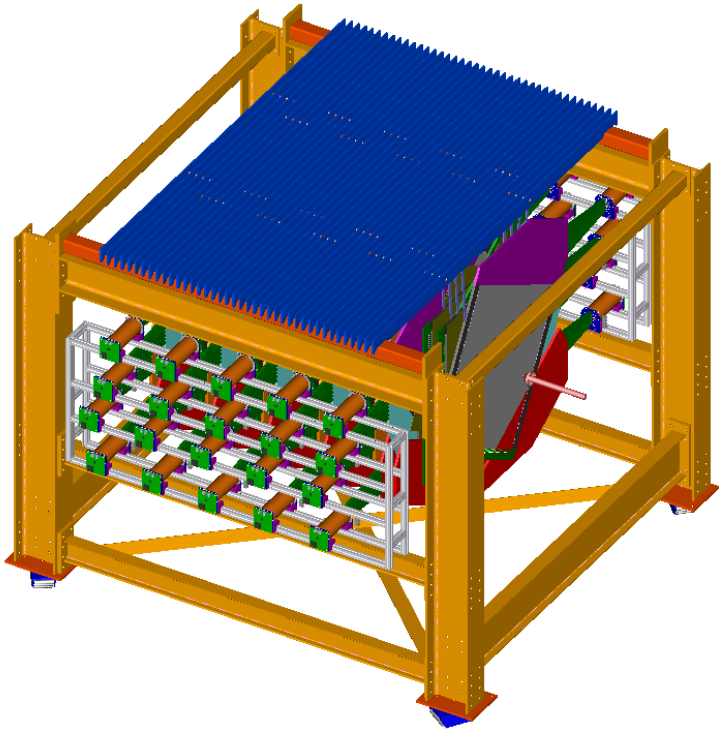


Test Beam Users

- **MINERvA**
  - **Need for measurement of calorimetric response of the detector to pions, protons, e^- from 200 MeV to few GeV**
  - **New tertiary beam being designed with momentum analyzing magnet**
    - 200–1000 MeV in new tertiary beam
    - 1–10 GeV in current secondary beam



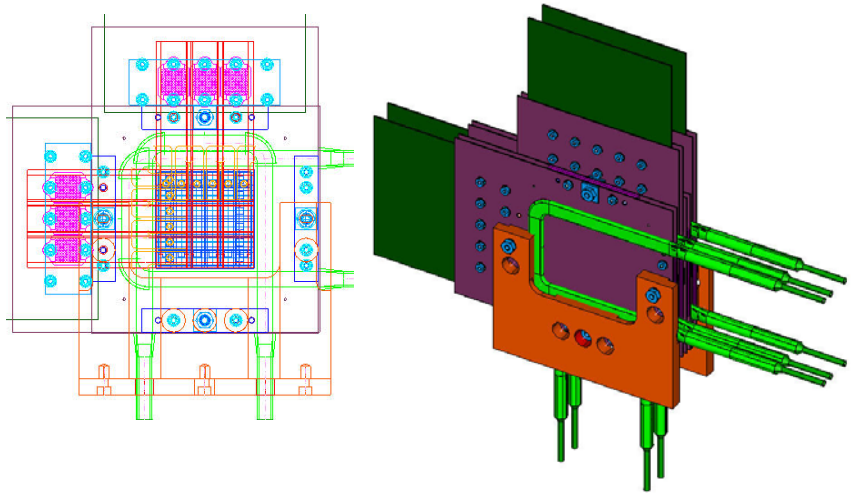
  - **Detector has removable Pb, Fe absorbers with scintillator to test all the different configurations found in the full MINERvA detector**



- **Fermilab is committed to support all beam tests**
  - **Access to technical staff**
  - **Access to computing resources**
  - **Engineering support for setup**

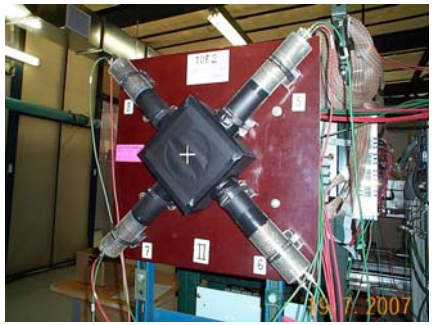
Beam Line Instrumentation and PID

- Building a four station pixel beam telescope (x,y,x,y) with a pointing resolution of ~3 μm
  - Synergy with the development and testing of thinned readout chips, FPiX in collaboration with RTI



- Installed new differential Cherenkov counter

- New TOF system planned: two large scintillator hodoscopes with SiPM readout
  - Separation of ~30 m, 4mm thick scintillator
  - Time-of-flight for beam less than 4 GeV with ~40 ps resolution



- Construction of four sets of scintillating fiber tracking detectors operating in vacuum

Conclusion

- Building on the unique characteristics of Fermilab
  - Excellent infrastructure, computing as well as detector development, and test facilities
  - Great access in multi-dimensional space

- Fermilab is developing a broad based, strategic plan for generic detector R&D by pursuing those technologies which – though challenging – hold most promise to significantly enhance the physics reach of new detectors
  - Established ourselves as world leader in the development of the 3D technology; many parties eager to collaborate with us.
  - The second branch we wish to develop is calorimetry

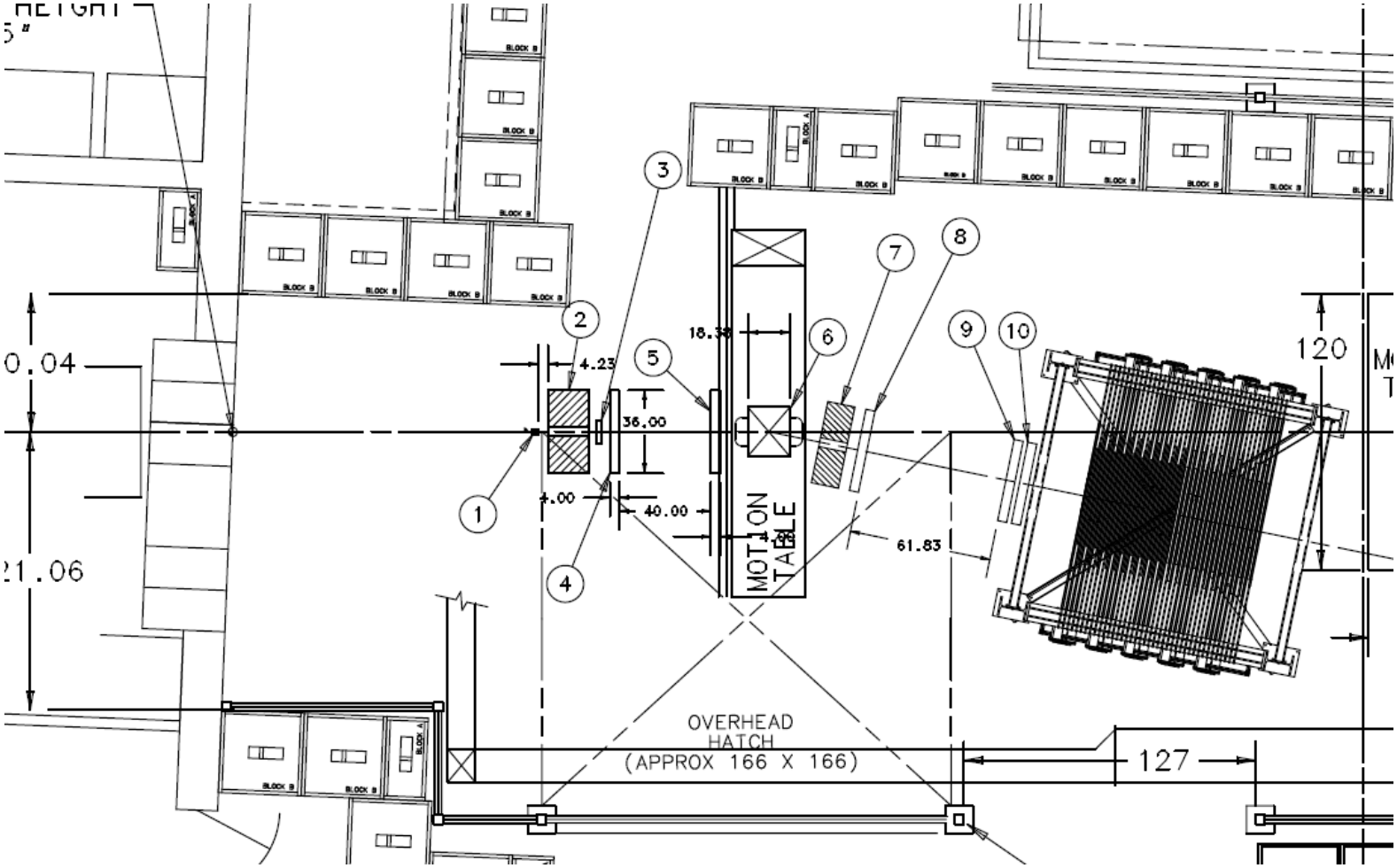
- Build scientific teams, including junior scientists, engaged in high-impact physics R&D efforts that are well supported with technical staff
  - Example is silicon 3D Vertical Integration effort

- Further establish Fermilab as a recognized center for physics and detector R&D, a scientific destination with a current, interim and long-term physics and R&D program

Backup Slides

MINERvA Tertiary Beam Design

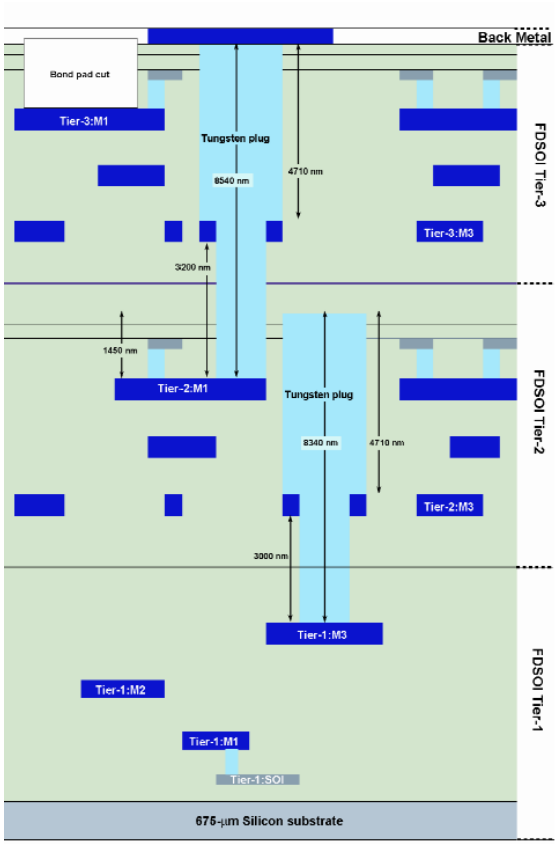
- Target takes 4-8 GeV pions from the incoming secondary beam
- Collimator – TOF station 1 – Tracking 1 and 2
- Bend magnet & collimator
- Collimator – TOF station 2 – Tracking 3 and 4

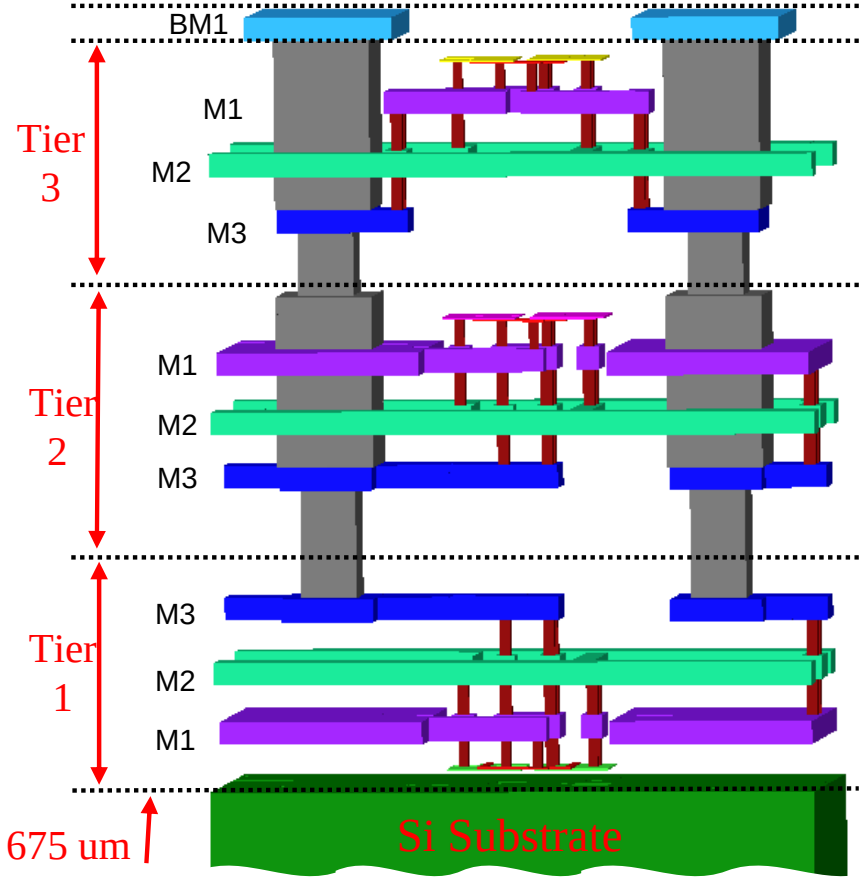


Modeling 3D Circuits

- **Applied for an SBIR Phase I grant with CFD Research Corporation (www.cfdrc.com) to develop automated design tools for detector and electronics integration which will allow the extraction of physical parameters of these devices based on the integrated circuit layout**
  - **Modeling and analysis of radiation effects**
  - **Modeling of thermal and mechanical properties**

MIT-LL 3D Layer Description

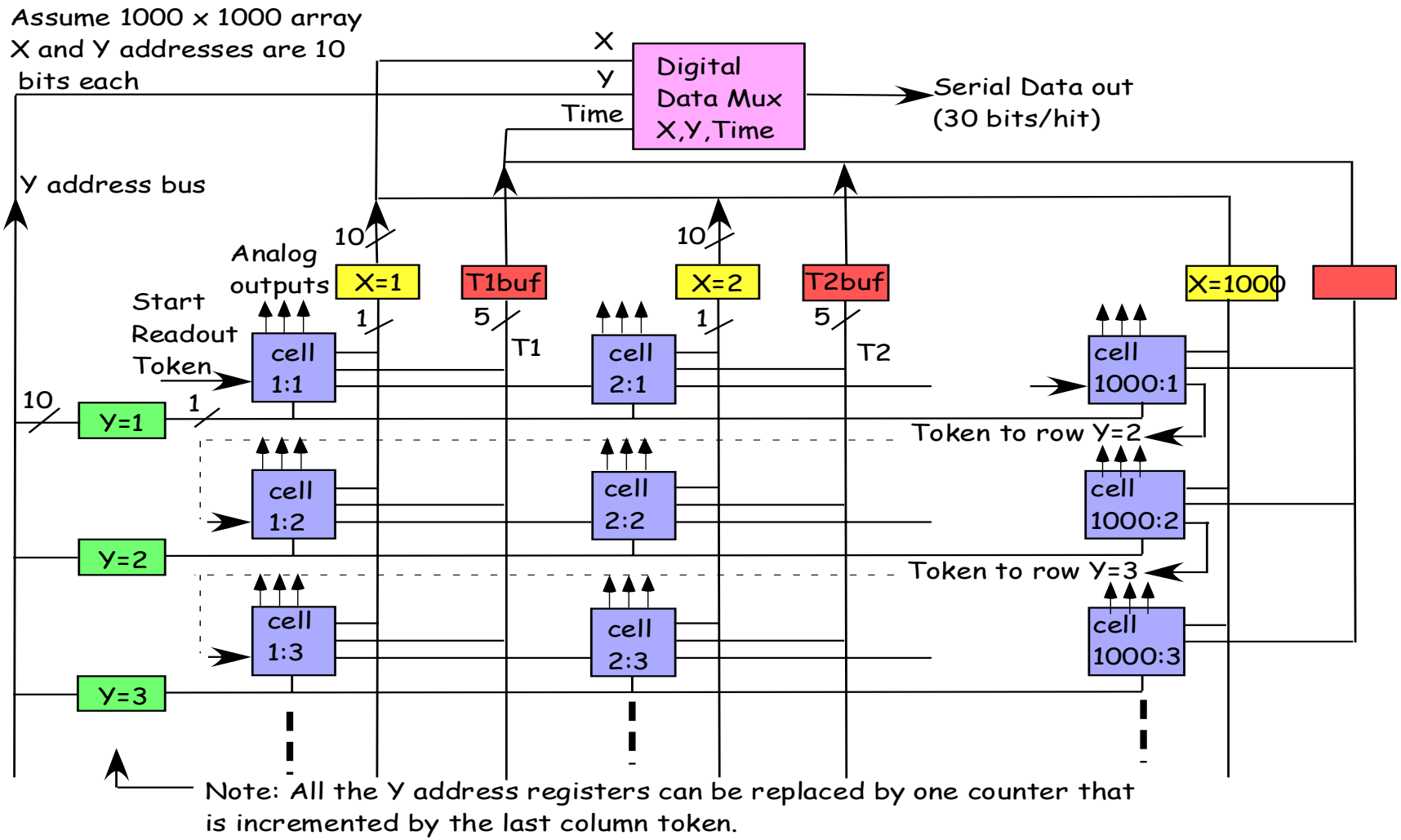




CFDRC Full 3D Model

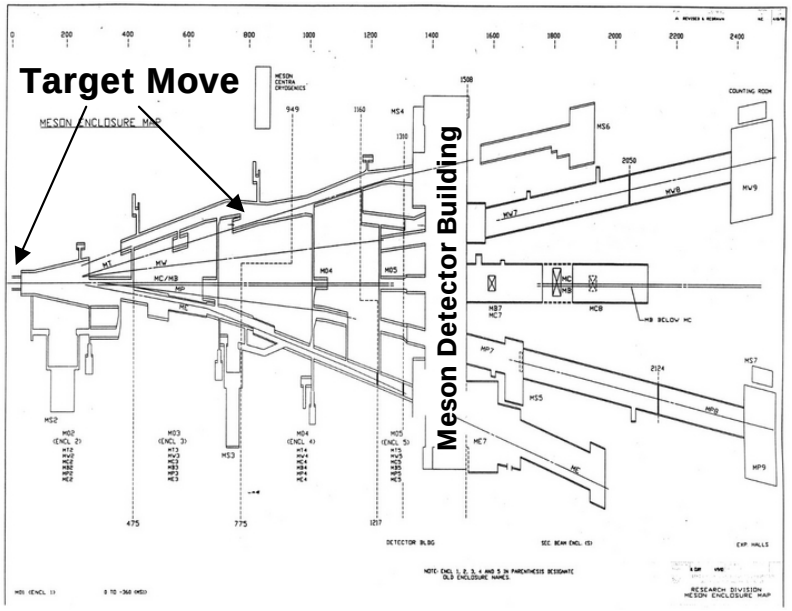
Pixel Readout Scheme

- Pixel being read points to the x address and y address stored on the perimeter.
- At same time, time stamp information and analog pulse height is read out
- During pixel readout, token scans ahead for the next hit pixel (200 ps/cell)



Possible Enhancement of Fermilab Beam Test

- **Further enhancements of the ILC R&D activities could be explored, with a concurrent scientific program, which could benefit the ILC community**
- **MCenter beam line, which houses the MIPP experiment, is currently not scheduled**
- **MCenter beamline**
  - **Beamline with excellent characteristics**
    - Six beam species ($p^{\pm}$,$K^{\pm}$,$p^{\pm}$) from 1 -- 85 GeV/c
  - **Excellent particle id capabilities**



- **Experimental setup**
  - **Could allow for better understanding of hadron-nucleus interactions, which could benefit our understanding of hadronic shower development, which is currently poorly understood**
    - Nuclei of interest that can be measured with an upgraded MIPP
      - H_2, D_2, Li, Be, B, C, N_2, O_2, Mg, Al, Si, P, S, Ar, K, Ca, Fe, Ni, Cu, Zn, Nb, Ag, Sn, W, Pt, Au, Hg, Pb, Bi, U, Na, Ti,V, Cr, Mn, Mo, I, Cd, Cs, Ba
  - **Moreover, experimental setup with the full spectrometer would allow for a tagged neutron beam from fully constrained reaction pp ➔ p,n,π^+**