ILC Detector R&D and Test Beams

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2007 FRA Visiting Committee

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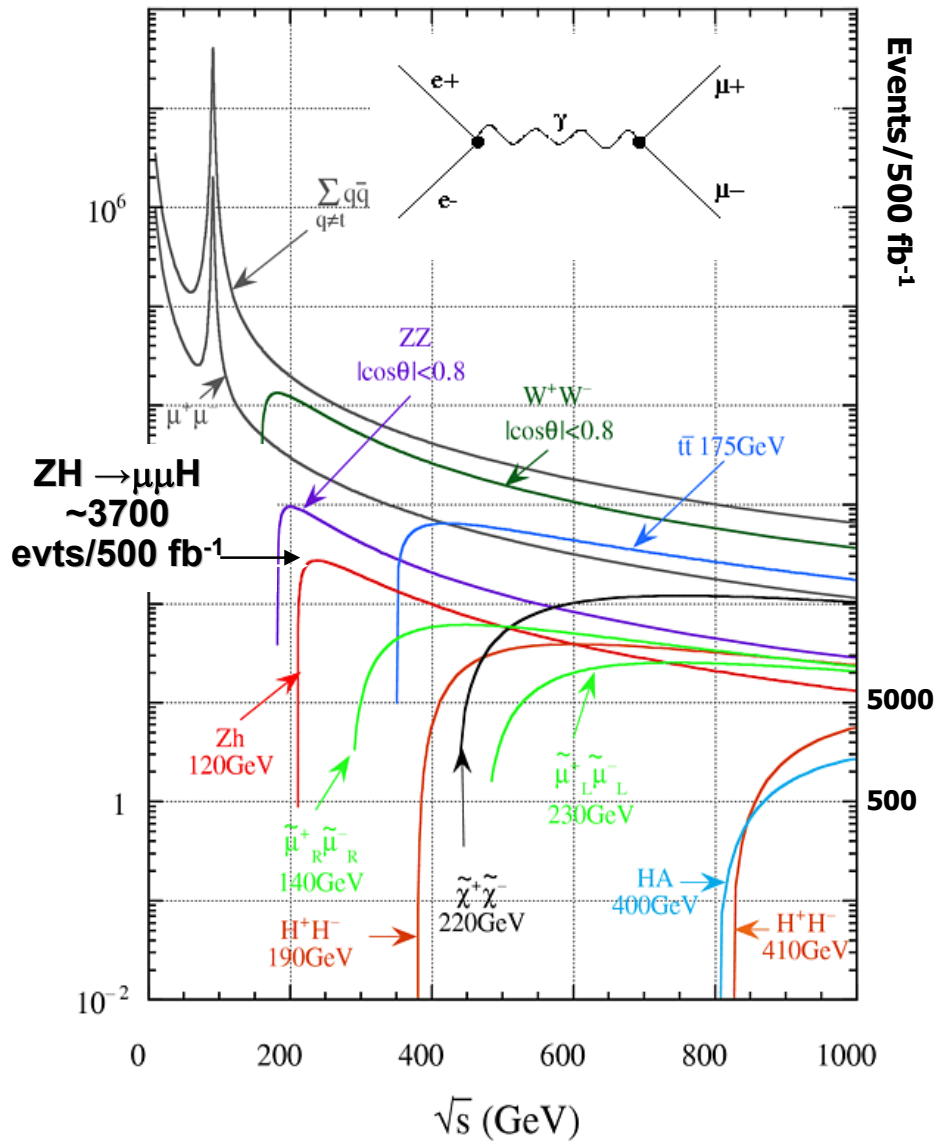
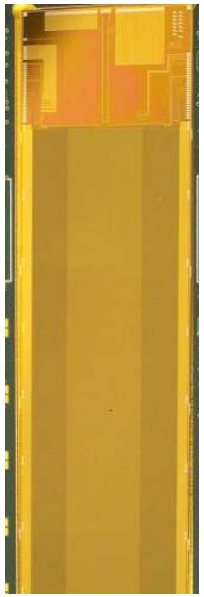
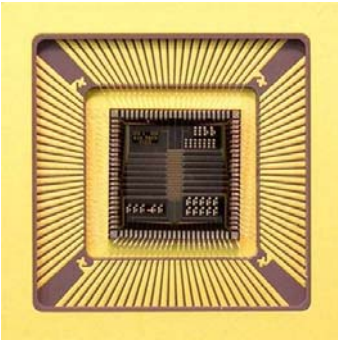
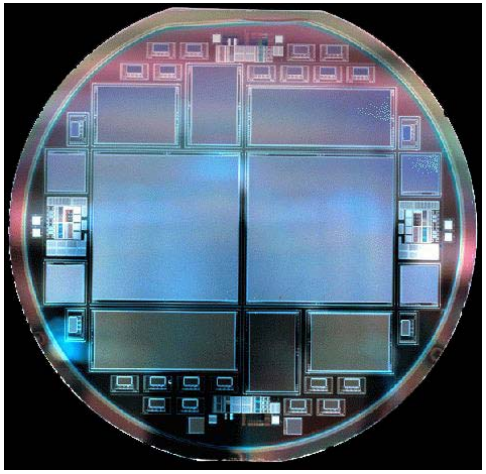
ILC Physics Characteristics

- **Machine design luminosity $\mathcal{L} = 2 \times 10^{34}\ cm^{-2}s^{-1}$ ($\sqrt{s}$ = 500 GeV)**
- **Processes through s-channel spin-1 exchange: $\sigma \sim 1/s$**
  - **Cross sections relatively democratic**
  - **Cross sections are small**
  - **Angular distribution: $(1 + \cos^2\theta)$**
    - Premium on forward region
    - Hermetic detectors
  - **Relatively large backgrounds**
    - 100k e^+e^- - pairs per bunch crossing
- **Near perfect particle identification**
  - **Discriminate W and Z in hadronic decay mode**
  - **Distinguish quarks from antiquarks**
- **Highly polarized e^- beam: ~ 80%**
  - **To employ discriminating power requires running at both polarities**
- **Every event counts !**

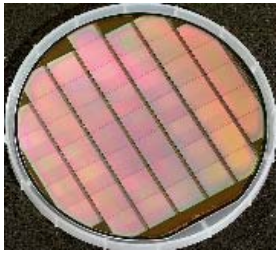
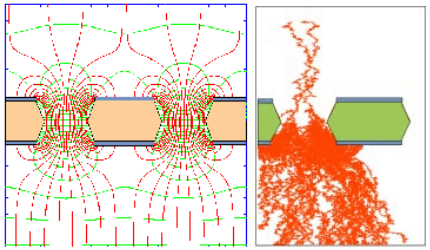
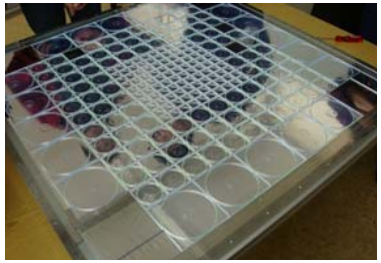


ILC Detector Characteristics

- **Pixel technologies**
  - CPCCD
  - CSCCD
  - FPCCD
  - DEPFET
  - CAPS
  - FAPS
  - MAPS
  - ISIS
  - SOI
  - 3D

- **Calorimeter Technologies**
  - Digital RPC Hcal
  - Digital GEM Hcal
  - Analog Scintillator Hcal
  - Dual Readout Hcal
  - Silicon-Tungsten Ecal
  - Scintillator-SiPM Ecal

- **ILC Detectors are first and foremost precision detectors**
- **Most technologies unproven**

Foci at Fermilab

- ***Development of pixel detector technologies***
  Based on extensive experience with silicon detectors and their associated readout, focus on the development of new pixel technologies in synergy with the development for LHC replacement and upgrade detectors.

- ***Development of low-mass silicon vertex detectors and trackers***
  Based on extensive experience with silicon trackers, focus on the design of low mass mechanical support structures for vertex detectors and trackers and pursue novel sensor technologies with special emphasis on the forward regions. Concurrently develop the tracking software enabling optimization of the detector design

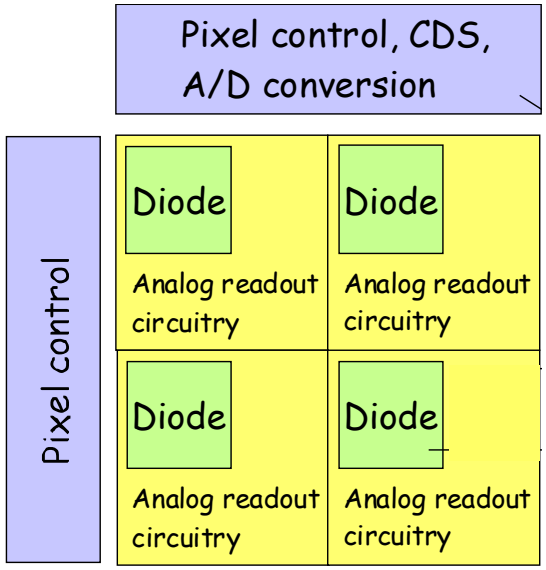
- ***Characterization of Geiger-mode Avalanche Photo Diodes and their application***
  Geiger-mode Avalanche Photo Diodes are a new technology to readout scintillation light. Due to their small size they can be highly integrated in the detector design and signal processing is much facilitated. They hold excellent prospects for many different applications. Being pursued is their application in scintillator-based muon detectors and scintillator and scintillator-leadglass dual readout calorimetry.

- ***Test Beam***
  Many detector technologies for the ILC are unproven. Redesigned the beam line at Mtest to accommodate the ILC needs, improve the beamline instrumentation and refurbished the facility.

- ***Physics Community Outreach***
  Organize and host many workshops with broad ILC perspective

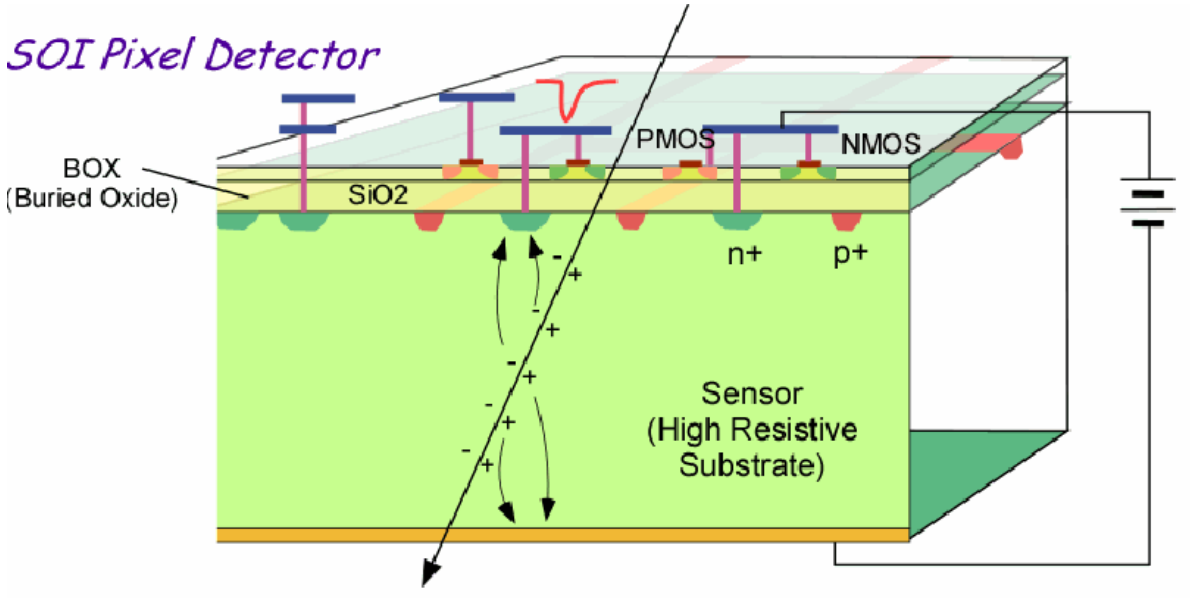
Pixel Detectors

- **Pixel detectors (for the ILC) are very difficult**
  - **Good angular coverage with many layers close to vertex**
  - **Excellent point resolution (< 4 μm)**
  - **Superb impact parameter resolution (5μm ⊕ 10μm/(p $\sin^{3/2}\theta$))**
  - **Transparency (~0.1% X_0 per layer)**
  - **Robust pattern recognition (track finding in vertex detector alone)**
  - **Integration over small number of bunch crossings (<150 = ~50 μs)**
  - **EMI immunity; Power Constraint (< ~100 Watts)**
- **Significant progress has been made to address these issues by integrating sensors and front end electronics within the pixel cell: Monolithic Active Pixel Sensors (MAPS)**
  - **Fundamental limitations**
    - Small signal dependent on epi thickness
    - Most designs are limited to NMOS transistors
    - Not 100% fill factor
    - Slow rise time set by diffusion
- **Fermilab is pursuing alternatives:**
  - **SOI (Silicon On Insulator) Pixel Sensors**
    - Offers improvements over MAPS
  - **3D integrated circuits**
    - Also SOI process, but offers improved performance over SOI pixel sensors.



Conventional MAPS 4 Pixel Layout

SOI Detector Concept



Advantages

- 100% fill factor
- Large and fast signal
- Small active volume: high soft error immunity
- Full di-electric isolation: latchup free
- Low Junction Capacitance: high speed, low power

- **Bonded Wafer: low resistive top layer + high resistive substrate, separated through a Buried OXide (BOX) layer**
  - Top layer: standard CMOS Electronics (NMOS, PMOS, etc. can be used)
  - Bottom substrate layer forms detector volume
  - The diode implants are formed beneath the BOX and connected by vias
- **Monolithic detector, no bump bonds (lower cost, thin device)**
- **High density and smaller pixel size is possible**
- **Small capacitance of the sense node (high gain V=Q/C)**
- **Industrial standard technology (cost benefit and scalability)**

SOI Detector Development

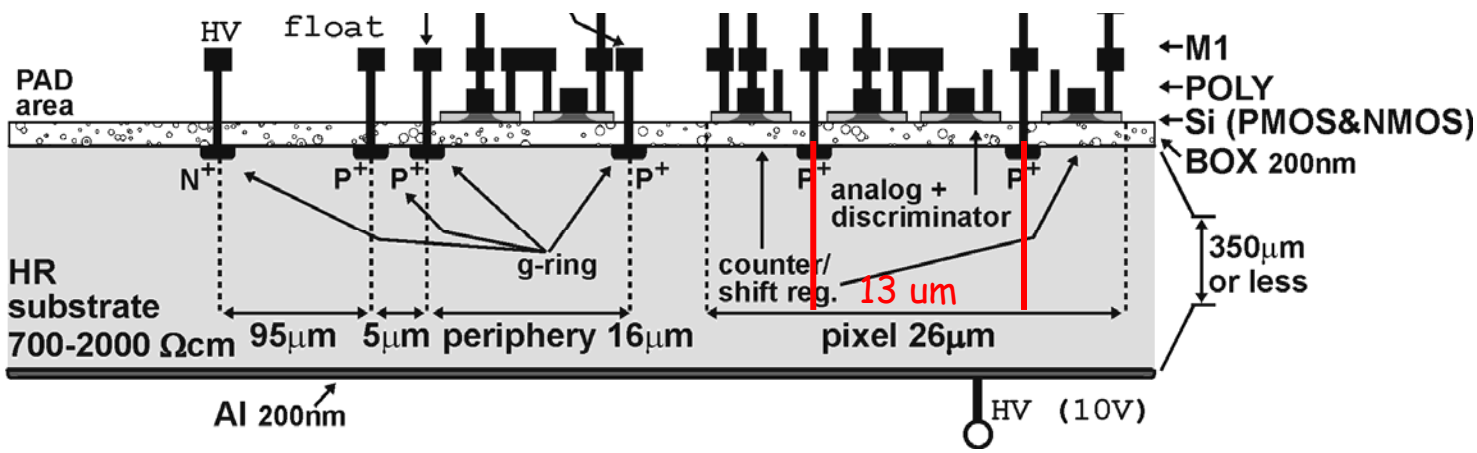
- **SOI detector development is being pursued by Fermilab at two different foundries**
  - **OKI Electric Industry Co. Ltd. in Japan through Multi-Project Wafer submission (KEK)**
  - **American Semiconductor Inc. (ASI) in US, through SBIR phase I grant (Cypress semiconductor)**

OKI		ASI	
Process	0.15μm Fully-Depleted SOI CMOS process 1 Poly, 5 Metal layers	Process	0.18μm Partially-Depleted dual gate SOI CMOS process, Dual gate transistor (Flexfet) No poly, 5 Metal layers
SOI wafer	Wafer Diameter: 150 mmϕ Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz、>1k Ω-cm (*No type assignment*), 650 μm thick	SOI wafer	Wafer Diameter: 200 mmϕ Handle wafer: FZ>1k Ω-cm (*n type*)
Backside	Thinned to 350 μm no contact processing plated with Al (200 nm).	Backside	Thinned to 50-100 μm polished, laser annealed and plated with Al.

- **Goal is to understand the advantages and problems of SOI detector design, in particular issues related to trapped charges in the BOX layer due to radiation and its potential remedies through voltage on the substrate and the reduction of "back gate effect"**

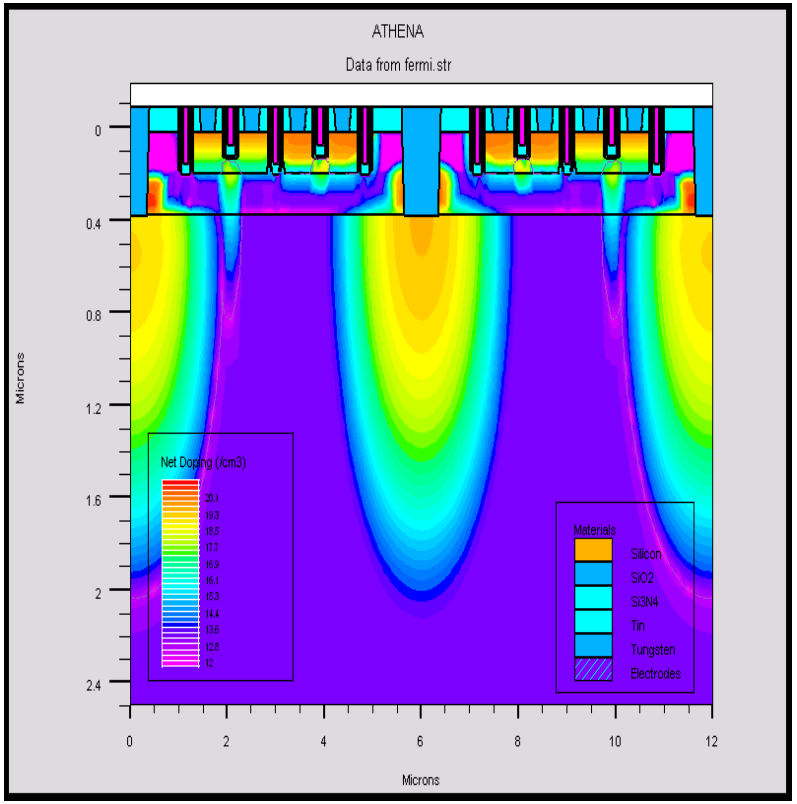
Pixel Design in OKI Process

- **MAMBO Chip: Monolithic Active pixel Matrix with Binary cOunters**
  - **A wide dynamic range counting pixel detector plus readout circuitry, sensitive to 100-400 keV electrons, high energy X-rays, and minimum ionizing particles, designed in the OKI 0.15 micron process**
- **OKI process incorporates diode formation by implantation through the BOX**
- **Chip architecture (simplified due to design time constraint): amplifier – shaper – discriminator – binary counter**
  - **Maximum counting rate ~ 1 MHz/pixel**
  - **Reconfigurable counter/shift register**
    - 12 bit dynamic range
  - **Limited peripheral circuitry**
  - **Drivers and bias generator**
  - **Submitted Dec. 15, '07; delivered this month.**
  - **Array size 64x64 pixels, 26μmx26μm**
  - **13 μm implant pitch, to minimize the "back gate" effect**
    - 4 diodes per pixel
  - **350 micron detector thickness**



Pixel Design in ASI Process

- **SBIR Phase I grant with American Semiconductor (ASI), Boise, Idaho**
- **ASI process (0.18μm) based on an SOI dual gate transistor called a Flexfet™**
  - **Flexfet has a top and bottom gate**
  - **Bottom gate shields the transistor channel from**
    - Charge build up in the BOX caused by radiation.
    - Voltage on the substrate and thus removes the back gate voltage problem
  - **Modeling and process simulation of a thinned, fully depleted sensor/readout device.**
  - **Studies of backside thinning, implantation, and laser annealing in collaboration with Cornell**
  - **Circuit design for ILC pixel cell**
    - Voltage ramp for time marker
    - ~20 micron analog pixel
    - Sample 1 - crossing time
    - Sample 2 - time over threshold for analogue pulse height information
    - Coarse time stamp



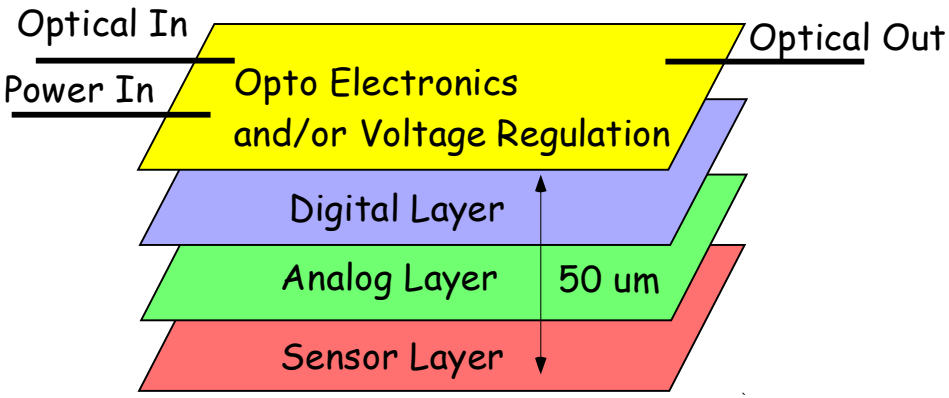
Diode simulation in Flexfet process

http://www.americansemi.com/

Vertical Scale Integrated Circuits (3D)

- **SOI detector technology offers several advantages over MAPS; 3D offers advantages over SOI detectors**

- **A 3D device is a chip comprised of 2 or more layers of semiconductor devices which have been thinned, bonded, and interconnected to form a monolithic circuit**
  - **Layers can have devices made in different technologies**
    - Process optimization for each layer
  - **Increased circuit density due to multiple tiers of electronics**
  - **Ability to mate various technologies in a monolithic assembly**

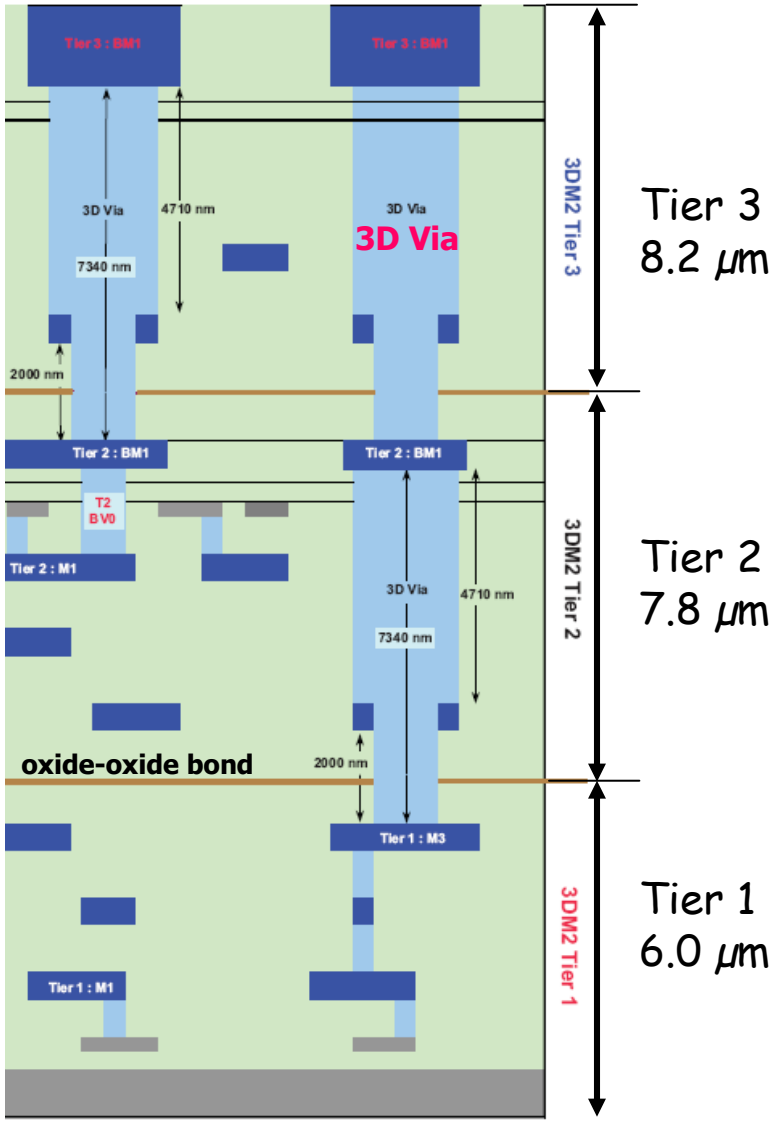


- **Technology driven by industry**
  - **Reduce R, L, C for higher speed**
  - **Reduce chip I/O pads**
  - **Provide increased functionality**
  - **Reduce interconnect power, crosstalk**

- **Critical issue are:**
  - **Layer thinning to < 10 μm**
  - **Precision alignment (< 1 μm)**
  - **Bonding of the layers**
  - **Through-wafer via formation**

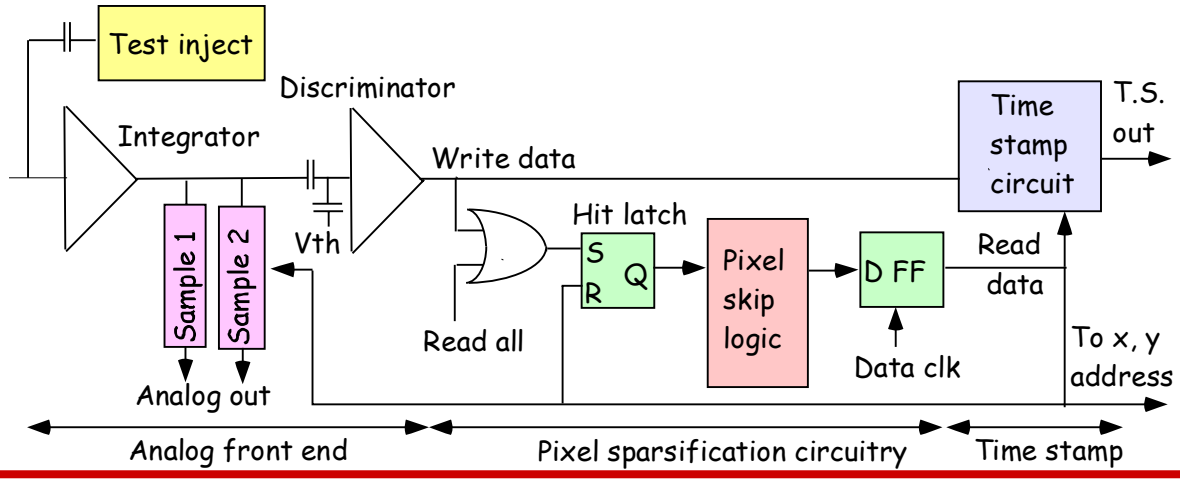
Development of a 3D Demo Chip

- **MIT Lincoln Laboratories (MIT-LL) has developed the technology that enables 3D integration**
  - **Demonstrated the 3D technology through fabrication of imaging devices**
  - **Has infrastructure to allow for 3D Multi-Project Run fabrication**
- **We were invited to participate in the MIT-LL three-tier multi-project run**
  - **3D design to be laid out in MIT-LL 0.18 μm SOI process**
    - SOI provides additional advantages: BOX, full isolation, direct via formation, enhanced low-power operation
  - **3 levels of metal in each layer**
- **Submission deadline was Oct. 15, 2006**
- **Requested wafer space of ~ 2.5 x 2.5 mm^2**
- **Pixel size 20 x 20 μm; 64 x 64 pixel array**
- **No integrated sensor**
- **Chip to be received sometime in fall**



Architecture of Demonstrator Chip

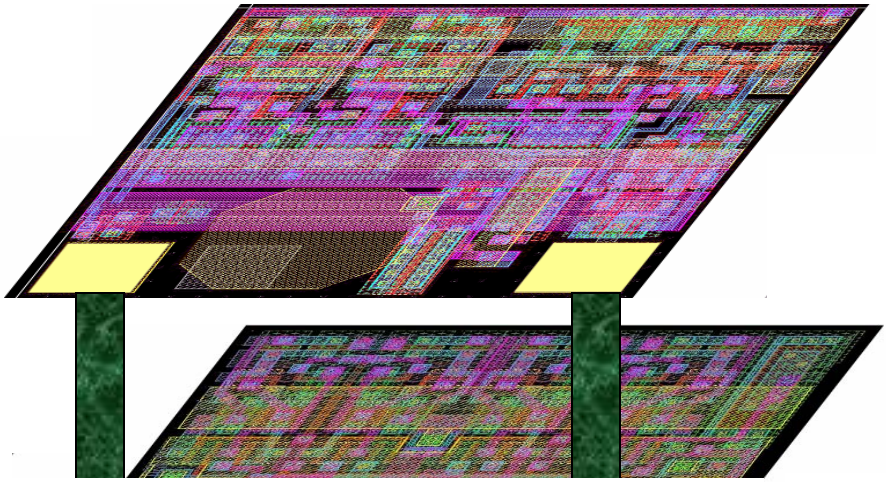
- **Design:**
  - **Provide analog and binary readout information**
  - **Time stamping of pixel hit for ILC environment**
    - Divide bunch train into 32 time slices; each hit pixel can store one time stamp equivalent to 5 bits of time information
  - **Sparsification to reduce data rate**
    - Use token passing scheme with look-ahead to reduce data output
      - During acquisition, a hit sets a latch
      - Sparse readout performed row by row with x- and y-address stored at end of row and column
  - **Chip divided into 3 tiers**
    - Pixels as small as possible but with significant functionality.
    - Design for 1000 x 1000 array but layout only for 64 x 64 array.



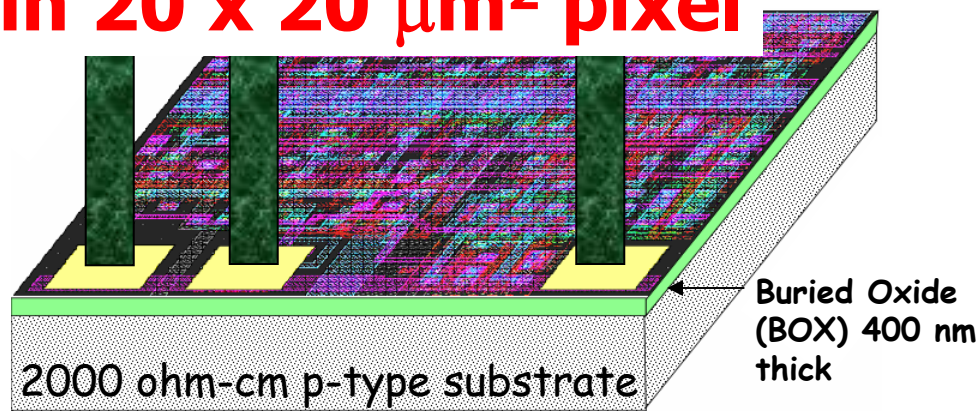
Schematic pixel cell block diagram

3D Stack

- Form 2 vias, 1.5 x 7.3 µm, through tier 3 to tier 2
- Tier 3
  - Integrator, DCS plus readout
  - Discriminator
  - 2 vias
  - 38 transistors
- Bond Tier 3 to Tier 2
- Form 3 vias, 1.5 x 7.3 µm, through Tier 2 to Tier 1
- Tier 2
  - 5 bit digital time stamp
  - Analog time stamp (ts)
    - Either analog or digital ts
  - 3 vias
  - 72 transistors
- Bond Tier 2 to Tier 1
- Tier 1
  - OR for READ ALL cells
  - Pixel skip logic for token passing
  - 3 vias
  - 65 transistors



175 Transistors in 20 x 20 μm^2 pixel



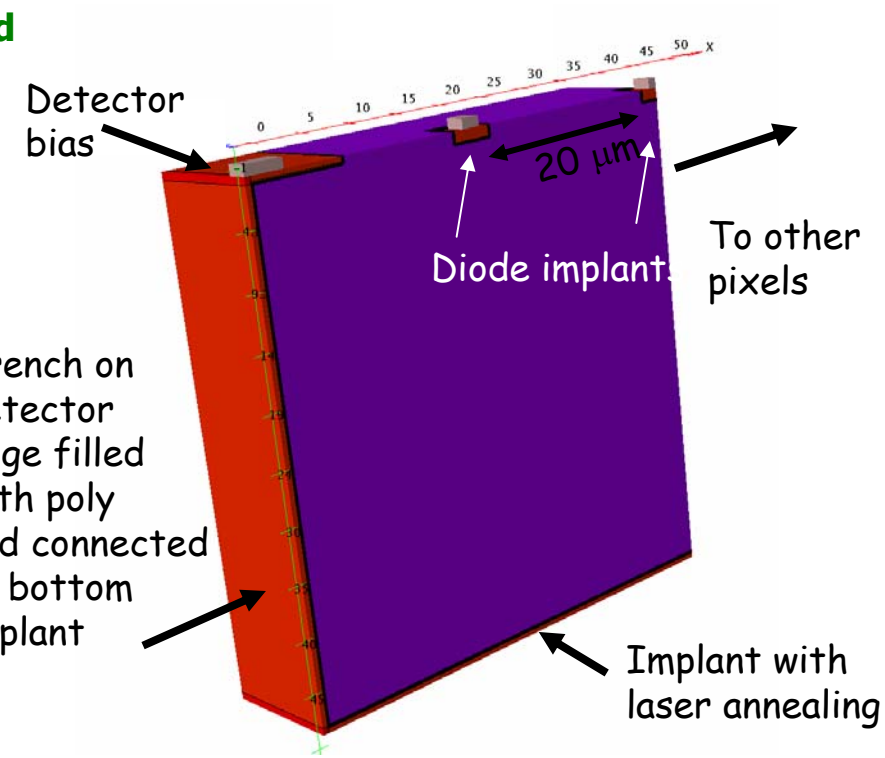
Development of Thinned Edgeless Sensors

- **3D chip provides only readout. In parallel we are designing mating sensors on 6", high resistivity, float-zone, n-type wafers to be bonded to 3D chips**

- **Sensor fabrication also at MIT-LL**
  - **Thinned to 50, 75, 100 microns, implanted and laser annealed**
  - **Sensors sensitive to the edge, 4-side abuttable, i.e. no dead space**
  - **Deep trench etch, n doped poly-silicon fill provides edge doping**

- **Sensors to be submitted to beam and probe tests**
  - **Validate the technology which provides thinned detectors sensitive to the edge**
  - **Measure the actual dead region in a test beam**
  - **Bond with 3D readout chip (and FPIX chip)**

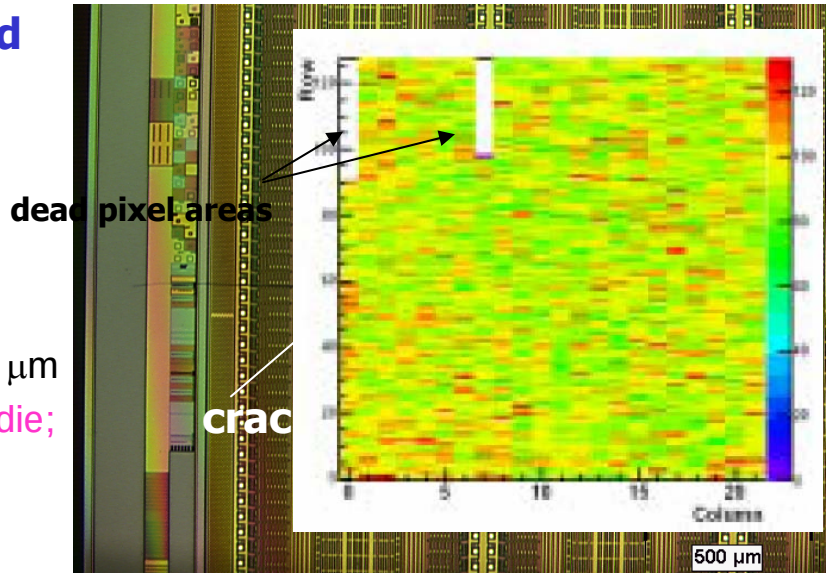
- **First design which, in principle meets 'all' of the ILC requirements for thickness, resolution, power dissipation, time stamping**

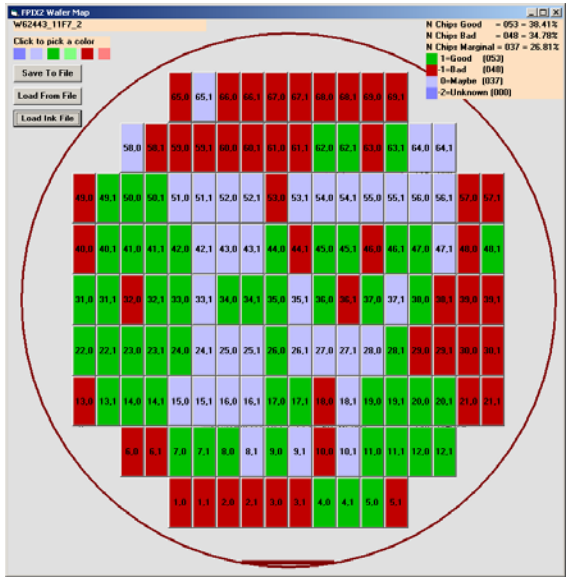


Detector Cross section near one detector edge

Device Thinning

- **Gaining experience on device thinning and thinned devices**
  - **Thinning of individual FPIX die at RTI**
    - Two step procedure:
      - Backgrind and polish to 150 μm
        - » 7 chips failed out of 72
      - Plasma thinning down to 50/25/15/10 μm
        - » 4 responding out of 20 testable die; all have areas of dead pixels
    - Repeat after evaluation
      - 6 chips out of 8 working (2 dead)
  - **Thinning of full wafer at IZM**
    - Yield ~50%

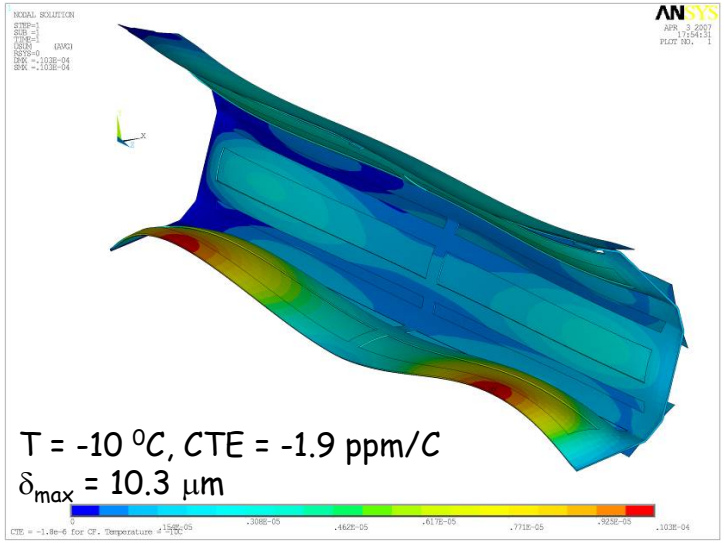




- **No indication of subtle electrical effects associated with thinning the wafer. The IZM wafer looks (visual inspection) very good except.**
- **Small (~10%) apparent noise and threshold dispersion increase observed for parts thinned by both RTI & IZM that tested "good" not understood**

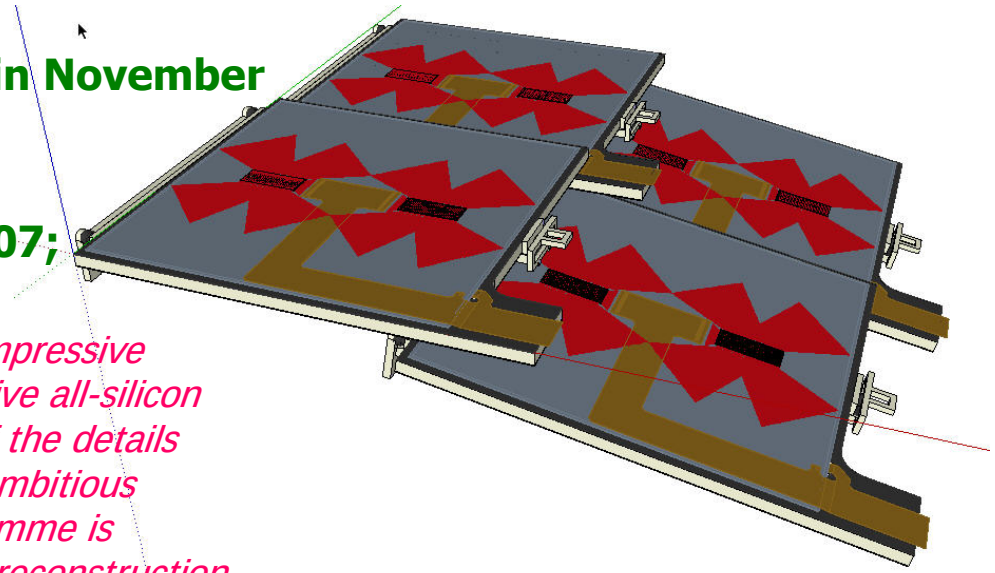
Vertex Detector Mechanical Design

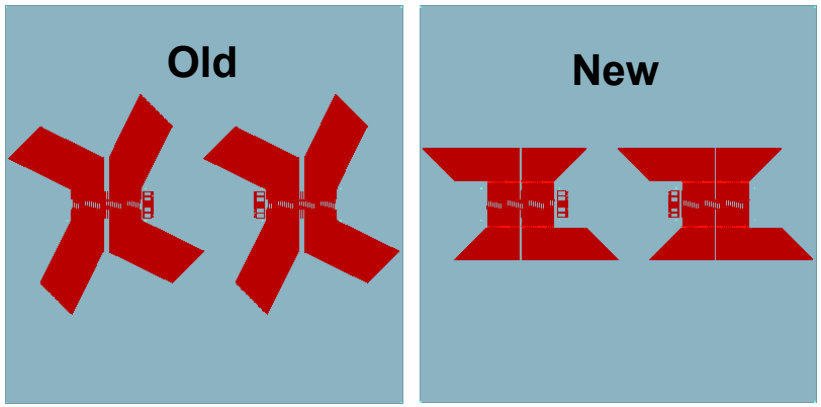
- **Multi-layered, high precision, very thin, low mass detectors**
  - **Goal: layer thickness of 0.1% X_0 per layer, equivalent of 100 μm of Si**
- **Collaborating with the University of Washington on carbon-fiber mechanical support structures**
- **Developing techniques for fabricating and handling thin-walled carbon fiber structures**
- **Prototypes of carbon-fiber support structures**
  - **Three prototype half-shell structures fabricated for evaluation and testing**
- **Develop assembly tooling/mandrels**
  - **Assembly mandrel, end ring glue fixture and vacuum chuck for precision placement of silicon wafers on support structure**
- **FEA analysis of mechanical and thermal behavior**
  - **Deflection under gravity OK**
    - maximum deflection vector is about 0.6 μm
  - **Thermal deflections unacceptably large**
    - assuming -10 ^{0}C operation, CTE mismatch
    - CTE = -1.9 ppm/C. δ_{max} = 10.3 μm
      - CTE_{Si} is 2.49 ppm/K



Outer Tracker Design

- **In collaboration with SLAC, progressing on:**
  - **Optimization of outer tracker design for SiD concept**
  - **Sensor and module design for outer tracker**
- **Conducted two major reviews**
  - **Internal sensor design review in November**
    - Bolla, Sadrozinski, Seidel, Tajima
  - **ILC WWS tracking review at ILC/GDE/ACFA meeting, Feb. '07; Review report:**
    - *"The SiD collaboration has made impressive progress in defining a comprehensive all-silicon tracking system, including many of the details which are needed to establish an ambitious material budget. Their R&D programme is supported by simulations of track reconstruction which can be expected to refine the design"*
- **Design modification**
  - **Fermilab Ansys capacitance calculation**
- **Goal is to finalize sensor drawings and submit to Hamamatsu**

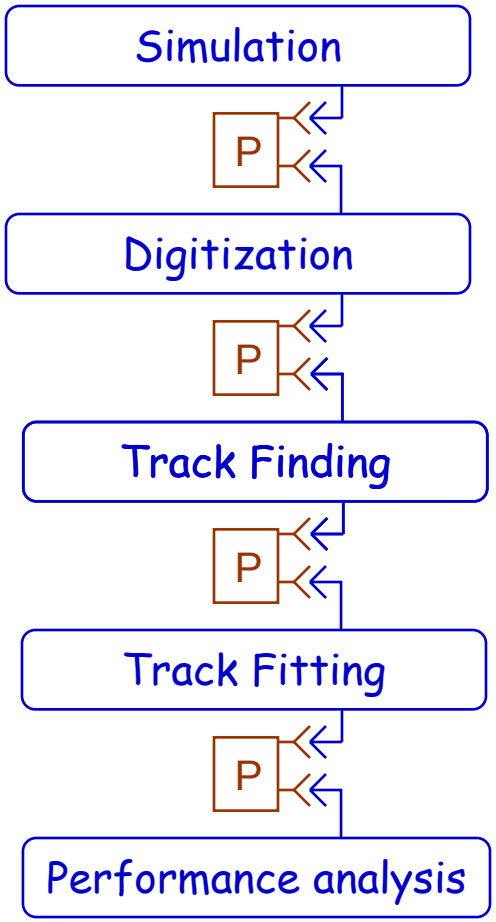




Tracking Software

- Recently added group from Computing Division to tracking software effort
- Effort will concentrate on various fronts:
  - Tracking infrastructure improvements
  - Track finding in forward region
    - Leaves much to be desired in many experiments
  - Vertexing involving in b-jec/c-jet separation
  - Physics benchmarking processes
  - Optimization of detector design

- Now have complete coverage of all aspects of vertex and tracking detectors
  - Sensors
  - Readout
  - Mechanical design
  - Vertex and track finding
  - Physics processes
  - Detector optimization
- Effort ongoing to include outside collaborators



Silicon Summary

- **Accomplished, we hope, a fully integrated and coherent detector approach based on existing strengths**
  - **Pursuing most promising pixel sensor technologies**
    - Only group world-wide pursuing 3D detectors
  - **Integration of readout**
  - **Simultaneous development of mechanical support structures**
  - **Software efforts on track and vertex finding**
    - Close communication between hardware and software developers
  - **Active participation in physics benchmark processes leading to**
  - **Detector optimization**

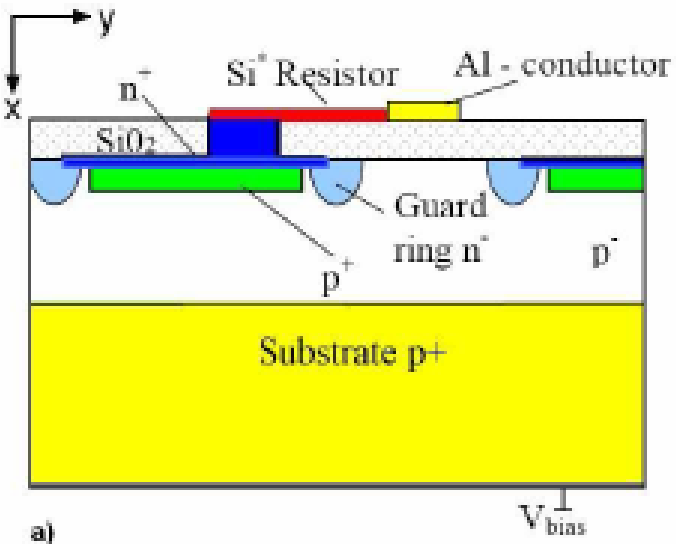
- **Plans are for strengthening this effort to**
  - **Include outside collaborators**
  - **Take advantage of synergies with other projects**

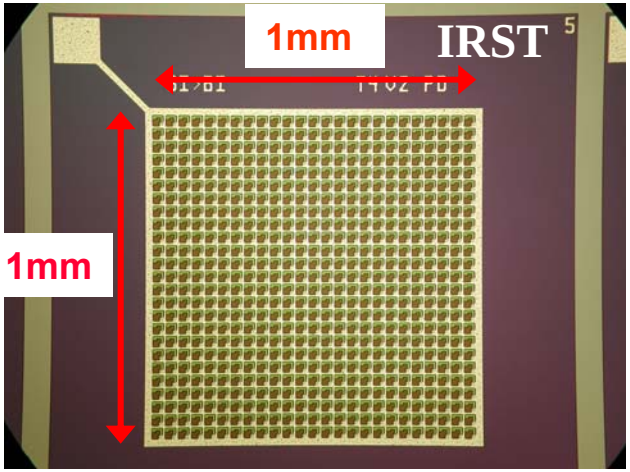
Geiger-Mode Avalanche Photo Diodes

- **Avalanche photodiode operating in Geiger mode, also called Multi-Pixel Photon Counter (MPPC) or Silicon photo-multiplier (SiPM)**
  - **Array of pixels connected to a single output**
  - **Signal = Sum of all cells fired**
  - **If probability to hit a single cell < 1 => Signal proportional to # photons**

- **New detector development; devices not readily commercially available yet**
  - **Hamamatsu (100, 50 and 25 μm pixels)**
  - **IRST-Trento (several designs)**
  - **CPTA**
  - **Mephi**
  - **Dubna (two designs)**
  - **MPI (back-illuminated)**
  - **SensL?**

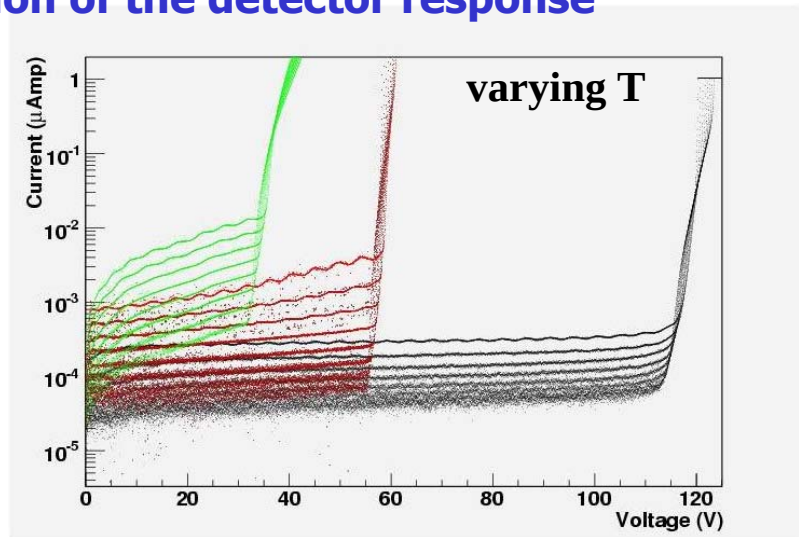
- **Multiple applications**
  - **Dual readout, lead-glass – scintillator sampling calorimetry**
  - **Analog scintillator tile hadron calorimeter**
  - **Muon detector based on scintillator strips**





SiPM Characterization and Plans

- Developing tools for complete characterization of the detector response
- Four step program envisioned
  - Database of Static Characteristics
  - Measurements "in the dark"
  - Characterization of response to a calibrated light pulse
  - Microscopic studies of the photo-detector
- Try to relate some of the characteristics to the detector design and construction and provide feedback to vendor



- Develop algorithm for readout strategy and calibration procedure for multiple applications and synergies
  - Scintillator based hadron calorimetry
  - Dual readout calorimetry
  - Muon detection
  - CMS interest as potential replacement of HPD's
  - MPPC's are baseline for T2K for which Fermilab provides the readout
  - (Medical imaging)

Upgrade of Test Beam Facilities

- **The old Fermilab Meson Test Beam Facility (MTBF)**
  - **Could not deliver a pion beam lower than 4 GeV**
  - **Electrons had a low flux because of significant material in the beam**

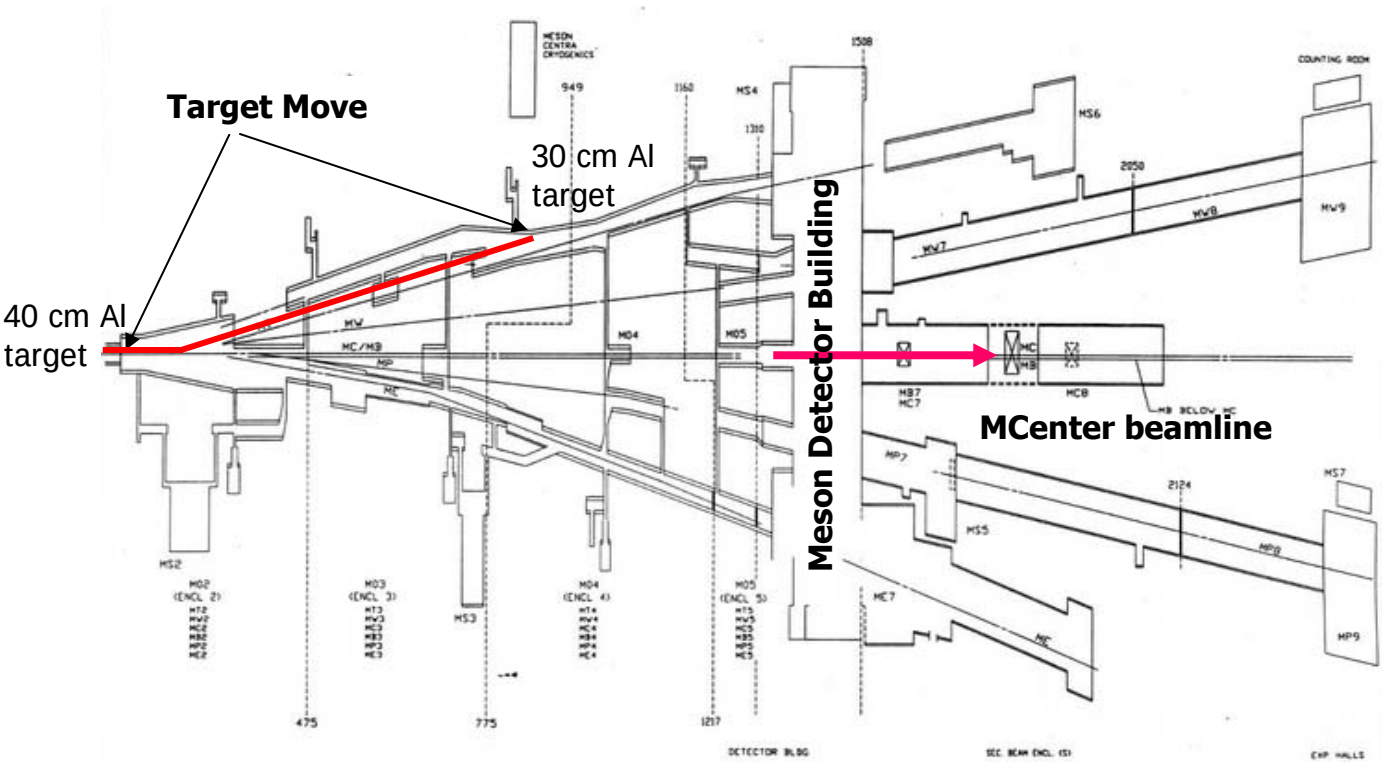
- **We recognized that test beams will be the lynchpin for new detector R&D for the ILC and we should support the community by providing the infrastructure for beam tests**

- **A new beamline was designed and completed early January '07, retaining former capabilities**

- **Also motivated by the ILC community, revised the spill structure and restated the program impact**
  - **SY120 beam can impact the program at the 5% level following a flexible algorithm**
  - **Spill structures:**
    - One 4 second spill every minute, for 12 hours a day
    - Two 1 second spills every minute, for 12 hours a day
    - One 4 second spill every two minutes, 24 hours a day (this is implemented if MIPP is running in MCenter)

Beam Specifications

- **Beam specifications for upgraded facility:**
  - **Particle momentum as low as 1 GeV**
  - **Momentum bite 2% < 5 GeV, 1% >5 GeV**
  - **Beam Spot 1" > 10 GeV, trigger counter determines below 10 GeV**
  - **Parallel section for Cherenkov <0.3 mrad**
  - **Horizontal dispersion 1% dp/p per inch**



Proton Mode: 120 GeV protons transmitted through upstrm target

Pion Mode: 8-66 GeV beam tuned for secondaries from upstrm target

Low Energy Pion Mode: 1-32 GeV beam tuned for secondaries from new dnstrm target

First Performance Numbers

- **Moving the target to MT3 (L=1273-1388' goes to L= 451-566') reduces the decay length for pions and reduction of the material in the beamline**

Tune (GeV)	Old Rate for 1E12 PPS from MI	New Rate for 1E12 PPS from MI	e- fraction	Energy Resolution
1	---	~4K		
2	---	~4K		
3	~150			
4	~500	~15k		2.4%
8	~5K	~20k	30%	5%
16	~20K	~35k	20%	1.2%
33	~30K			1.0%
66	~100K			
120	~800K			

Blue = proton mode

Green = pion mode

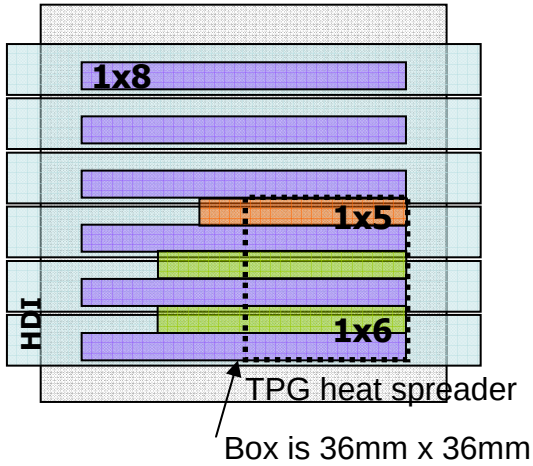
Red = low E mode

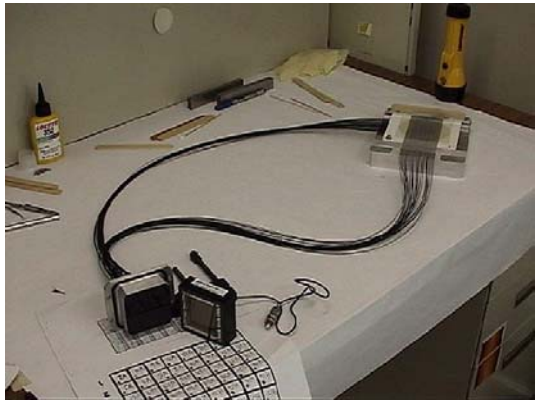
	Beam Composition	
	16 GeV	8 GeV
Positrons	20%	30%
Muons	2-5%	10-15%
Pions	45-50%	15-20%
Protons	30%	30-40%

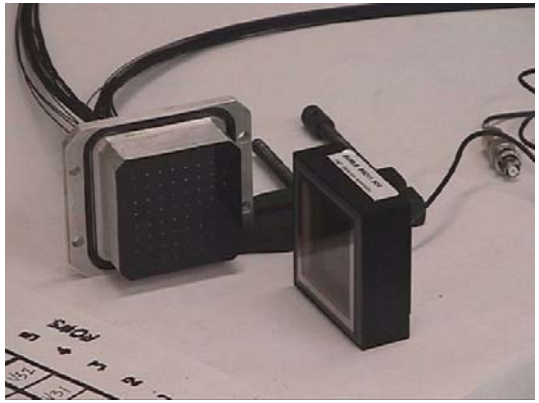
- **Performance of beam line almost "out of the box"; further retuning**
- **Additional improvements planned:**
  - **Upstream target will be made movable out of the beamline for the Low Energy mode. This will increase fluxes significantly.**
  - **Muon tuning has not been tried yet**
- **Many users lined up for use of facility**

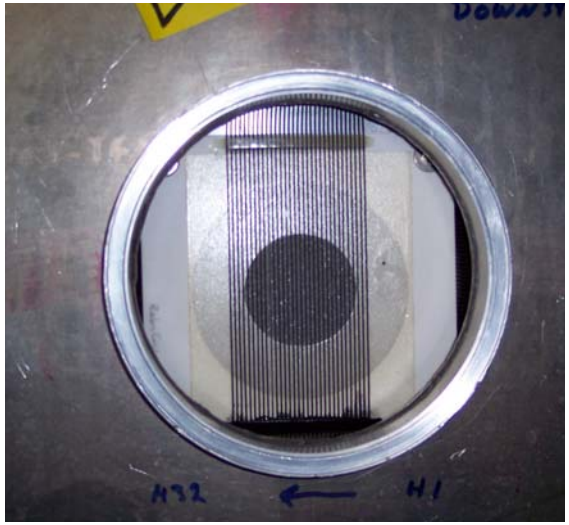
Beam Line Instrumentation and PID

- **Building a pixel beam telescope with a pointing resolution of ~3 μm**
  - **Synergy with the development and testing of thinned readout chips, FPiX in collaboration with RTI**
- **One threshold Cherenkov detectors will be converted into differential counter**
- **New TOF system: two large scintillator hodoscopes with 4 PMT's on each one**
  - **Separation of about 30 meters, 4mm thick scintillator**
  - **Time-of-flight for beam less than 4 GeV with ~250 ps resolution**
- **Construction of four sets of scintillating fiber tracking detectors operating in vacuum**



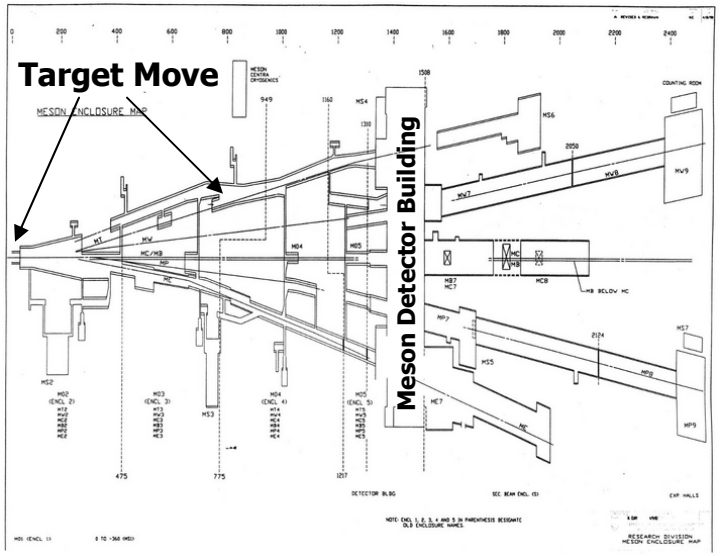






Possible Enhancement of Fermilab Beam Test

- **Further enhancements of the ILC R&D activities could be explored, with a concurrent scientific program, which could benefit the ILC community**
- **MCenter beam line, which houses the MIPP experiment, is currently not scheduled**
- **MCenter beamline**
  - **Beamline with excellent characteristics**
    - Six beam species ($p^{\pm}$,$K^{\pm}$,$p^{\pm}$) from 1 -- 85 GeV/c
  - **Excellent particle id capabilities**



- **Experimental setup**
  - **Could allow for better understanding of hadron-nucleus interactions, which could benefit our understanding of hadronic shower development, which is currently poorly understood**
    - Nuclei of interest that can be measured with an upgraded MIPP
      - H_2, D_2, Li, Be, B, C, N_2, O_2, Mg, Al, Si, P, S, Ar, K, Ca, Fe, Ni, Cu, Zn, Nb, Ag, Sn, W, Pt, Au, Hg, Pb, Bi, U, Na, Ti,V, Cr, Mn, Mo, I, Cd, Cs, Ba
  - **Moreover, experimental setup with the full spectrometer would allow for a tagged neutron beam from fully constrained reaction pp → p,n,π^+**

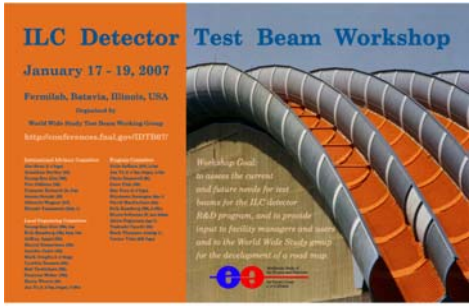
Collaborative Efforts

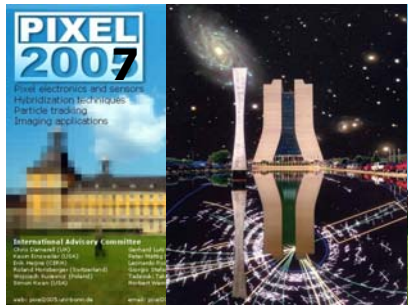
- Our goal is to establish as many collaborative efforts as possible
- Pixel sensor technology
  - Continuous Active Pixel Sensors (CAPS): Hawaii – Fermilab collaboration
  - Monolithic Active Pixel Sensors (MAPS): UC Berkeley – LBL – Fermilab – Strasbourg
  - 3D Technology: Fermilab – Purdue – Cornell – Bergamo collaboration
- Vertex detector Mechanical Design
  - Fermilab - SLAC – Strasbourg - UC Berkeley – U of Washington collaboration
- ASIC development
  - DCAL chip for digital hadron calorimetry (RPC and GEM): Argonne – Fermilab – UTA collaboration
- Hadron Calorimetry
  - SiPM characterization: Fermilab – INFN Pisa -- NIU – Udine – ITC-irst collaboration
  - Muon Tail Catcher mechanical and electronics design: Fermilab – NIU collaboration
- Muon Spectrometer
  - Fermilab – Indiana - NIU – Notre Dame - UC Davis - Wayne State collaboration
- Solenoid Design
  - Fermilab – Iowa – SLAC - Tokyo – KEK – Toshiba collaboration
- Tracking Software Development
  - Brown – Fermilab – SLAC – Lecce collaboration

- Communication
  - Merged SLAC lcd meeting with Fermilab ILC detector and physics meeting into a weekly joined ALCPG Physics and Detector meeting
  - Weekly ILC lunch discussions

Physics Community Outreach

- **To address issues of critical importance to the ILC and the community at large and to strengthen its role to bid to host**
  - **Hadronic Shower Simulation Workshop**
    - Understand shortcomings of modeling of hadronic showers
    - Agreement to make it a periodic meeting
    - Sept. 6-8, 2006
  - **Test Beam Workshop**
    - Evaluation of test beam needs at Fermilab
    - Jan. 17-19, 2007
  - **SiD Workshop**
    - Preparations for CDR for SiD detector concept
    - April 9-11, 2007
  - **The LHC early phase for the ILC**
    - ILC-LHC interplay
    - April 12-14, 2007
  - **Loopfest VI**
    - Radiative corrections for the ILC and LHC
    - April 16-18
  - **Joint ALCPG/GDE Meeting**
    - Regional ILC meeting
    - October 22-26, 2007
  - **Pixel 2007**
    - Most significant conference on pixel detector work
    - Use synergies with LHC and Imaging applications
    - Fall 2007





Summary and Plans

- Developed and implemented a cogent plan for pixel technologies; looking towards further enhancing that program with the goal of becoming a leader in the design of pixel technologies.
- Developing a similar plan for calorimetry with initial emphasis on photo-detector characterization with the goal to participate in the development of the calorimetry for the ILC and the associated algorithms
- Increase our role in physics benchmarking processes and detector design optimization
- Further enhance the test beam facility with associated support for particle identification, data acquisition and data analysis
  - Test beam environment should be as user-friendly as possible

- For our "global" role as potential host
  - Create an intellectually inviting, supportive environment for ILC collaborators and a vibrant user community
  - Co-lead and direct world-wide efforts; facilitate test beam coordination

- ILC is still the highest priority at Fermilab. Detector and Physics R&D cannot fall behind the GDE schedule for the machine

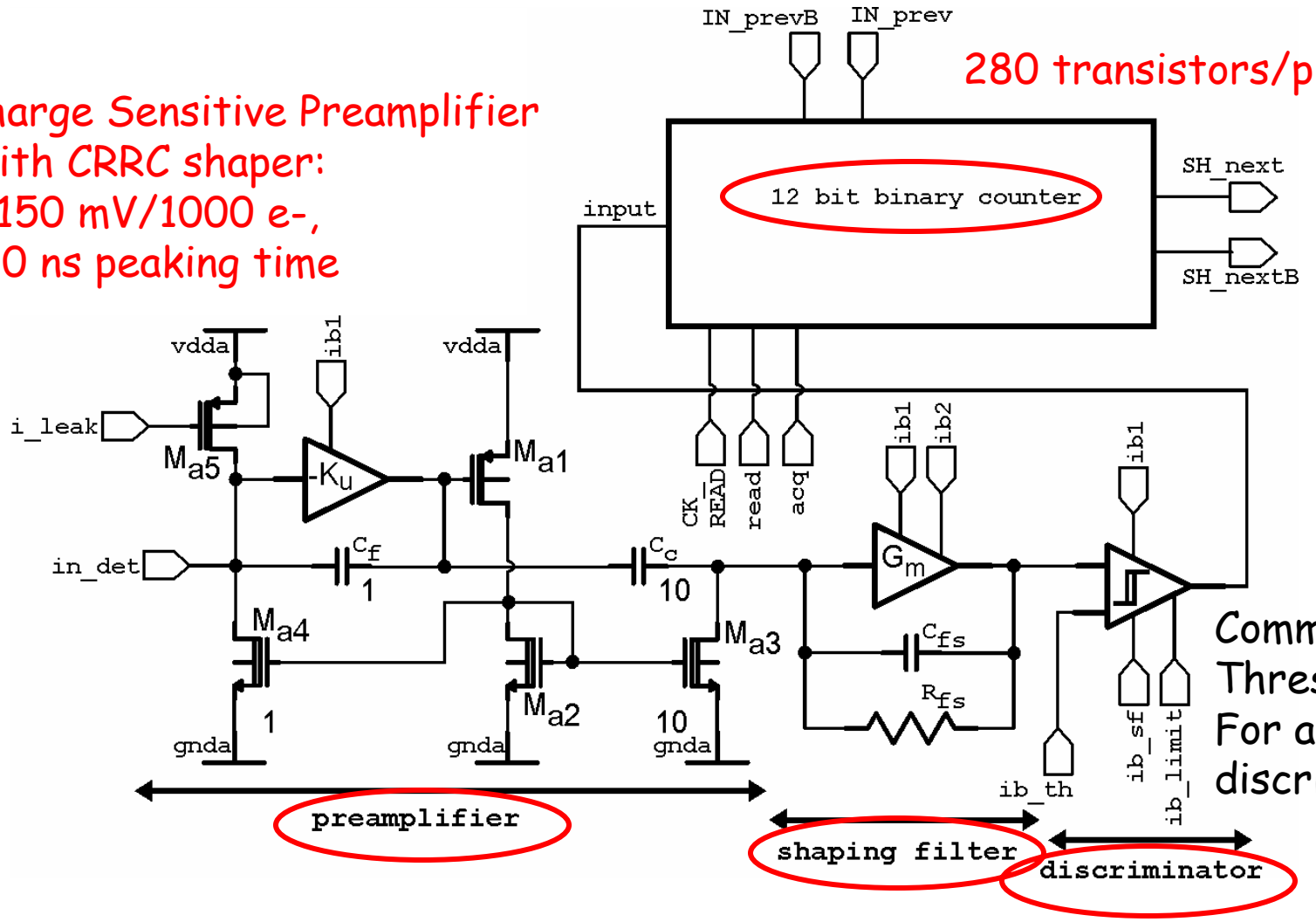
Backup Slides

Pixel Design in OKI Process

- **Schematic of pixel design in OKI process**

Charge Sensitive Preamplifier
with CRRC shaper:
~ 150 mV/1000 e-,
150 ns peaking time

280 transistors/pixel cell

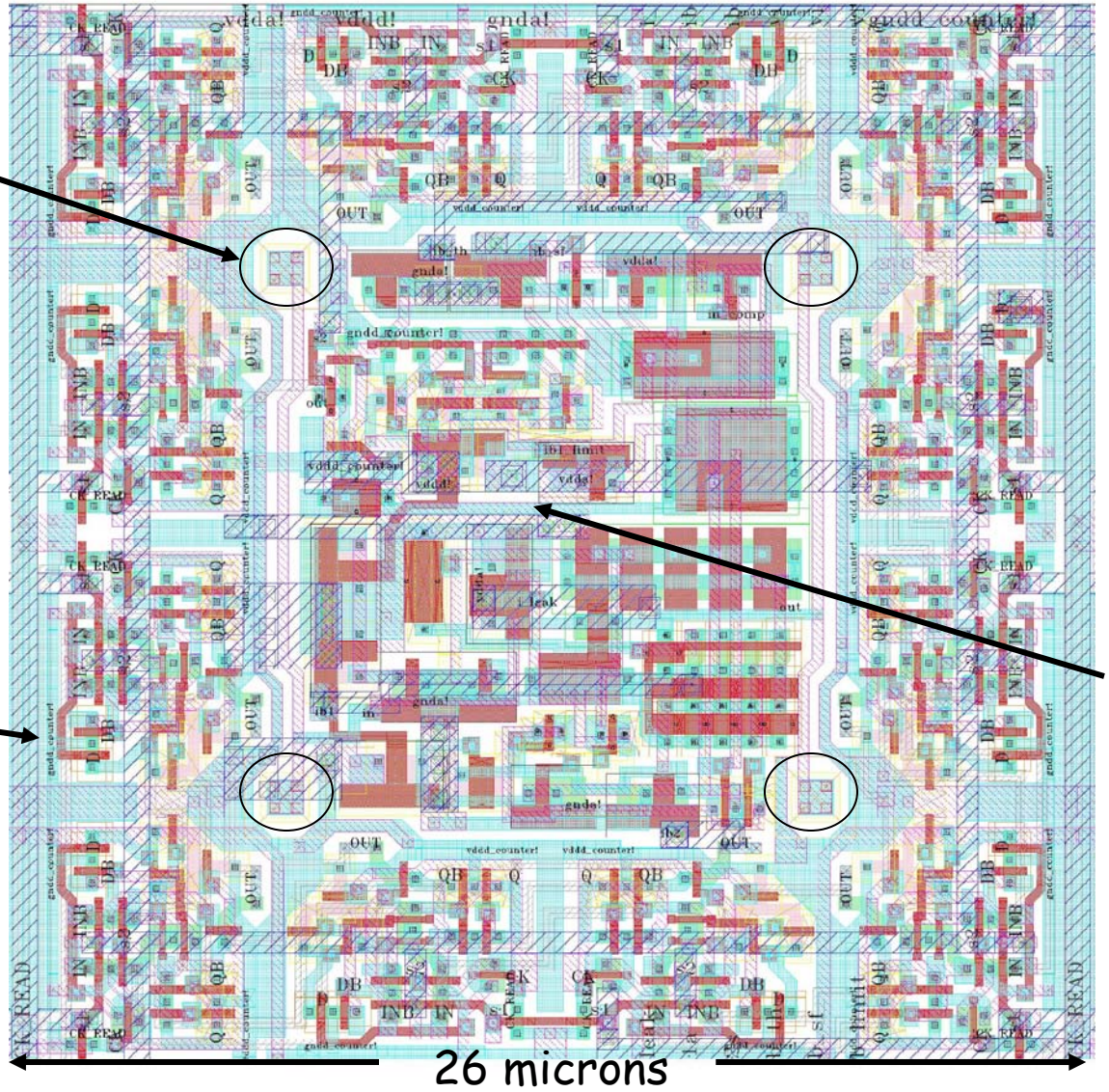


Common
Threshold
For all
discriminators

OKI Pixel Cell Layout

One of four detector diodes

One of twelve D flip-flops arranged around perimeter of pixel cell

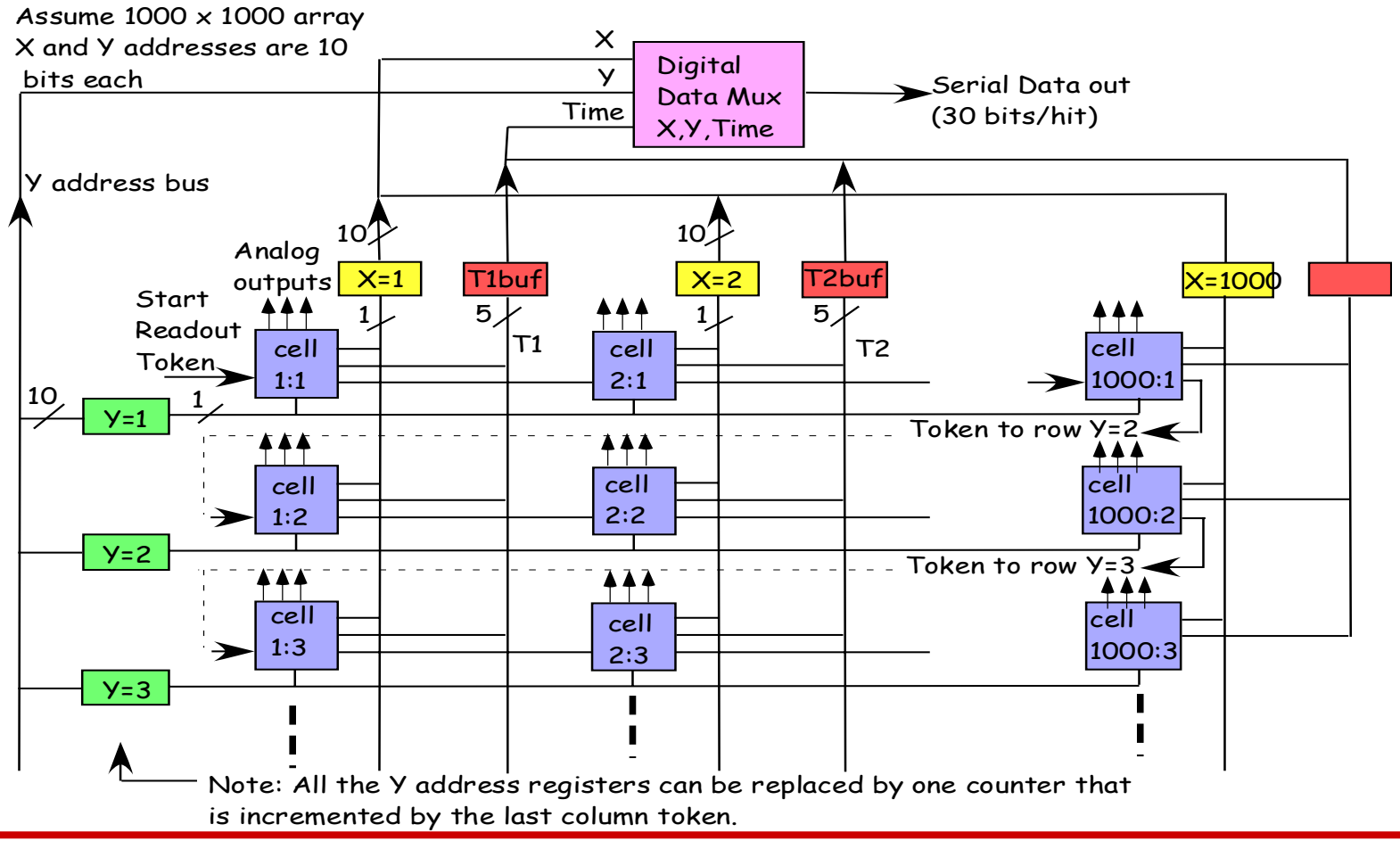


All analog circuits are located in center of pixel cell between diodes and surrounded by guard ring

26 microns

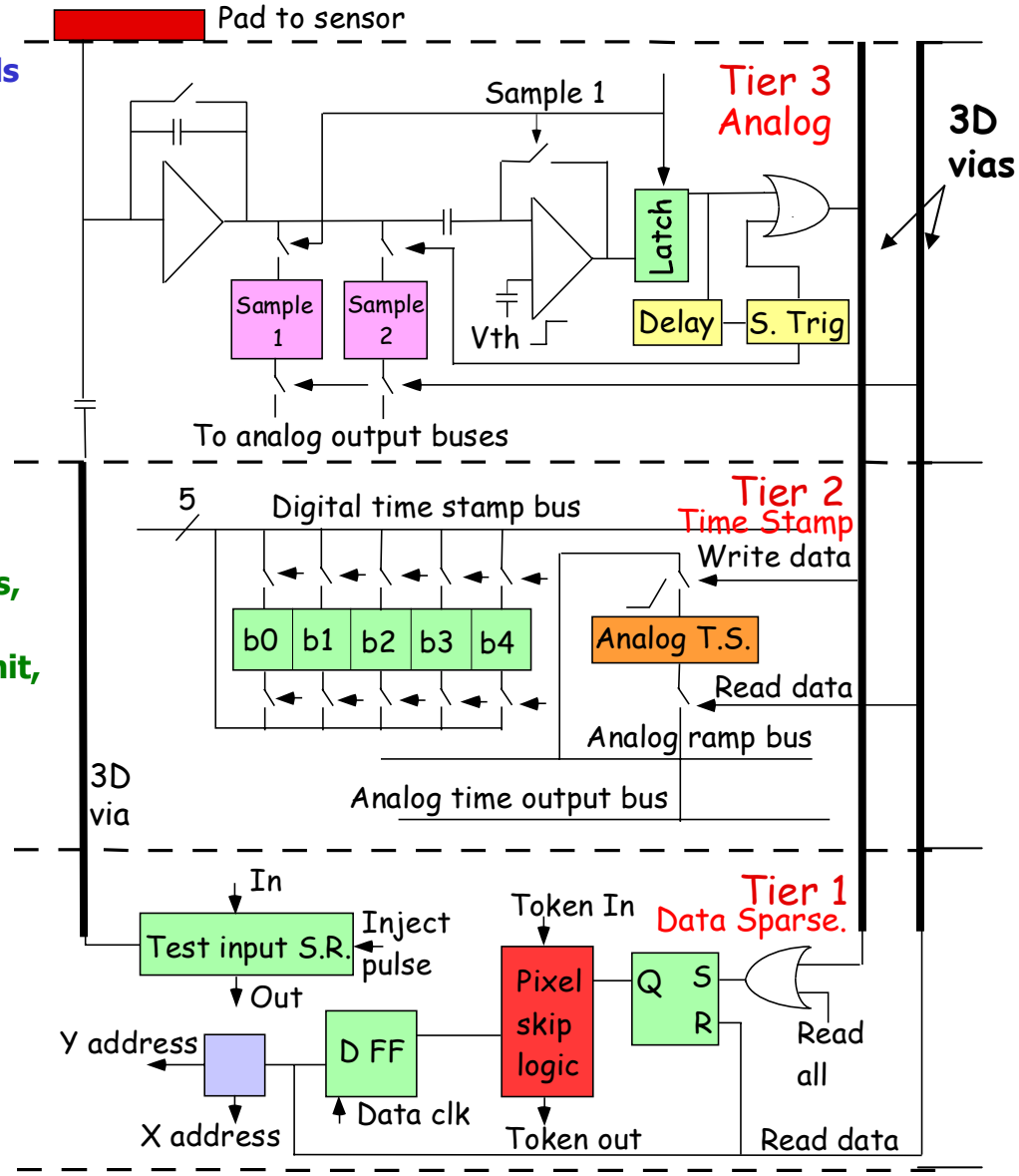
Pixel Readout Scheme

- **Pixel being read points to the x address and y address stored on the perimeter.**
- **At same time, time stamp information and analog pulse height is read out**
- **During pixel readout, token scans ahead for the next hit pixel (200 ps/cell)**



3D Three Tier Pixel Layout

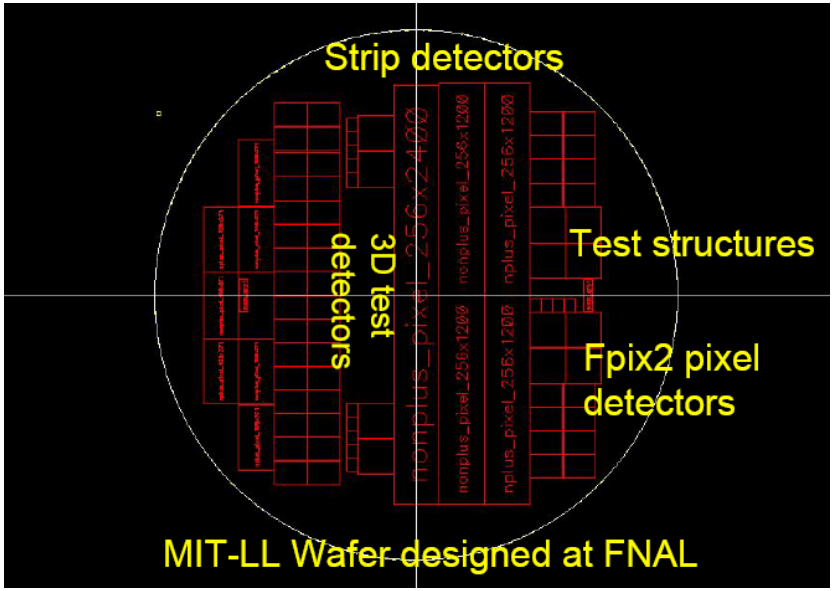
- **Readout speed for an ILC environment**
- **Assume 1k x 1k array with 20 x 20 μm² pixels**
  - **First pixel in each row always read out**
    - Adds 1000 cells, small increase in data volume
  - **Time to scan 1 row: 200 ps x 1000 = 200 ns**
  - **Time to readout cell 30 bits x 20 ns/bit = 600 ns**
  - **Plenty of time to find next hit pixel during readout**
- **Assume maximum number of hits/chip of 250 hits/mm²**
  - **For a 1000 x 1000 array of 20 μm pixels, 100k hits/chip**
  - **For 50 MHz readout clock and 30 bits/hit, readout time: 100,000 hits x 30 bits/hit x 20 ns/bit = 60 msec.**
- **Readout time is far less than the ILC allowed 200 msec. Thus the readout clock can be even slower or several chips can be put on the same bus. Readout time is even less for smaller chips**

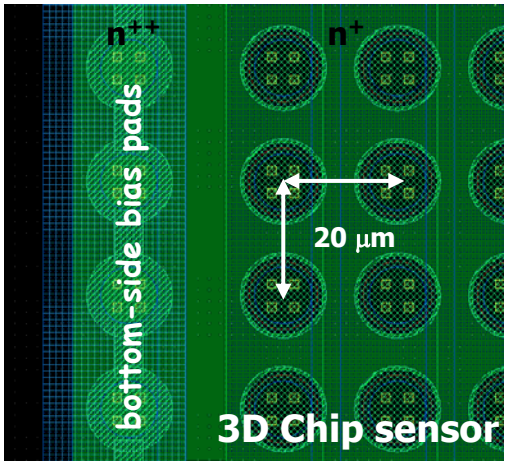


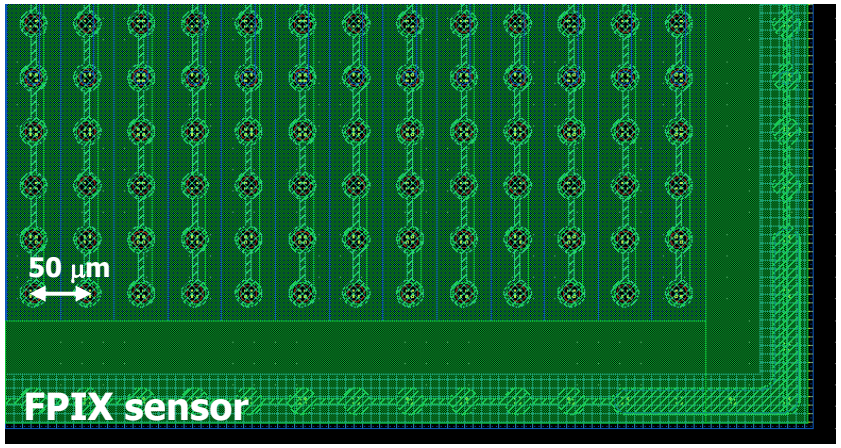
Thinned Edgeless Sensors

- **Note: LL 3D process has been used with a thinned, edgeless sensor layer as the bottom tier, which is the ultimate goal of our 3D development**

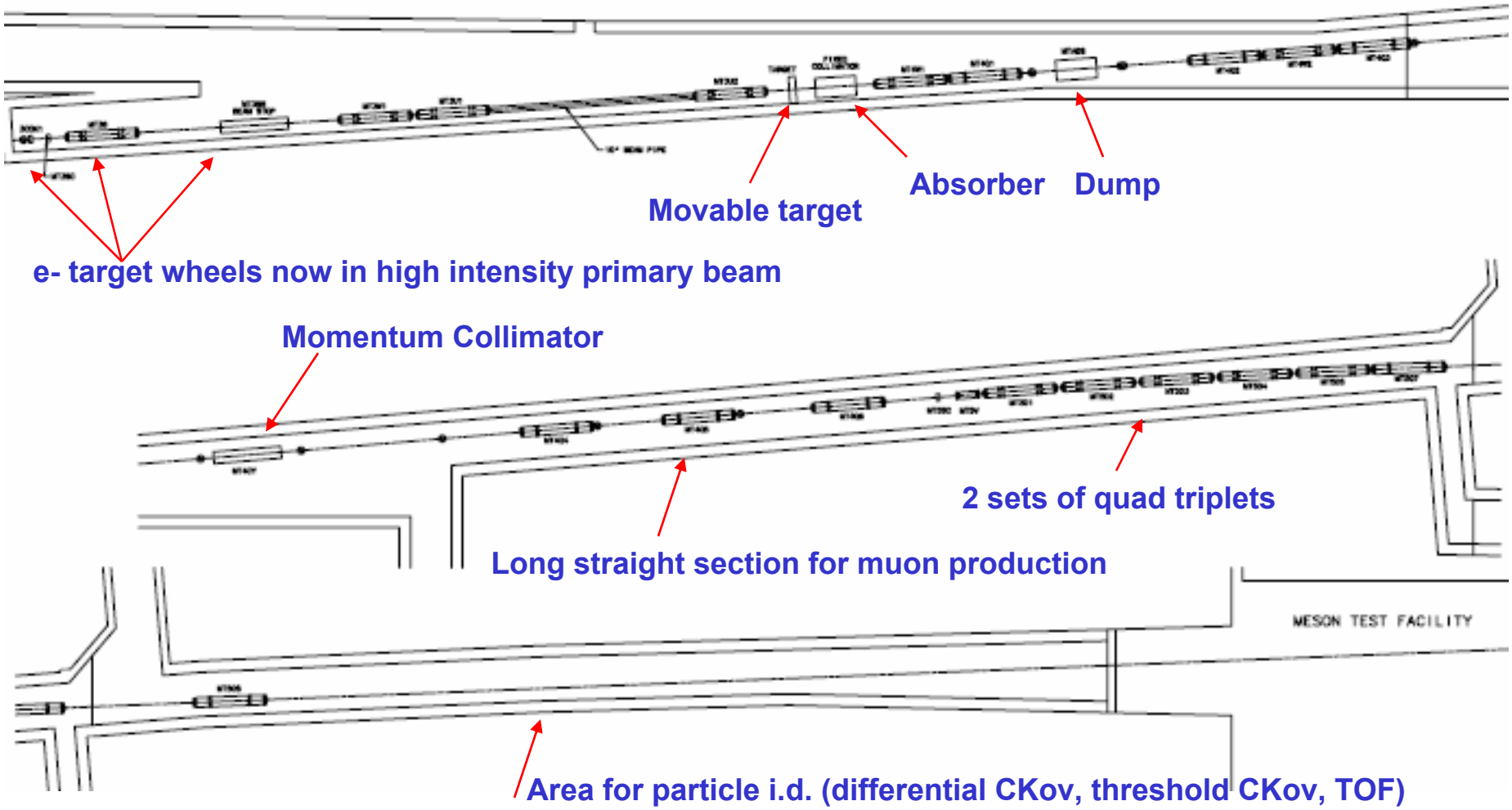
- **First design which, in principle meets 'all' of the ILC requirements for thickness, resolution, power dissipation, time stamping**
  - **Power is 0.75 microwatt/pixel ~ 18.75 microwatts/mm^2 (after pulsing)**
  - **Noise is ~30-40 e$^-$**
  - **S/N = 100-200:1**







Beam Layout



- **Move 13 magnets, add 7 new elements, add Hall probes, add low current power supplies, move beam line transversely including trim magnets, instrumentation, vacuum pumps**