Linear Collider Detector R&D at Fermilab

Fermilab Annual DOE Review

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Fermilab

For the Fermilab ILC Detector Group

Fermilab
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Fermilab's Role

- **There are two distinct and crucial roles the laboratory should play for a leadership position within the ILC detector community**

- **'Local Role'**
  - **R&D carried out by the laboratory itself, in collaboration with other groups**
    - There needs to be an intellectual involvement in the ILC detectors and the physics, building on the strengths of the laboratory
    - Fermilab is a natural place to have a well-balanced program between the ILC, Tevatron and also the LHC efforts, including the users.

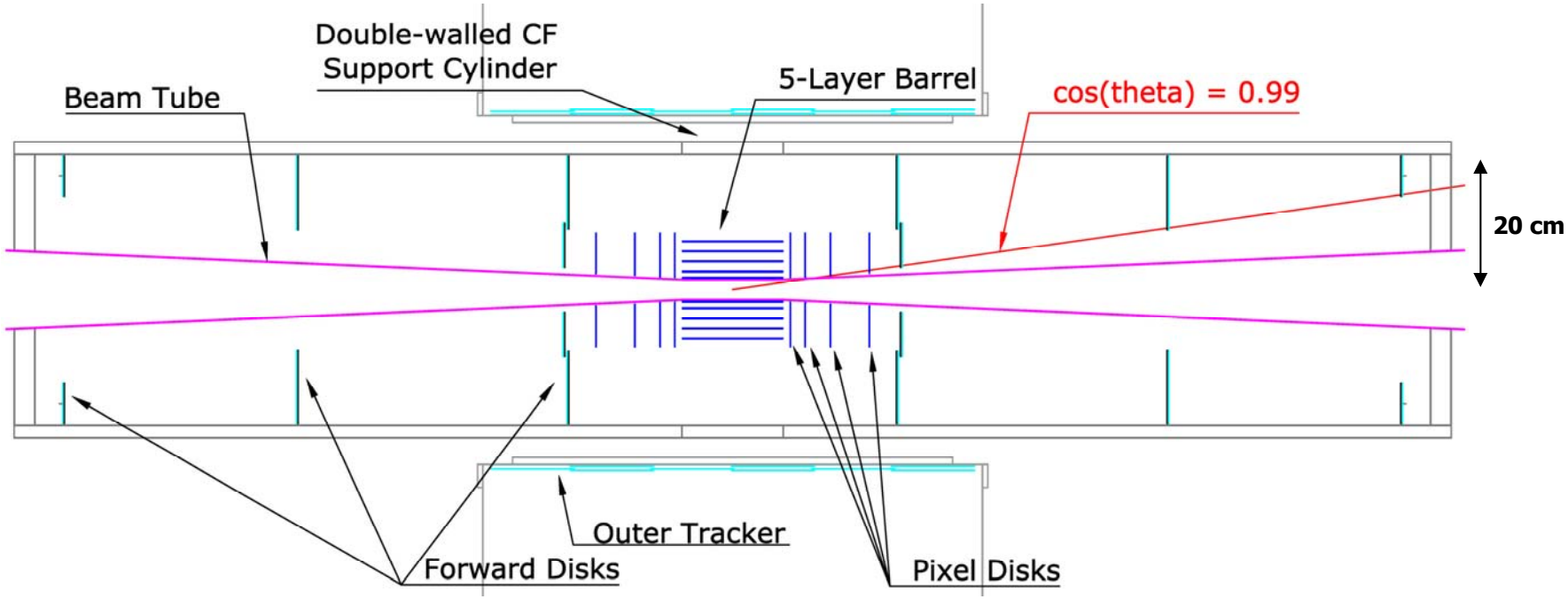
- **'Global Role'**
  - **Role as a host laboratory creating a global, inviting environment for ILC collaborators, independent of detector concept, to establish a coherent program for detector studies**
    - Fermilab test beam facility, with associated support
    - Analysis support center
    - Fermilab as facilitator

Outline

- ***Highlights of laboratory's current ILC detector R&D***
  - **Silicon Vertex Detector**
  - **Silicon Tracker**
  - **Calorimetry**
  - **Solenoid**
  - **Muon system**
- ***Fermilab's support and community role***
  - **Test beams**
  - **Machine-Detector Interface**
  - **Peripheral Support**
  - **Community Activities**
- ***Program Organization***
  - **Budget and Effort**
- ***Plans, Goals and Conclusions***

Vertex Detectors

- **Multi-layered, high precision, very thin, low mass detectors**
  - **Layer thickness of 0.1% X_0 per layer, equivalent of 100 μm of Si**
  - **High granularity: 5 - 20 μm pixels; 10^9 pixels for barrel detector**
  - **Modest radiation tolerance**
- **Low mass approaches**
  - **Reduce mass using alternate materials**
  - **Reduce power so less mass is needed to extract heat**
- **Integrated mechanical design of an ILC vertex detector by Fermilab**

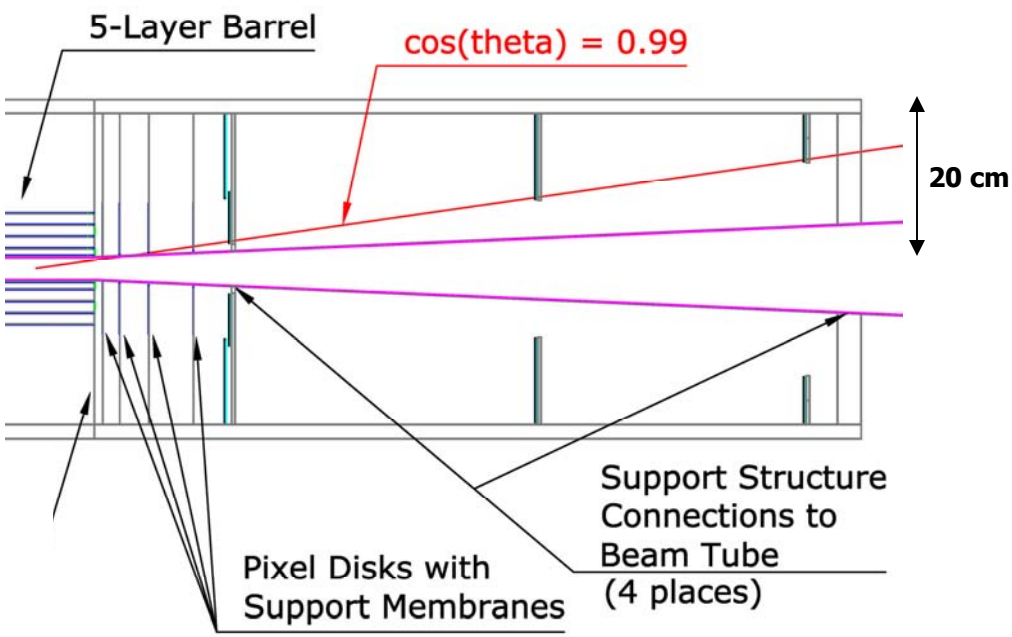


Integrated Vertex Detector Design

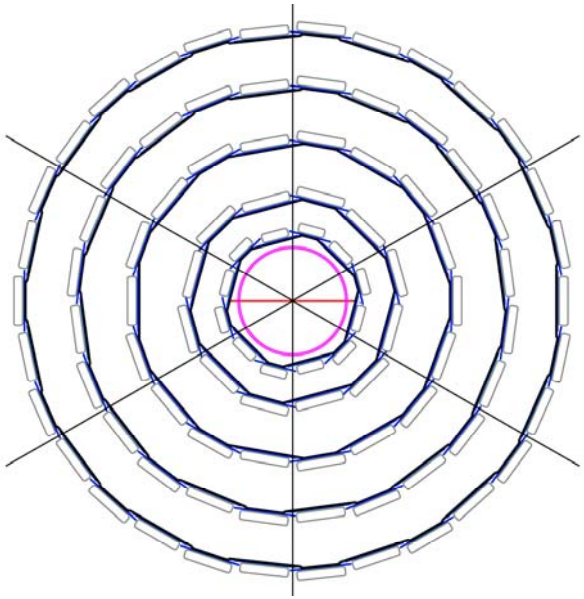
- Vertex detector mounted in an outer, double-walled support cylinder
  - Cylinder is split along beam line to allow assembly around beampipe
  - Cylinders couple to the beam tube at z = ± 214 and ± 882 mm, and are supported by the beam tube, and stiffen it
- Carbon fiber membranes support the barrel and disks

- Barrel Region
  - Five layers
  - Longitidunal coverage: ± 62.5 mm
  - Radial coverage: 14 < R < 61 mm

- Forward regions
  - Four disks
  - z = ± 72, ± 92, ± 123, ± 172 mm
  - Radial coverage: R < 71 mm



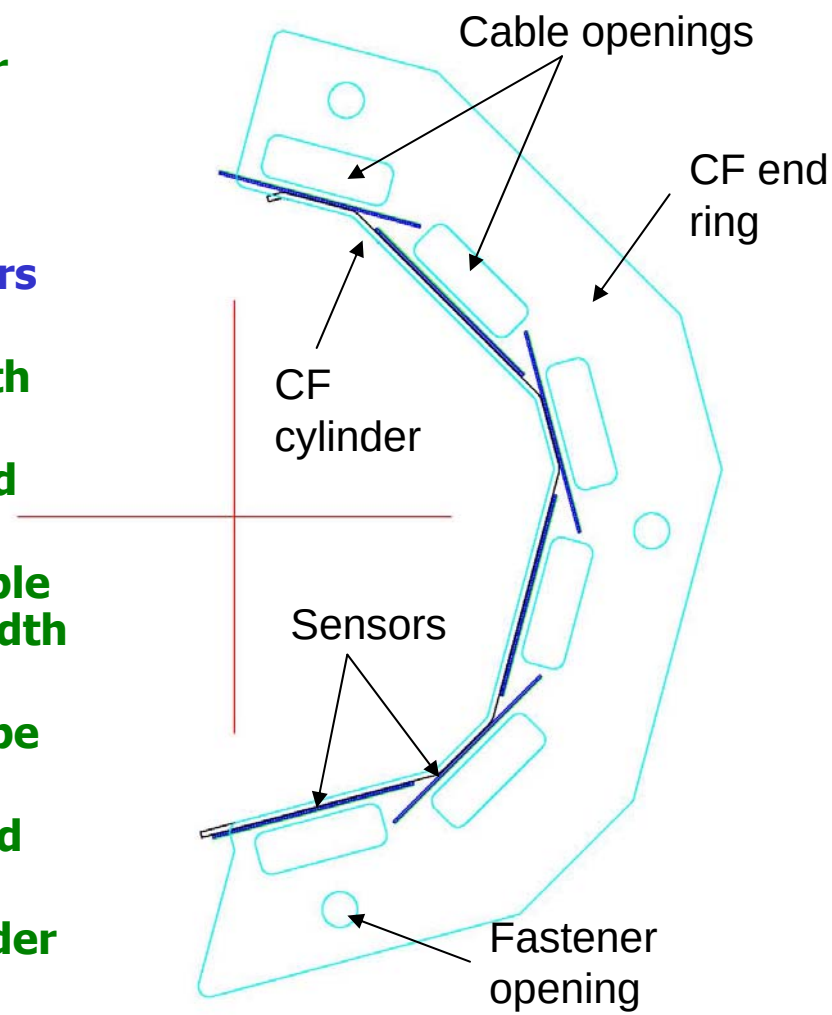
side view



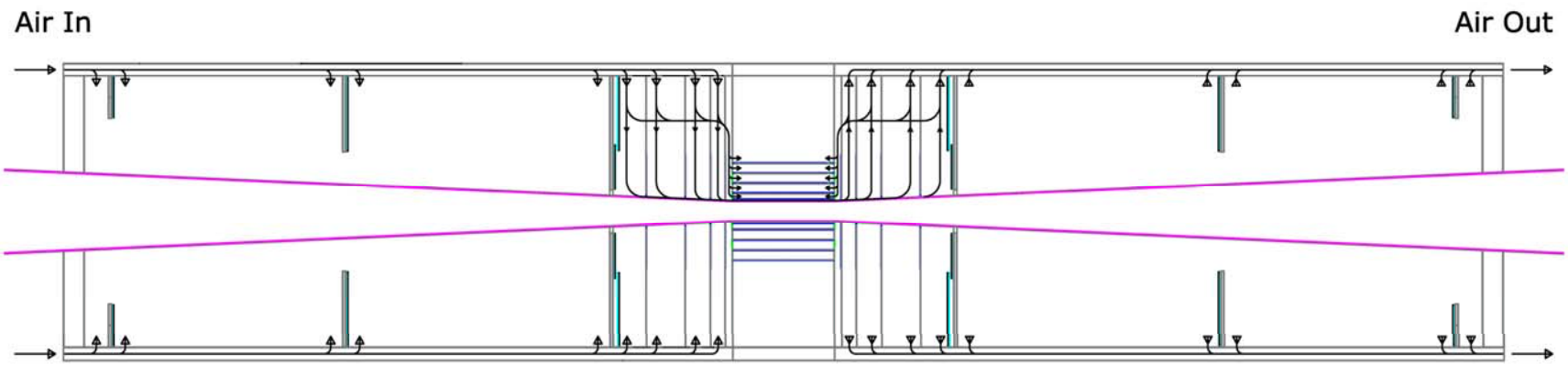
end view

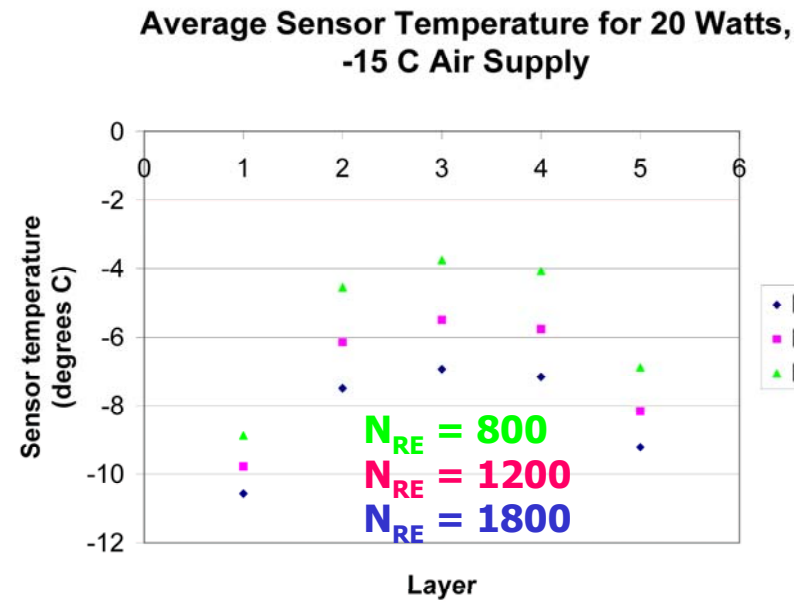
Vertex Detector Barrel Layers

- **Barrel layer geometry**
  - **6-fold symmetry**
  - **2 types of sensors; A and B sub-layer geometry**
  - **To reduce mass, barrel layers are glued to form a unit.**
- **Design has CF polygonal support cylinders which cover 180°.**
  - **Cylinders would be single-walled with 3 or 4 plies.**
  - **180° annular rings at each end would control out-of-round.**
  - **Openings in those rings to pass a cable and its connector, but not the full width of a sensor.**
  - **To control material openings would be cut into CF leaving lattice-work.**
  - **Sensors glued to the CF with required electrical insulation / connections.**
  - **Up to 15 sensors would be in a cylinder sub-assembly.**



Vertex Detector Cooling

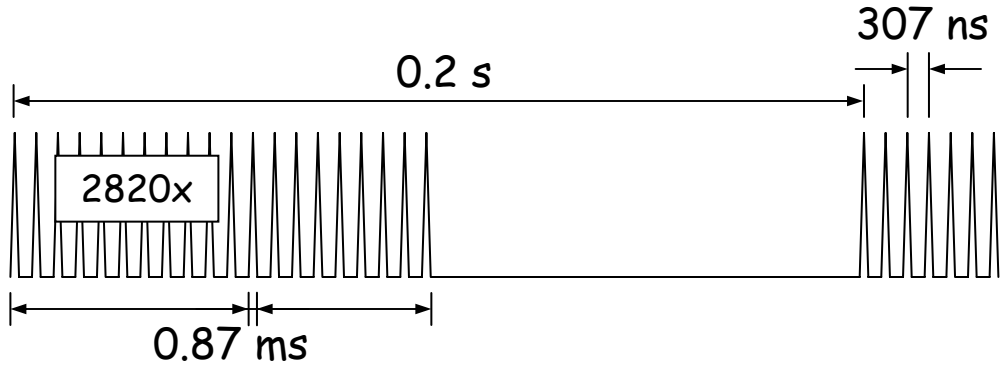




- Assumed sensors are cooled by forced flow of dry air
- Sensor operating temperature > -10° C.
- Dry air was assumed to enter the barrel at a temperature of -15° C
- Assumed no heat transfer from the beam pipe to the innermost layer, that is, the beam pipe would have thermal intercepts.
- Total power dissipation of 20 Watts was assumed for the barrel
  - power dissipation of central pixel sensors of 131 μW/mm^2
  - power dissipation in the forward disks of 33 μW/mm^2

Sensor Technology

- **Sensor challenge due to beam structure**

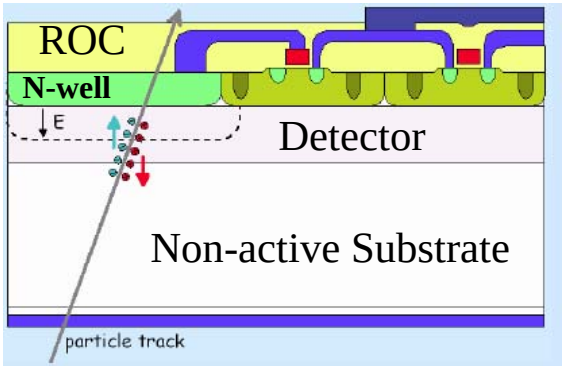


- **What readout speed is needed ?**
  - **Inner layer 1.6 MPixel sensors**
    - Once per bunch = 300ns per frame : *too fast*
    - Once per train ~100 hits/mm^2 : *too slow*
    - 5 hits/mm^2 => 50μs per frame: may be tolerable
      - Note: fastest commercial imaging ~ 1ms / MPixel
- **Major R&D effort in CMOS sensors**
  - **Readout during bunch trains**
    - CCD's, MAPS, DEPFET, SOI, Hybrid, …
  - **Readout between trains**
    - FAPS, ISIS, 3D, …

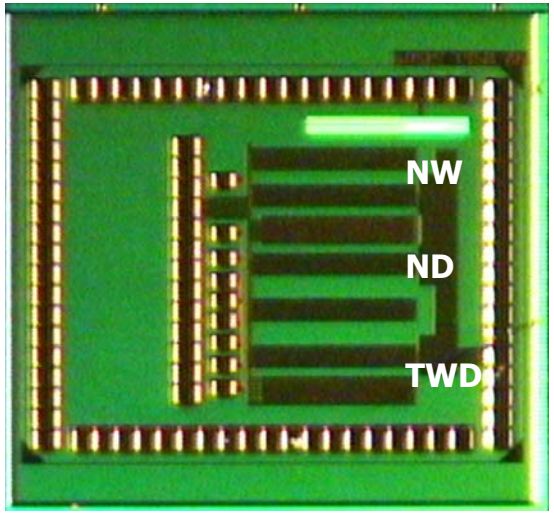
Monolithic Active Pixel Sensors

- **A MAPS device is a silicon structure where the detector and the primary readout electronics are processed on the same substrate**
- **MAPS can be divided into two classifications:**
  - **Those using standard CMOS processes**
  - **Those using specialized processes**

- **As introduction into this area submitted a 130 nm chip in IBM CMOS process to study characteristics:**
  - **Feature devices on chip**
    - Registers for SEU evaluation
    - LVDS drivers
    - Test devices
  - **Pixel layout**
    - 80 row x 3 column pixel readout array
      - Column with no diodes
      - Column with N-well
      - Column with triple N-well
    - Fine pitch readout circuit: 10x340 μm
    - Fine pitch diodes, 10 x 150 μm, connected to readout circuits
  - **In process of characterizing performance**



MAPS Principle

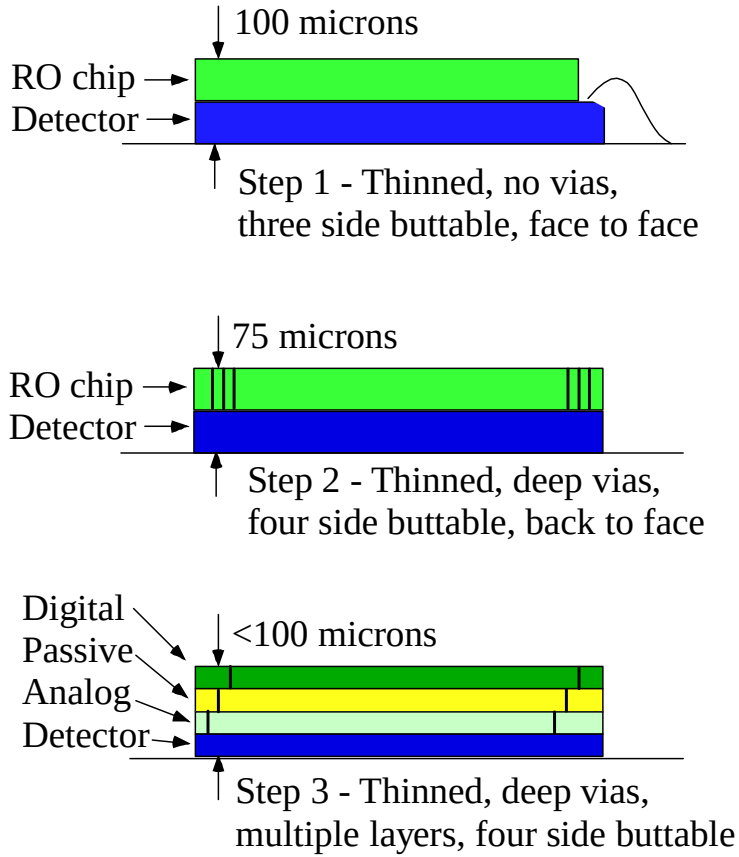


3x80 pixel array

- **Evaluated a FAPS device from the University of Hawaii**

3D Technology

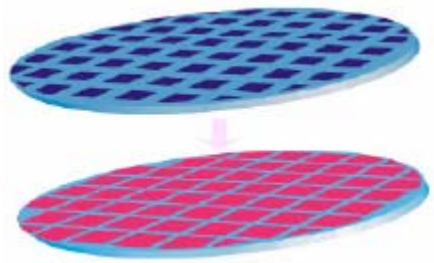
- **A 3D device is a chip comprised of 2 or more layers of semiconductor devices which have been thinned, bonded, and interconnected to form a monolithic circuit**
  - **Layers can have devices made in different technologies**
    - Process optimization for each layer
- **Technology driven by industry**
- **We believe that this technology holds enormous promise for particle detectors and matches well with our strength and expertise**
- **Critical issue are:**
  - **Thinning of the layers**
  - **Bonding of the layers**
  - **Establishing the electrical interconnects**



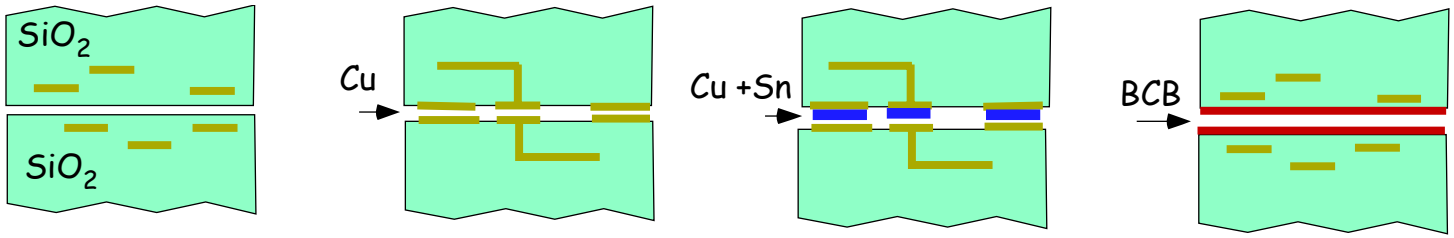
3D Process

- **Wafer thinning**
  - **Thinning of individual tiers may be done before or after bonding to another tier.**
  - **Thinning is generally done by grinding and lapping followed by etching (plasma or wet) and CMP (chemical mechanical polishing)**

- **Wafer bonding**
  - **Bonding approach**
    - wafer to wafer bonding
    - die to wafer bonding
  - **Bonding techniques**



wafer to wafer bond



Direct silicon bonding

Copper to copper bonding

Copper-tin eutectic bonding

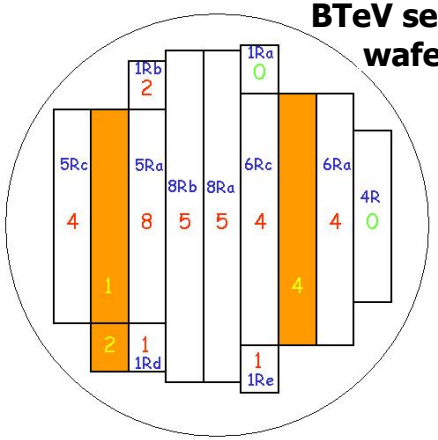
Adhesive (BCB) bonding

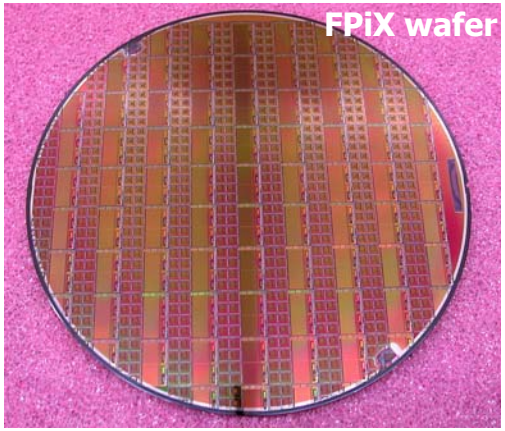
- **Electrical connectivity**
  - **Pad contacts in bonding process**
  - **Through wafer via formation**

Thinned Devices

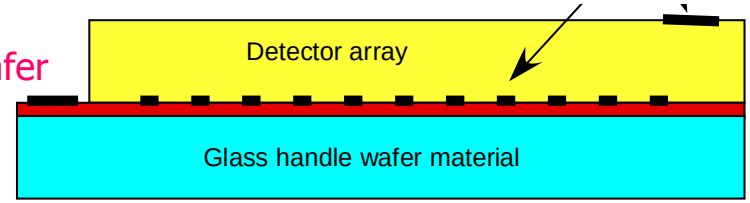
- **Utilize existing inventory to characterize and gain experience with thinned devices, which are well understood before thinning**
  - **Use BTeV 4" sensor wafers, 270 mm thick**
    - Five/One/Three/Three/Two 1/4/5/6/8 chip arrays
  - **Use 8" FPIX readout chip wafers**
    - TSMC 0.25 u CMOS, 760 microns thick
    - Wafer shared with TRIPt chip
    - About 130 FPIX chips/wafer
- **Placed order with RTI, NC, for thinning**
    - Add Cu (and Sn) to pads on face of each wafer.
    - Place handle wafer on face side of FPIX wafer and reduce thickness to 75, 50, 25 and 15 microns

BTeV sensor wafer



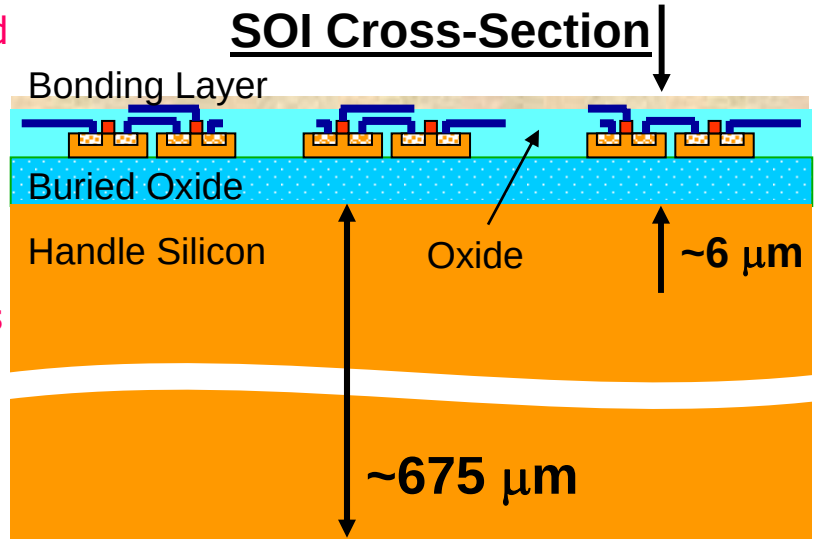


- **Expect to proceed with bonding**
  - **Possible procedure**
    - Place handle wafer on back side of FPIX wafer
    - Remove handle wafer from face side of FPIX wafer
    - Dice FPIX wafer, section detector wafer
    - Bond FPIX die onto wafer detector sections.



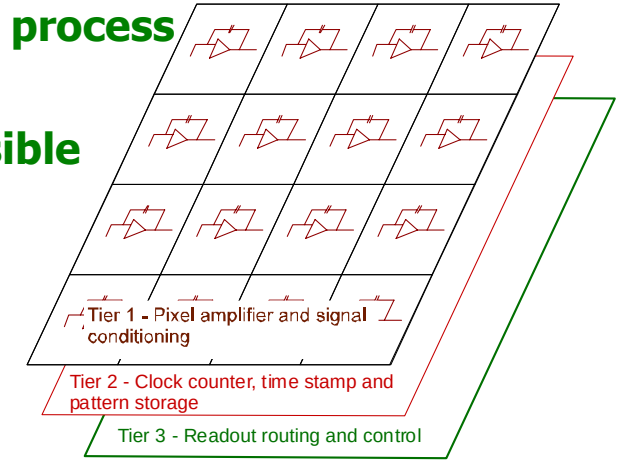
3D Devices – MIT - LL

- **We have started a collaboration with MIT-Lincoln Laboratory: Federally-Funded Research and Development Center run by MIT under contract with the Air Force**
- **MIT-LL Program**
  - **Developed technologies enabling 3D integration**
    - Precision wafer-to-wafer overlay
    - Low-temperature wafer-to-wafer oxide bonding
    - High-density wafer-to-wafer electrical interconnects
  - **Demonstrating the 3D technology by fabricating high-definition 3-layer imaging modules**
  - **Has infrastructure to allow for 3D Multi-project Run fabrication**
- **Uses Silicon-on-Insulator (SOI) for 3-D Circuit Integration**
  - **Advantages:**
    - The electrically active portion of an integrated circuit wafer is < 1% of the total wafer thickness
    - Buried oxide layer in SOI provides ideal etch stop for wafer thinning operation prior to 3D integration
    - Full oxide isolation between transistors allows direct 3D via formation without the added complexity of a via isolation layer
    - SOI's enhanced low-power operation



3D Device Design

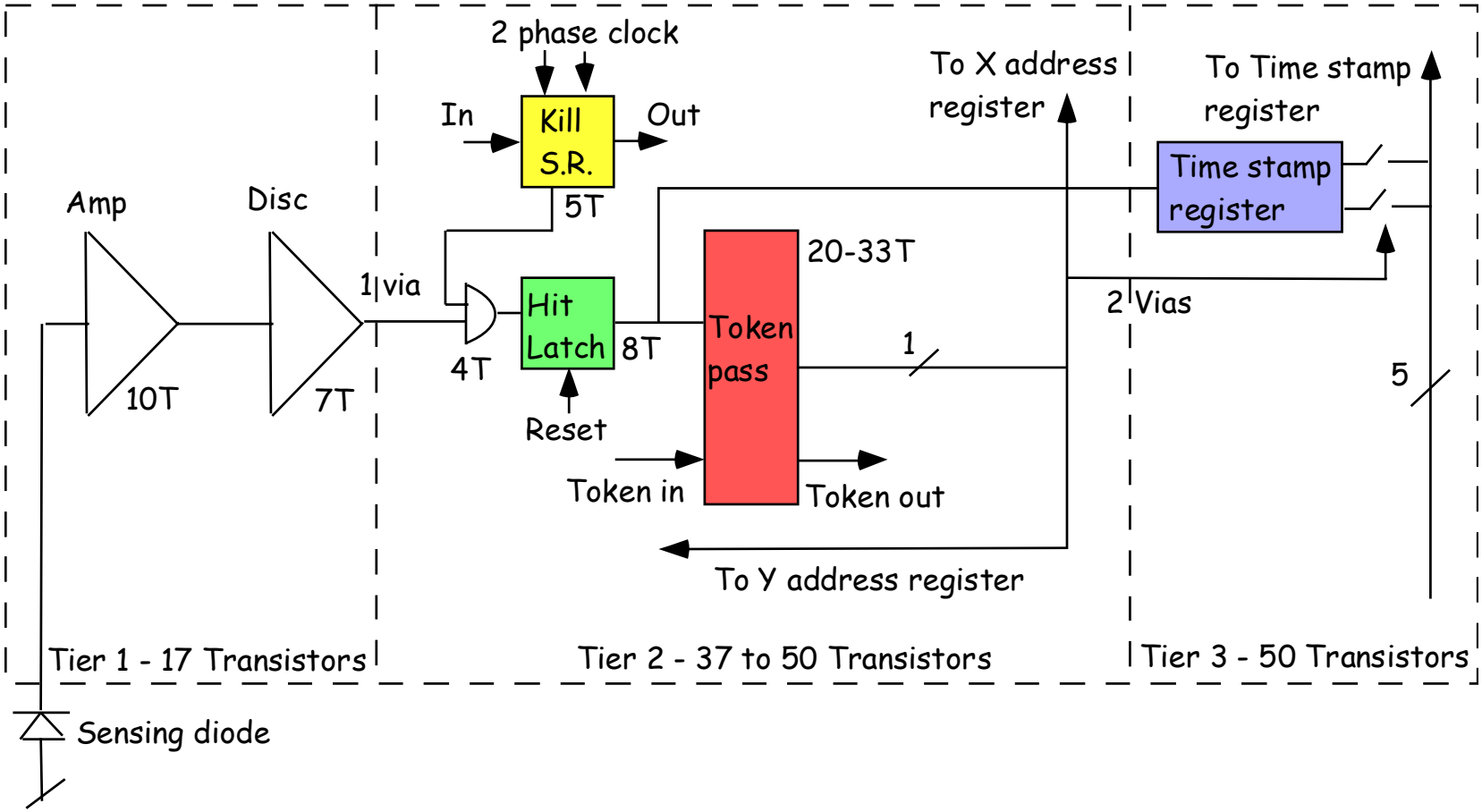
- **Invited to participate in the MIT-LL three-tier multi-project run**
  - **3D design to be laid out in MIT LL 0.18 um SOI process**
  - **3 levels of metal in each layer**
  - **40 transistors in a 15 x 15 um cell may be possible**
- **Submission deadline is Oct. 1, 2006**
- **Requested wafer space of 1.5 x 1.5 mm^2**
- **Suggested pixel size 15 x 15 um; expect 40x40 pixel arrays in 3D device structures**



- **Design:**
  - **Time stamping of pixel hit for ILC environment**
    - Divide bunch train into 32 time slices, pixel can store one time stamp equivalent to 5 bits of time information
  - **Sparsification to reduce data rate**
    - Use token passing scheme developed for FPIX and FSSR to reduce data output
      - During acquisition, a hit sets a latch
      - Sparse readout performed row by row with x- and y-address counter
      - While reading out first address, scan ahead looking for next hit

3D Device Design

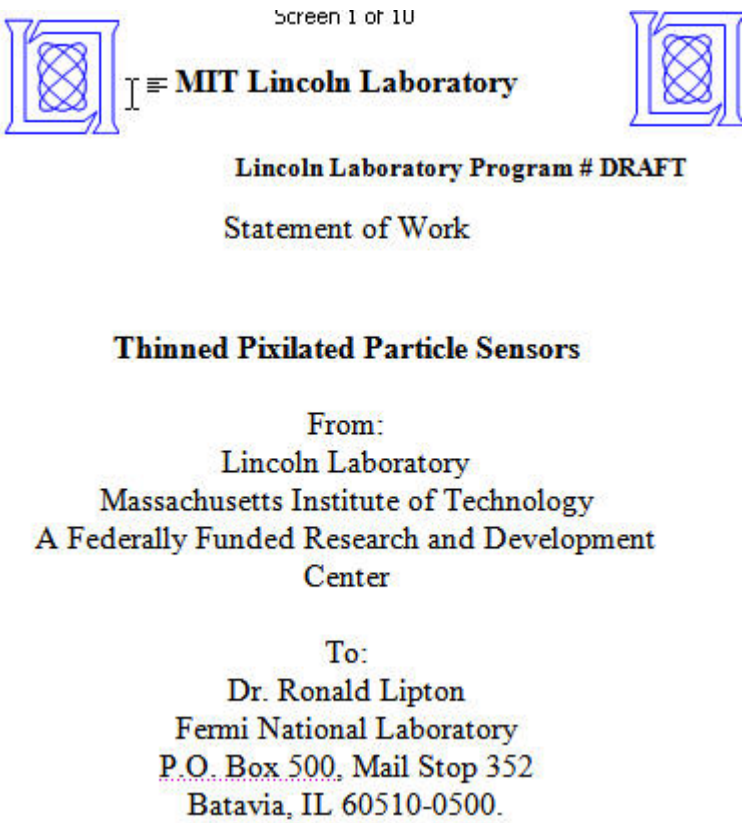
- **First pass at pixel cell block diagram**



- **Layout aggressive for 15x15 μm pixel size (0.18 μm SOI process)**
- **Only one/two vias needed for tier 1-2/2-3 for electrical connection per pixel**

Sensors for 3D Device

- DARPA (Defense Advanced Research Projects Agency) funded 3D run will only provide us with readout circuitry
- 3D Readout needs to be mated to the appropriate sensor, which have the appropriate pitch, corresponding to the readout chips
- Layout of 6" wafer is in progress
  - Standard p-on-n diodes
  - ALICE sensors
  - BTeV sensors
  - ...
- Statement of Work and contract with Air Force being drafted by local DoE office



Screen 1 of 10

MIT Lincoln Laboratory

Lincoln Laboratory Program # DRAFT

Statement of Work

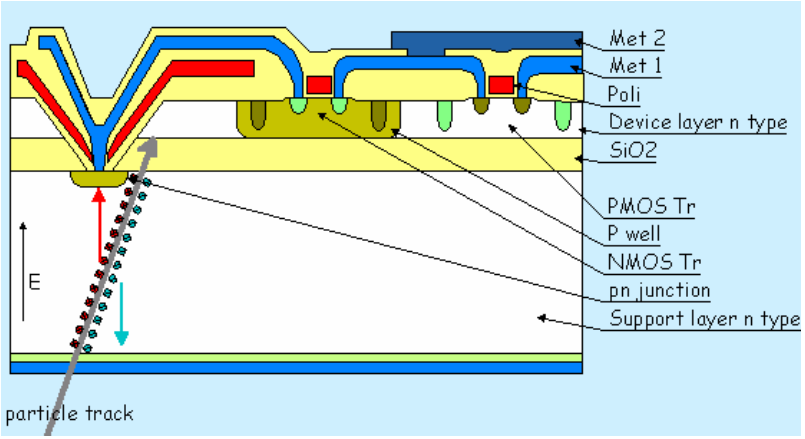
Thinned Pixilated Particle Sensors

From:
Lincoln Laboratory
Massachusetts Institute of Technology
A Federally Funded Research and Development Center

To:
Dr. Ronald Lipton
Fermi National Laboratory
P.O. Box 500, Mail Stop 352
Batavia, IL 60510-0500.

SBIR

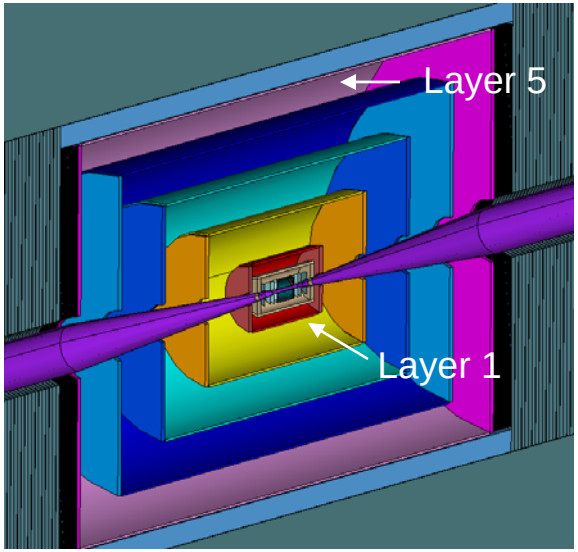
- **Collaboration with industry through SBIR/STTR grants**
  - **SBIR = Small Business Innovation Research grant**
  - **STTR = Small Business Technology Transfer grant**
- **Collaboration with American Semiconductor, Inc. (ASI) on SOI detector R&D**
  - **Located in Boise, Idaho (http://www.americansemi.com/)**
  - **Has access to state-of-the art 130 and 180 nm processing facilities**
- **Silicon on Insulator (SOI)**
  - **Non-standard process**
  - **Handle wafer, normally passive, is the detector**
  - **Signal collected in fully depleted substrate, thus large signals**
  - **Electronics in the device layer**
  - **Should be rad. hard; can have NMOS and PMOS transistors**

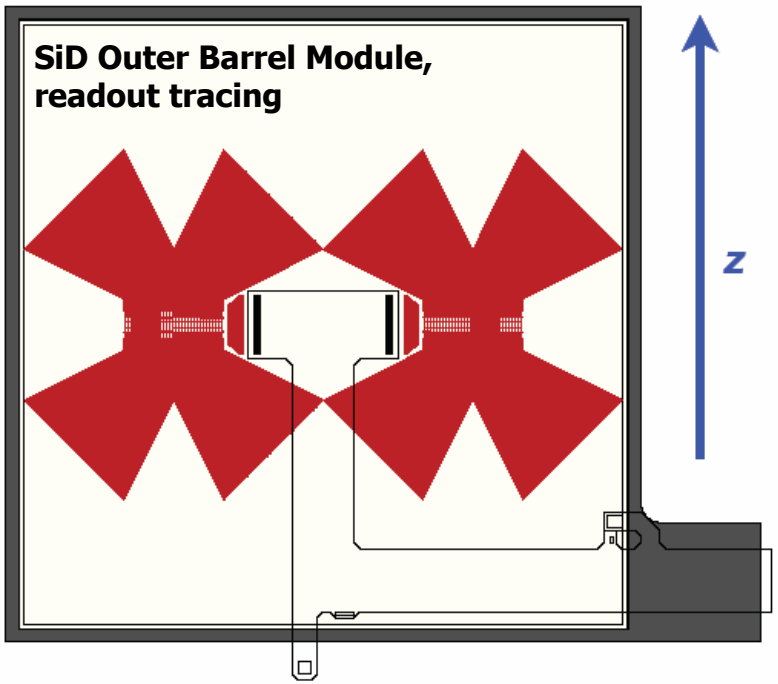


- **Submitted three STTR proposals in collaboration with Fermilab**
- **One proposal granted**
  - **ILC SOI device**
    - Feasibility demonstration for the development of a new low-mass, high-speed, radiation-hard sensor for ILC use.
      - The proposal calls for Fermilab to work with ASI on the pixel design and to provide an amplifier design to be used for circuit and radiation modelling.

Outer Tracker Design

- Completed 5-layer tracker design with 5 barrels and 5 disks on carbon fiber supports
- Collaborating with SLAC on module design for barrel tracker (builds on SiD Ecal modules)
  - sensors are 9.75 cm square, axial strips
  - 1920 channels with double-metal layer
  - Two readout chips bump bonded to sensor
  - Limit capacitance to 40 pF, keep S/N > 25





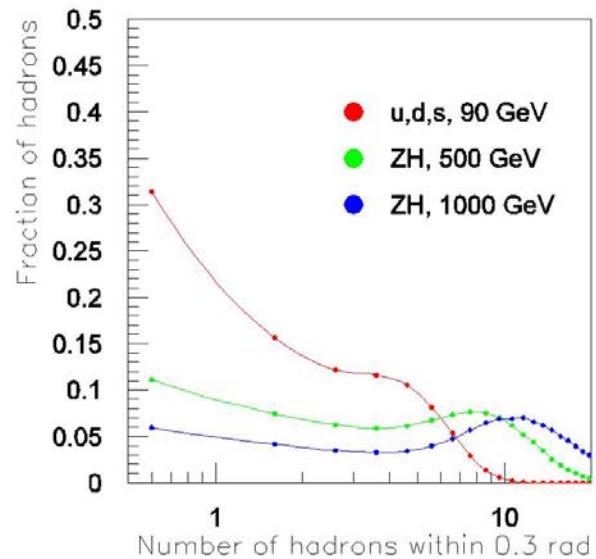
- Designing sensor layout with double-metal layer to equalize capacitive load
- New carbon fiber support frame: 0.125" rohacell between two 9 mil sheets of high-modulus CF composite
- Developing design for module mounting that provides required z overlaps and has adequate precision for standalone momentum measurement

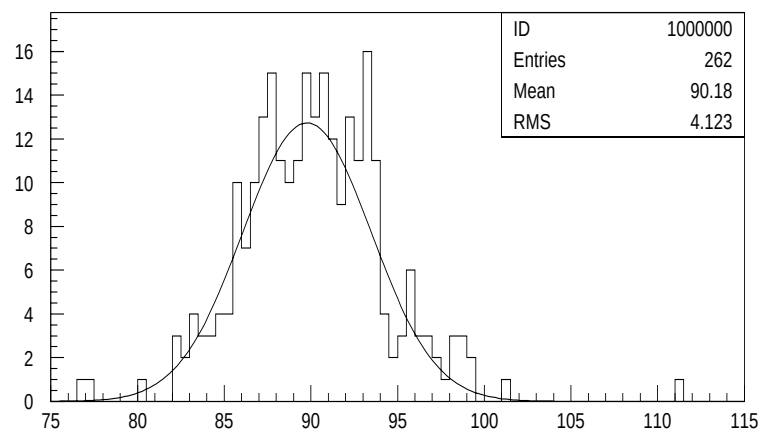
Calorimetry

- **Demonstration of Particle Flow Algorithm (PFA) achieving energy resolution required for ILC physics (separation of W/Z in hadronic decays) is critical**
  - **Calorimeters with unprecedented longitudinal and transverse granularity**
  - **Jet energy resolutions of 30%/√E required**

- **At Fermilab focusing on jet calorimetry for the ILC**
  - **PFA from the perspective of hadronic shower development**
    - Fraction of particles within 0.3 mrad for Z-pole events, ZH production at √s = 500, 1000 GeV
  - **Study the contributions to the jet energy resolution in the Particle Flow Algorithm related to the jet fragmentation function**
  - **Study the systematic uncertainties of the PFA algorithm and design possible experimental tests of its performance**
  - **Optimization of the energy resolution of the scintillator-based hadron calorimeter taking advantage of the fine granularity of the detector**
    - Preliminary non-PFA algorithm obtains energy resolution of 39%/√E for Z-pole events with single Gaussion, no tails

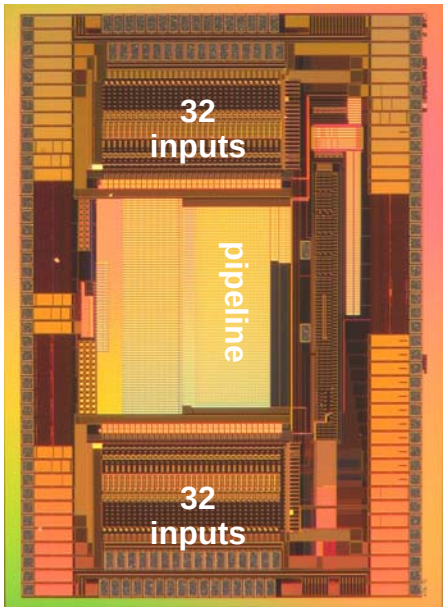
- **In addition we work closely with neighboring institutions on ILC calorimetry**

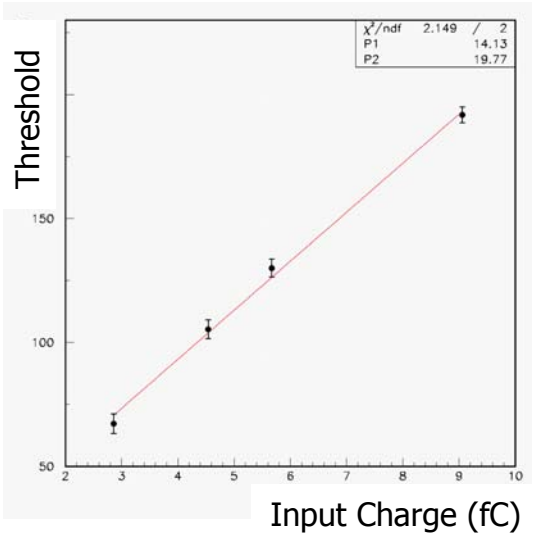




Calorimeter Readout, Digital

- **Readout chip for Digital HCAL for RPC and GEM's designed by Fermilab**
  - 64 channels/chip; 1 cm x 1 cm pads
  - Detector capacitance: 10 to 100 pF
  - Smallest input signals: 100 fC (RPC), 5 fC (GEM)
  - Largest input signals: 10 pC (RPC), 100 fC (GEM)
  - Adjustable gain; Signal pulse width 3-5 ns
  - Trigger-less or triggered operation
  - 100 ns clock cycle
  - Serial output: hit pattern + timestamp
- **Bench tested by ANL**
  - **Chip performs very well**
  - **Chip has full functionality**
- **Requested modifications to chip**
  - **Decrease of input sensitivity by x100**
    - Currently upper threshold corresponds to 7.6 fC
    - Smallest RPC signals ~ 100 fC
  - **Decouple output clock and chip clock**
  - **Redesign will start late May**
- **Submission on July 22nd**
  - **Critical for slice test of set of 10 planes of RPC's in fall 2006 in Mtest test beam**

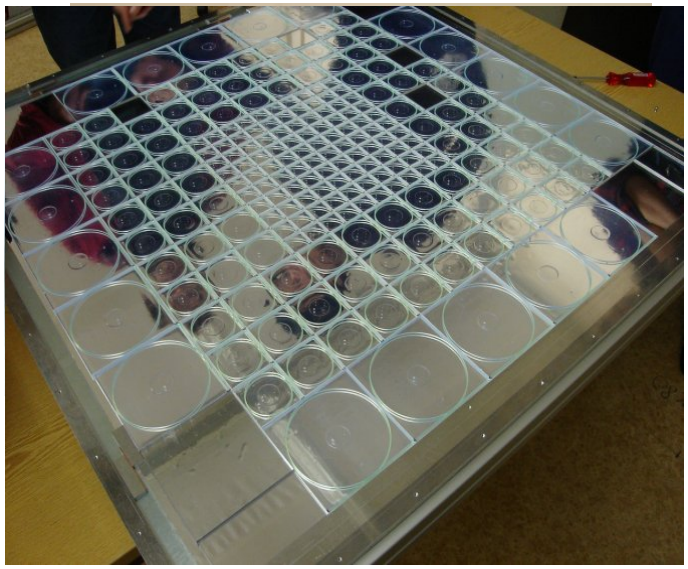


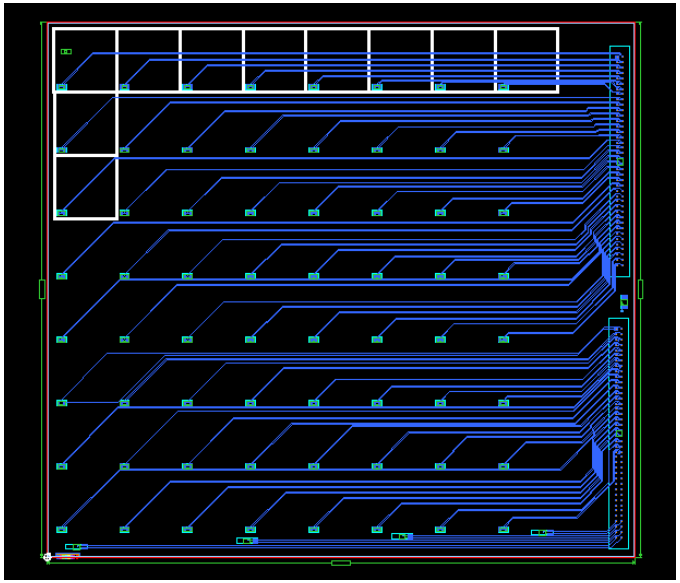


Calorimeter Readout, Analog

- Scintillator tiles with WLS fiber at NIU
- Readout through Silicon Photo Multipliers
  - Pixel Geiger Mode APDs
  - Gain 10^6, bias ~ 50 V, size 1 mm^2 with about 1000 pixels
  - QE x geometry ~ 15%

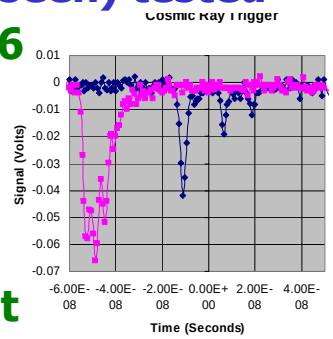
- Fermilab focusing on elec. and mechanical integration; designed PCB for readout
  - 64 Si-pm's and 4 temperature sensors
  - 8 mil trace with 8 mil spaces.
- Studied various options of placing Si-pm's at different angles
- Critical element for full scale test of scintillator based hadron calorimeter / tailcatcher; tests at MTest starting fall 2006

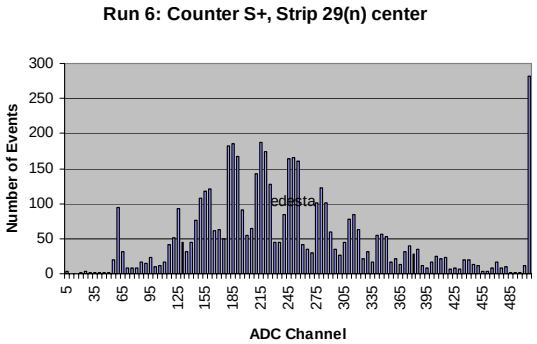




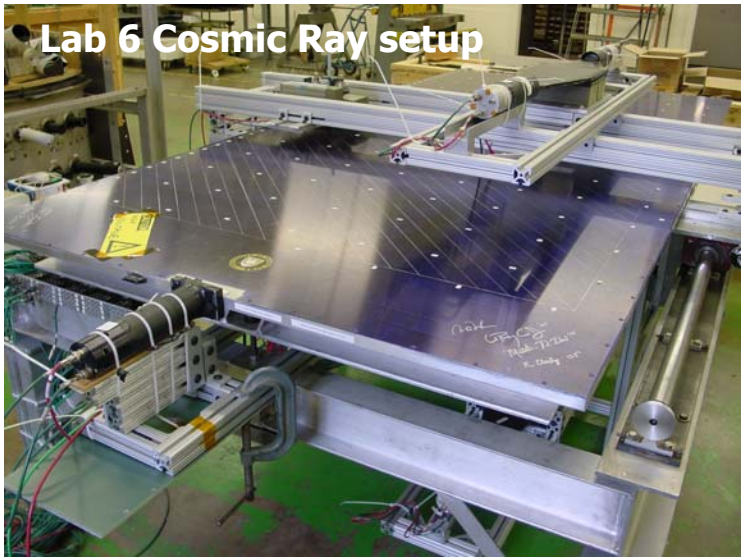
Muon System

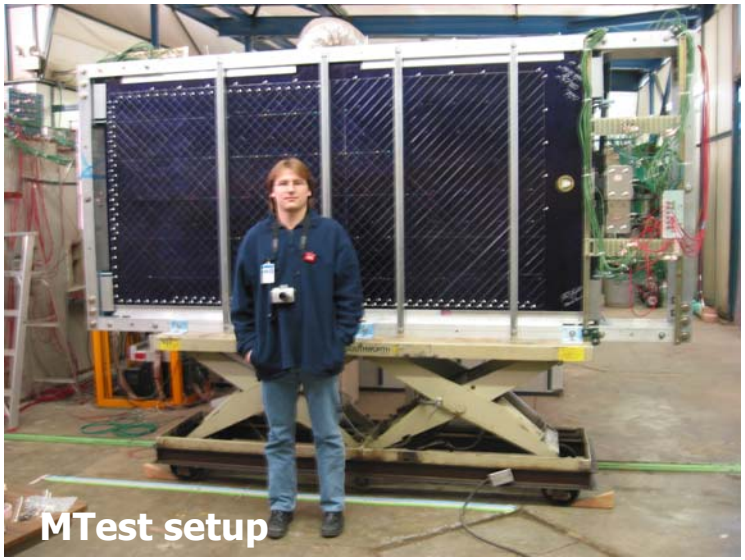
- **Scintillator based muon tracking system**
  - **Scintillator strip panels with Multi-Anode PMT (MAPMT)**
    - Chamber 2.5 m x 1.25 m
    - Strips: 4.1 cm X 1 cm
- **Four planes (out of 8-12 foreseen) tested**
  - **Cosmic Ray setup in Lab 6**
    - 2 chamber setup
    - channels readout with single PMT and MA-PMT
  - **120 GeV protons at MTest**
    - First pass measurement of response to 120 GeV protons





- **Plan to characterize response and move to readout with Si-PM's**

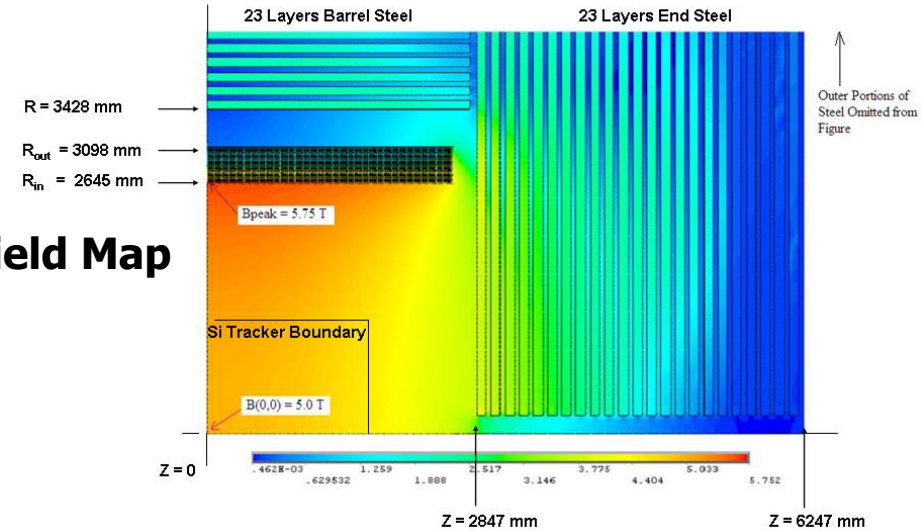


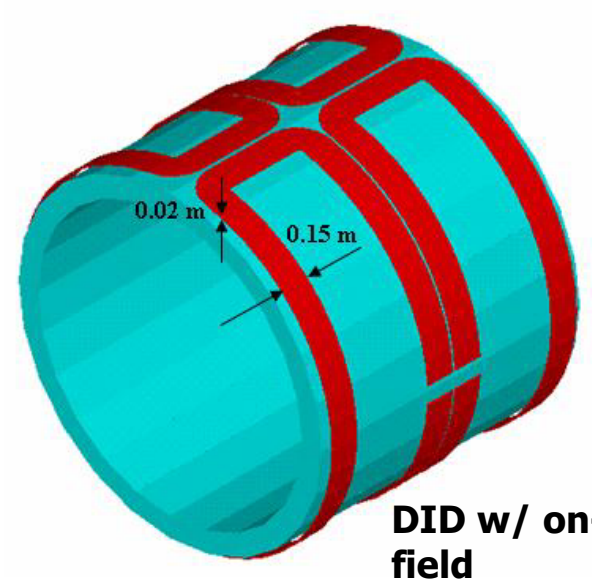


Solenoid

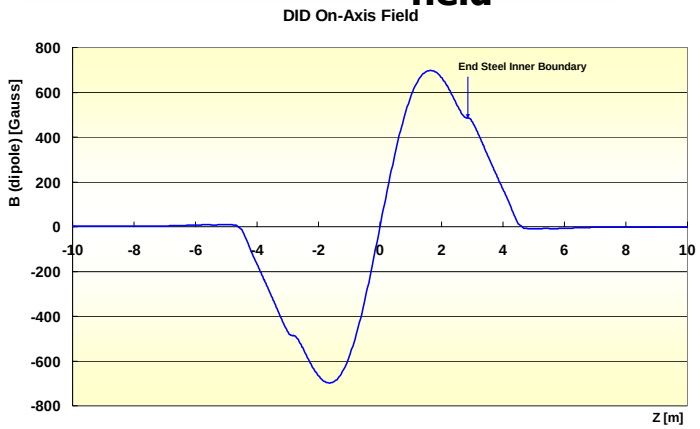
- **Carried out feasibility study of solenoid with B(0,0) = 5T, complete with FEA**
  - **Clear Bore Ø ~ 5 m; L = 5.4 m: Stored Energy ~ 1.2 GJ**
    - For comparison, CMS: 4 T, Ø = 6m, L = 13m: 2.7 GJ

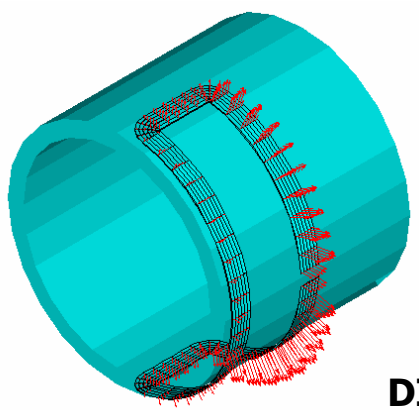
Field Map





DID w/ on-axis field





DID stresses

Testbeam Facility

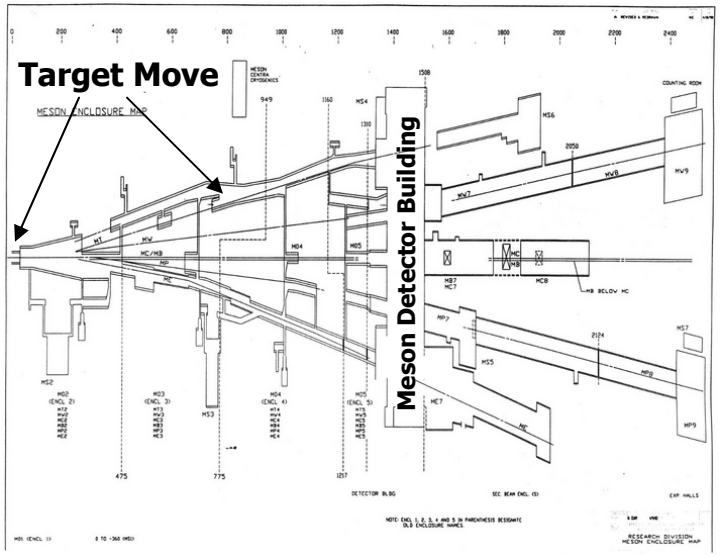
- **Testbeam facility at MT6 set up, commissioned and supported**
- **Testbeam configuration**
  - **Beam parameters:**
    - Momentum between 4 and 120 GeV
    - protons, pions, muons, electrons
    - Resonant extraction
    - Variable intensity
    - 4 second spill every 120 seconds

- **List of MTBF Memoranda of Understanding (MOU):**
  - **T926: RICE Experiment completed**
  - **T927: BTeV Pixel Experiment completed**
  - **T930: BTeV Straw Experiment completed**
  - **T931: BTeV Muon Experiment completed**
  - **T932: Diamond Detector Signed**
  - **T933: BTeV ECAL Experiment completed**
  - **T935: BTeV RICH Experiment completed**
  - **T936: US/CMS Forward Pixel Taking data**
  - **T941: UIowa PPAC Test Experiment completed**
  - **T943: U. Hawaii MA PS Detector Experiment completed**
  - **T950: Kaon Vacuum Straw Tracker Analyzing data**
  - **T951: ALICE EMCAL Prototype Test Analyzing data**
  - **T953: U. Iowa Cerenkov Light Tests Analyzing data**
  - **T955: RPC Detector Tests (Argonne) Taking data**
  - **T956: ILC Muon Detector Tests (Indiana) Taking data**
  - **T957: ILC Tail Catcher (NIU) Taking data**

- **ILC community has proposed an extensive, multi-year, test program at Fermilab (FNAL-TM-2291)**
  - **Proposal needs a long tem occupation (> 1 year) in MTBF**
  - **Broad range of particle types (e,μ,π,p)**
  - **Current plans call for move to Fermilab in 2007**
  - **Requests for high energy electrons (>25 GeV) and low energy pions (1 GeV): can't be met by current facility**

Testbeams for ILC

- **Test beams will be the lynchpin for new detector R&D for the ILC**
- **Currently only one beamline available for test beams**
  - **MTest with 2 enclosures that cannot be operated independently**
  - **Beam does not meet requirements of the ILC community**
- **Further development of the test beam facilities is critical to the success of the ILC**
- **It is both a responsibility and opportunity for the laboratory to invest in the test beam**



- **Room for improvement of the current beamline, which would greatly benefit the ILC community (and NOvA, Minerva)**
- **External Beams Group is working on**
  - **General beamline improvements through reduction of material**
  - **Improved particle id.**
  - **Two schemes to install a movable target 700' downstream from the current target**
    - Option 1: Adiabatic installation, no new magnets, momentum resolution 5%
    - Option 2: New magnets, impact on running, momentum resolution 2%
  - **Both schemes provide for**
    - Secondary pion beams down to 1 GeV with good rate
    - Electron beams up to ~33 GeV

Testbeams for ILC

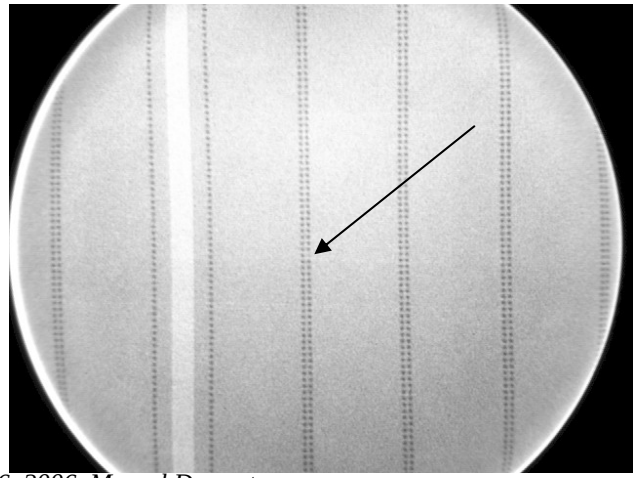
- **Further enhancements of the ILC R&D activities are being explored, with a concurrent scientific program which could benefit the ILC community**
- **MCenter beam line, which houses MIPP, is currently not scheduled**
- **MCenter beamline**
  - **Beamline with excellent characteristics, very well understood**
    - Six beam species ($p^{\pm}$,$K^{\pm}$,$p^{\pm}$) from 1 -- 85 GeV/c
  - **Excellent particle id capabilities**
- **Experimental setup**
  - **Could allow for better understanding of hadron-nucleus interactions, which could benefit our understanding of hadronic shower development, which is currently poorly understood**
    - Large array of nuclei of interest that can be measured with an upgraded MIPP
  - **Moreover, experimental setup with the full spectrometer would allow for a tagged neutron beam from fully constrained reaction pp → p,n,π^+**

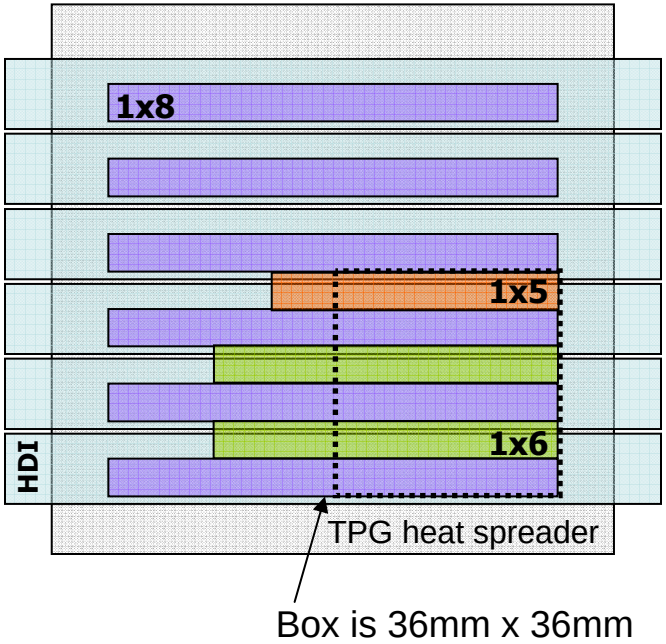
Testbeam Instrumentation

- **As part of the improved testbeam instrumentation, we will build an 8-plane pixel beam telescope with pointing resolution of ~3 μm**
  - **Project uses existing inventory of BTeV experiment**
  - **Overlaps fully with the development and testing of thinned readout chips (FPiX chip with RTI)**
  - **Synergistic, inter-laboratory collaboration with the Phenix experiment to build pixel tracking detector**
- **Layout of beam telescope**
  - **Given variety of devices available from BTeV sensor wafers, various options with regard to size of telescope**
    - 1x8 active area = 73.6mm x 6.4mm
    - light blue shows size of 8-chip HDI

X-ray of Bump bonded FPiX chip on BTeV sensor

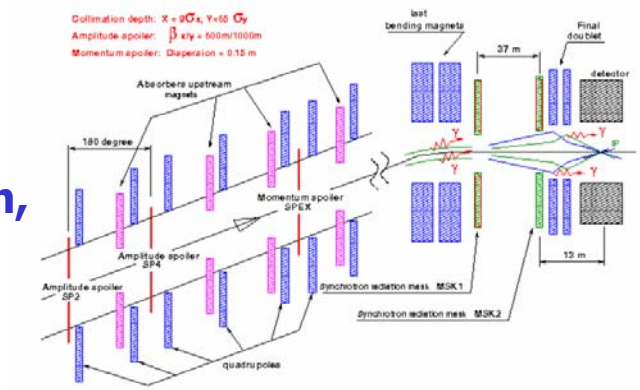
Find the bad bump

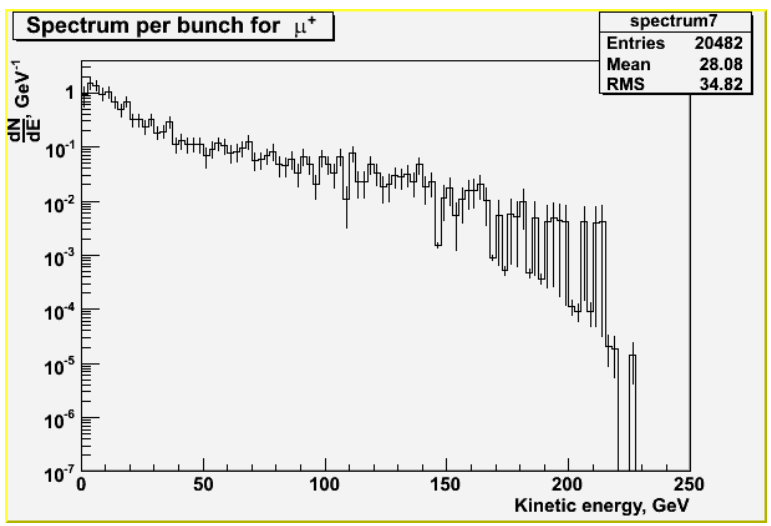


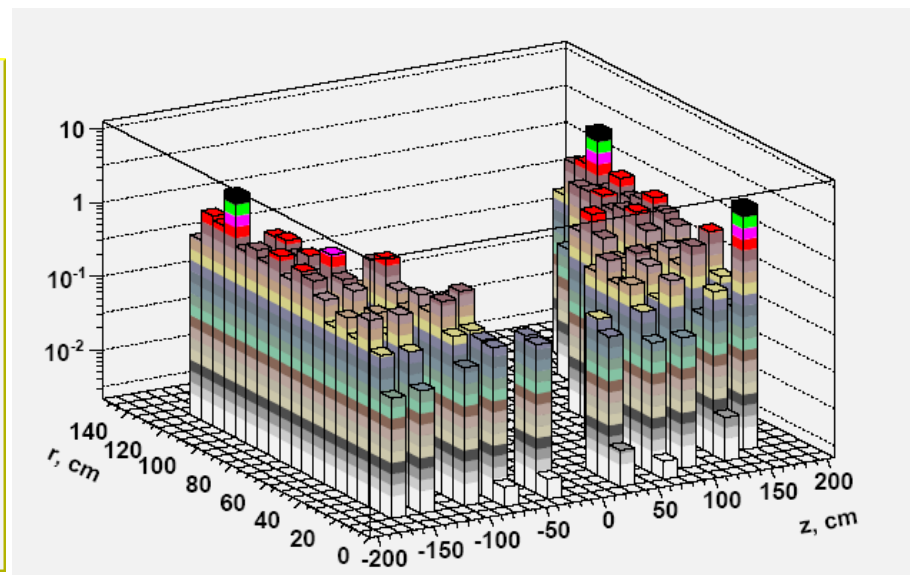


BDIR - MDI

- **Beam Delivery and Interaction Region / Machine Detector Interface group characterized machine related backgrounds in the SID Detector**
  - **Simulations are done with the MARS15 code**
  - **Model describes the last ~1500 m of 20-mrad e^+ line, including all elements**
- **Backgrounds in the SiD detector (2800 bunch/train, 2 10^{10} e^+/bunch) calculated for all particle species**
- **Example, muon energy spectrum in the detector and radial distribution of hits in the tracker end cap without spoilers in beamline**







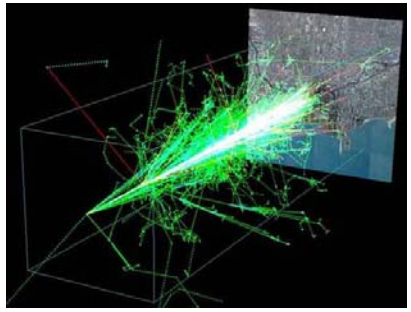
Peripheral Support

- **Simulations**
  - **Activities are accompanied by simulation efforts to optimize the design**
  - **Fermilab Computing Division has installed the Simulation for the Linear Collider (SLIC) framework on Fermilab cluster**
    - SLIC is core North-American simulation package
      - dependencies: Geant4, Xerces, GDML, LCDD, LCIO, LCPhys
      - http://cd-amr.fnal.gov/ilc/slic.shtml
  - **Farmlet available for simulations at ilcsim.fnal.gov**

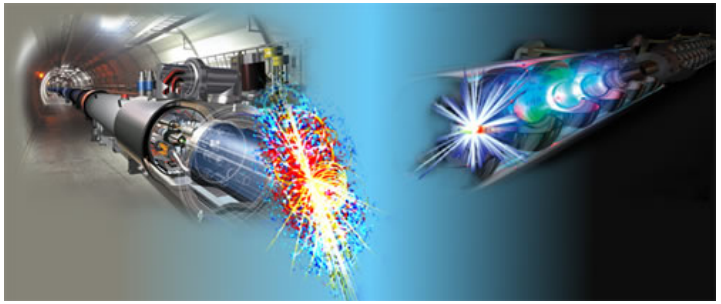
- **Grid**
  - **Active ILC community utilizing**
    - Enabling Grids for E-SciencE (EGEE)
      - European Union sponsored
    - LHC Computing Grid (LCG) infrastructure
  - **Virtual Organization (VO) defined: "ILC"**
  - **All Grid infrastructure made available to the ILC community at Fermilab**
      - http://grid.fnal.gov/

Community Activities

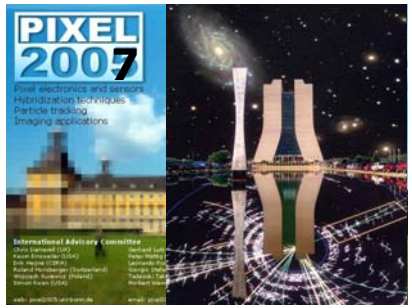
- **Fermilab has initiated and/or offered to host three workshops in the not too distant future**
  - **Taking the lead in addressing issues of critical importance to the ILC and of benefit to the community at large**



  - **Hadronic Shower Simulation Workshop**
    - Understand shortcomings of modeling of hadronic showers
    - Device strategy to address the outstanding issues
    - Fermilab acts as facilitator
    - Sept. 6-8, 2006



  - **ILC - LHC Connections**
    - Investigate how analyses at the LHC could profit from results obtained at the ILC and vice versa.
    - Continuation of previous set of meetings
    - Previous meeting at CERN in Dec. 05
    - Dates: Oct. 12-14, 2006



  - **Pixel 2007**
    - Most significant conference on pixel detector work
    - Use synergies with Astroparticle physcs applications
    - Spring 2007

Budget and Effort

M&S in k$	FY05		FY06		FY07 Request	
SWF in FTE	SWF	M&S	SWF	M&S	SWF	M&S
ILC Detector	~4	200	6.1	400	14	1100

- **Breakdown according to resource for FY06**

Sum of Cum FTE: FY06	Resource Name							
LWWBS Description	Computer Professional	Drafter	Engineer	Engineering Physicist	Scientist	Technical Specialist	Technician	Grand Total
Linear Collider Detector R&D	0.15	0.19	1.80	0.04	3.31	0.29	0.37	6.14

- **Total effort within particle physics division for FY06 expected to be 17.9 FTE's, which includes support for conventional facilities**

- **Request for FY07 does not include SWF and M&S for beam line improvements for the test areas, anticipated to be 6 FTE's and $450k for MTest line only**

Goals, Plans and Conclusion

- **Goals:**
  - **As bidding host laboratory, create an intellectually inviting, supportive environment for ILC collaborators and vibrant user community**
  - **Co-lead and direct world-wide efforts**
  - **As research laboratory, become leader in certain key areas of ILC detector R&D**

- **Plans:**
  - **Build world-class test beam facility with associated support for data acquisition and data analysis**
  - **Take a prominent role in physics benchmarking processes and detector design optimization**
  - **Become the leader in design of pixel sensors for ILC, the readout electronics and the design of mechanical support structures for vertex and tracking detectors**
  - **Participate in the development of the calorimetry for the ILC and the associated algorithms**

- **Conclusion:**
  - **Our ILC Detector R&D has grown considerably over the course of the year and our efforts are more focused; expect to downselect further in the coming year**
  - **We aim at more than doubling our effort in the coming year with focus on pixel detectors and calorimetry with associated simulation support, and significant upgrades to the test beam facilities**