



Run IIb DZero Detector Project

- Run IIb design guidelines
- Project organization
- Technical overview, status
- Schedule, cost overview & status
- Conclusions

Jonathan Kotcher
FNAL DOE Review
March 18-20, 2003



Run IIb Design Guidelines

• Run IIb: increase in instantaneous, integrated luminosity relative to guidelines that drove Run IIa detector design. Laboratory guidance:

	Integrated Luminosity (fb ⁻¹)	Instantaneous Luminosity (X10 ³² cm ⁻² sec ⁻¹)
Run IIa	2	1-2
Run IIb	10-15	2-4
Requirements for Run IIb	Silicon replacement, more rad-hard version	Trigger upgrades (dominated by Level 1)

• Silicon:

- ◆ Current detector designed for ~ 2 fb⁻¹, evidence that it will survive to 3-4 fb⁻¹
 - ▲ The most appropriate radiation-hard technology used at that time
- ◆ After study of various options, have chosen to pursue full silicon replacement
 - ▲ Partial replacement not viable: unacceptable level of technical risk, more down-time for removal/installation, limited SVX2 chip availability, etc.

• Trigger:

- ◆ Increase in luminosity results in unacceptable increase in rates - occupancies, pileup, combinatorial effects
- ◆ Move rejection upstream in readout stream (contain dead time), maintain downstream rejection, event selectivity
- ◆ Address need for higher-bandwidth data logging



Run IIB Project Organization

DO Run IIB Project
 J. Kotcher, Project Manager
 R. Partridge, Deputy; V. O'Dell, Associate; W. Freeman, Assistant
 M. Johnson, Technical Coordinator
 A. Amorn-Vichet, Budget Officer; T. Erickson, Administration

**WBS 1.1
 Silicon**
 M. Demarteau
 G. Ginther

- 1.1.1 Sensors
R. Demina, F. Lehner
- 1.1.2 Readout System
A. Nomerotski, E. von Toerne
- 1.1.3, 1.1.5 Mechanics & Assembly
W. Cooper, K. Krempetz
- 1.1.4 Production
J. Fast
- 1.1.4 QA, Testing, & Burn-in
C. Gerber
- 1.1.6 Monitoring
M. Corcoran, S. de Jong
- 1.1.7 Software & Simulation
F. Rizatdinova, L. Shabalina
- 1.1.8 Administration
(M. Demarteau)

**WBS 1.2
 Trigger**
 H. Evans
 D. Wood

- 1.2.1 L1 Cal Upgrade
M. Abolins, (H. Evans),
P. LeDu
- 1.2.2 L1 Cal/Track Match
K. Johns
- 1.2.3 L1 Track Trigger
M. Narain
- 1.2.4 L2β Upgrade
R. Hirosky
- 1.2.5 Silicon Track Trigger
U. Heintz
- 1.2.6 Simulation
M. Hildreth, E. Perez
- 1.2.7 Administration
(D. Wood)

**WBS 1.3
 DAQ/Online**
 S. Fuess
 P. Slattery

- 1.3.1 Level 3 Systems
D. Chapin, G. Watts
- 1.3.2 Network & Host Systems
J. Fitzmaurice,
S. Krzywdzinski
- 1.3.3 Control Systems
F. Bartlett, G. Savage,
V. Sirotenko
- 1.3.4 DAQ/Online Management
(P. Slattery)

**WBS 1.4
 Project Administration**

**WBS 1.5
 Installation**
 R. Smith

- 1.5.1 Silicon Installation
Mechanical:
H. Lubatti
Electronics:
L. Bagby, R. Sidwell
- 1.5.2 Trigger Installation
D. Edmunds

Installation being managed as integral part of Run IIB project, but not formally part of project baseline

Experienced group, key positions in place since summer CY01. All managers assigned through WBS Level 3.



Subproject Overviews

- **WBS 1.1: Silicon Detector**
 - ◆ Replace with more radiation-hard version, improved b-tagging capability
- **WBS 1.2: Trigger Systems**
 - ◆ **Level 1: Shift some trigger functionality upstream to hardware level trigger**
 - ▲ WBS 1.2.1, L1 Calorimeter Trigger
 - ▲ WBS 1.2.2, L1 Calorimeter/Track Match
 - ▲ WBS 1.2.3, L1 Central Track Trigger
 - ◆ **Level 2: Incremental upgrades to Run IIa systems**
 - ▲ WBS 1.2.4, L2 Beta System
 - ▲ WBS 1.2.5, L2 Silicon Track Trigger
- **WBS 1.3: DAQ/Online System**
 - ◆ Address need for enhanced filtering capability, higher bandwidth data logging
- **WBS 1.4: Project Administration**
 - ◆ Project personnel, travel, miscellaneous supplies
- **WBS 1.5: Installation**
 - ◆ Integration of silicon, trigger installation & pre-beam commissioning



Past Run IIb Milestones, Reviews

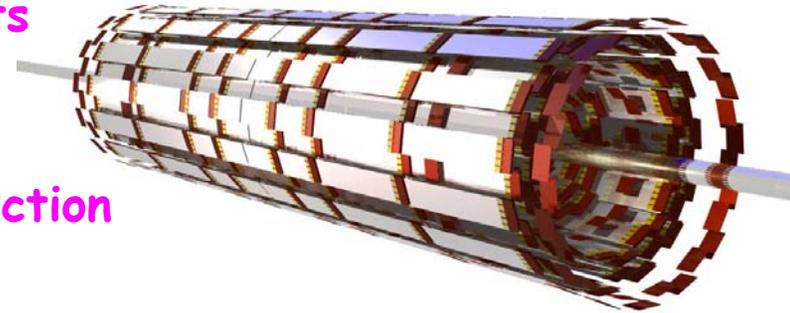
- April/Nov '00: Initial presentations of Run IIb plans to PAC
- June '01: DZero Trigger Task Force, clarify Run IIb trigger needs
 - ◆ Co-chairs: M. Hildreth, R. Partridge
- Nov '01: Silicon TDR and Trigger/Online CDR presented to PAC
- Dec '01: Director's Technical Review of CDF and D-Zero Run IIb Upgrades
 - ◆ Chair: J. Pilcher
- April '02: Director's Review of Run IIb Upgrade Projects
 - ◆ Chair: E. Temple
- June '02: Aspen PAC recommends Stage I approval
- Aug 12-15 '02: Director's Review of Run IIb Upgrade Projects
 - ◆ Co-chairs: E. Temple, J. Pilcher
 - ◆ Project preparedness, quality & depth of staffing noted
- Sep 24-26 '02: DOE (Lehman) Review
 - ◆ "DOE should move forward expeditiously with CD-1, CD-2, CD-3a"
- Nov 04-08 '02: DOE External Independent Review (Jupiter Corporation)
 - ◆ "Well-managed", "quality projects", "reasonable" and "realistic" cost estimates
- Feb 07 '03: DOE approval granted for equipment spending in FY03
- Mar 26-27 '03: P5 Review



Performance of Proposed Detector

- Performance studies based on full Geant simulation

- ◆ Full model of geometry and material
- ◆ Model of noise, mean of 2.1 ADC counts
- ◆ Single hit resolution of $\sim 11 \mu\text{m}$
- ◆ Longitudinal segmentation implemented
- ◆ Pattern recognition and track reconstruction



- Benchmarks

- ◆ $\sigma(p_T)/P_T \sim 3\%$ at $10 \text{ GeV}/c$
- ◆ $\sigma(d_0)^2 = 5.2^2 + (25/p_T)^2$
 - ▲ $\sigma(d_0) < 15 \mu\text{m}$ for $p_T > 10 \text{ GeV}/c$

- b-tagging

- ◆ Loose b-tag algorithm: signed impact parameter
 - ▲ Loose track selection
 - ▲ Impact parameter significance
 - 2 tracks: $d_0/\sigma(d_0) > 3$
 - 3 tracks: $d_0/\sigma(d_0) > 2$
- ◆ b-jet tagging efficiency of $\sim 65\%$ per jet

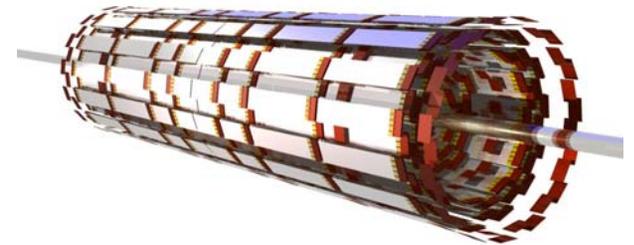
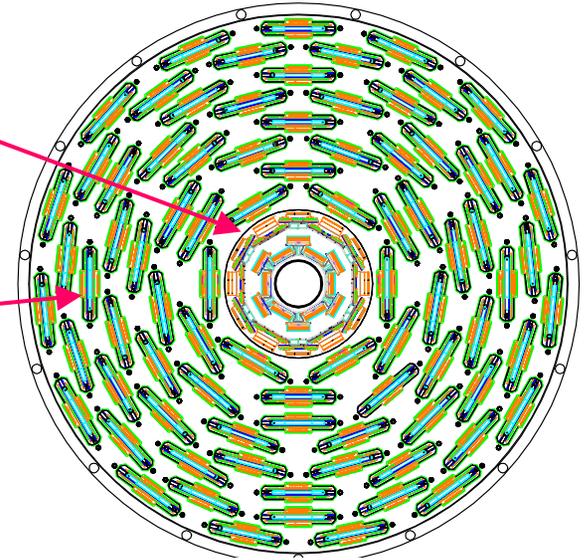
	TDR
$P(n_b \geq 1)$	76%
$P(n_b \geq 2)$	29%
Mistag Rate	$< 1.5\%$

Based on WH-events, with b's falling within acceptance



WBS 1.1: Basic Silicon Design Choices

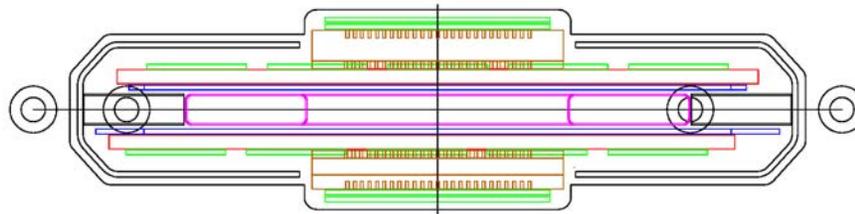
- Six layer silicon tracker, divided into two radial regions
 - ◆ Inner layers: Layers 0 and 1
 - ▲ Axial readout only
 - ▲ Mounted on integrated support
 - ▲ Assembled into one unit
 - ▲ Designed for V_{bias} up to 700 V
 - ◆ Outer layers: Layers 2-5
 - ▲ Axial and stereo readout
 - ▲ Stave support structure
 - ▲ Designed for V_{bias} up to 300 V
- Employ single sided silicon only, 3 sensor types
 - ◆ 2-chip wide for Layer 0
 - ◆ 3-chip wide for Layer 1
 - ◆ 5-chip wide for Layers 2-5
- No element supported from beampipe





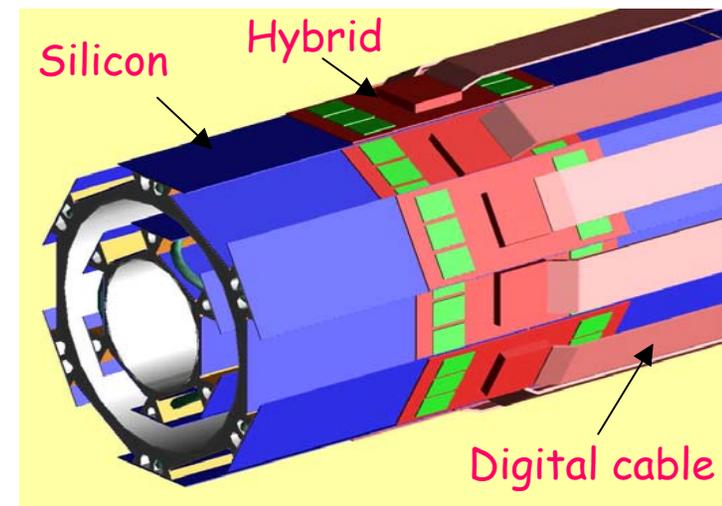
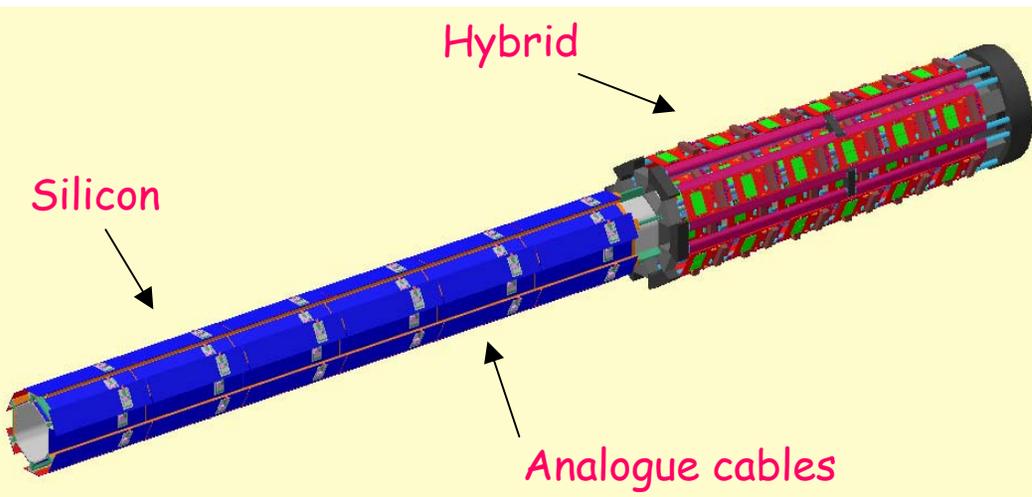
Silicon Detector Elements

- 168 silicon staves: basic building block of outer layers
- Supported in positioning bulkheads at $z=0$, $z=610$ mm



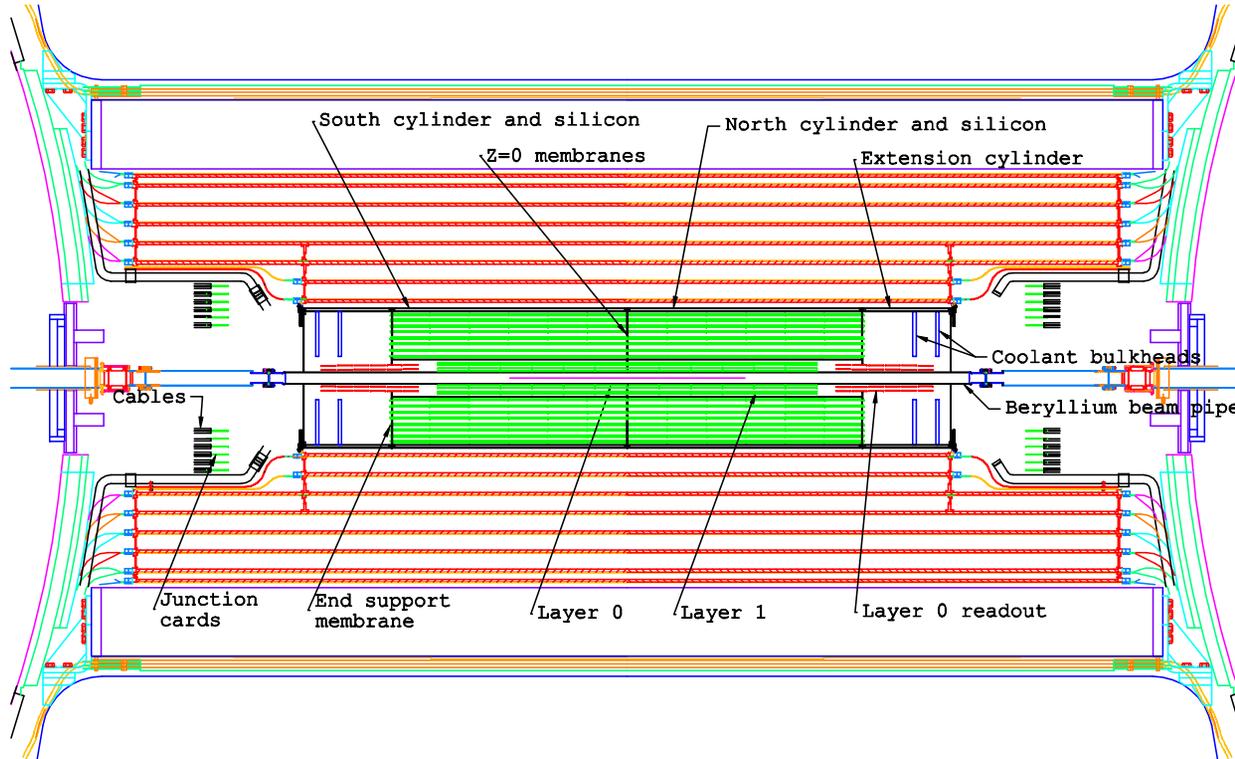
- Layer 0
Support structure: University of Washington

- Layer 0/Layer 1 mated





Plan View of Run IIb Barrel Region



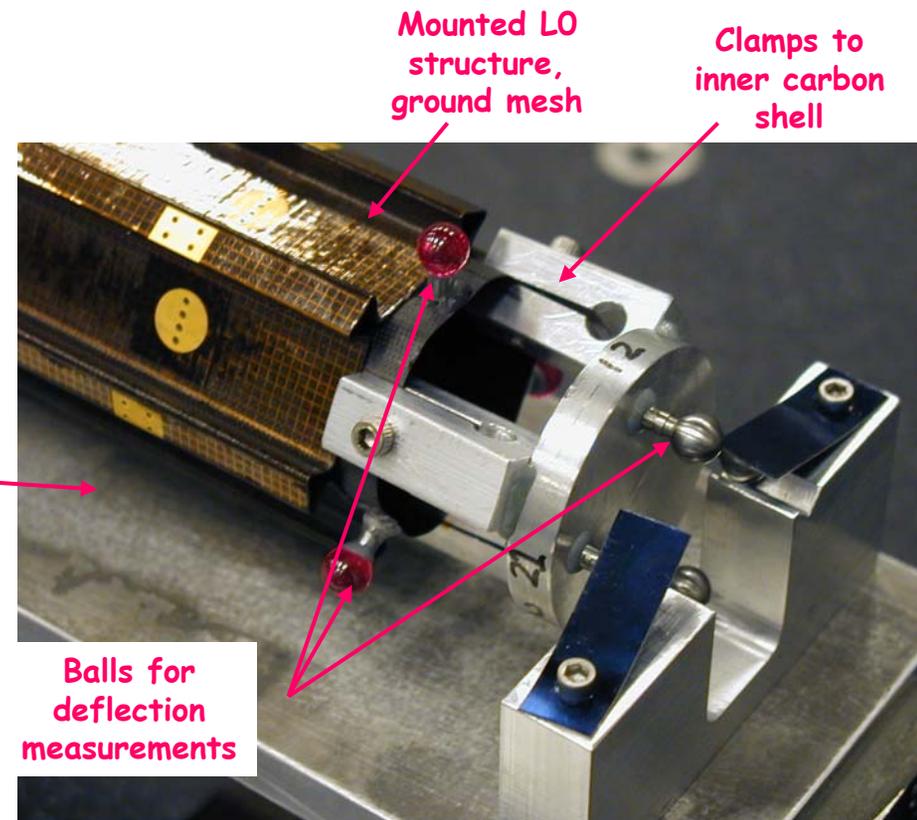
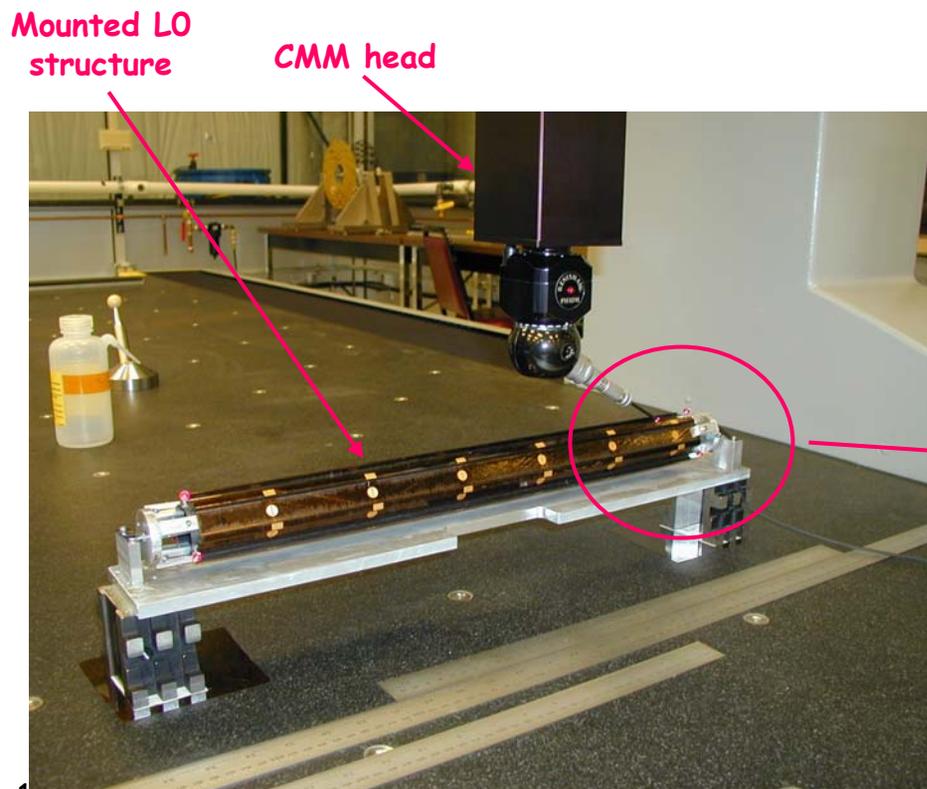
- 18.542 mm IR beam tube
- L0 and L1: 12 sensors long, each 79 mm in length
- L2 - L5: 12 sensors long, each 100 mm in length
- 1220 mm long barrel region
- Support from "bulkheads" at $z = 0$ and $z = \pm 610$ mm



Silicon Layer 0 Support Structure

University of Washington

- First Layer 0 prototype carbon fiber support structure delivered to Fermilab for tests in January
- Integrated grounding - kapton/copper ribbon
- Performs to specification under deflection tests - significant technical achievement





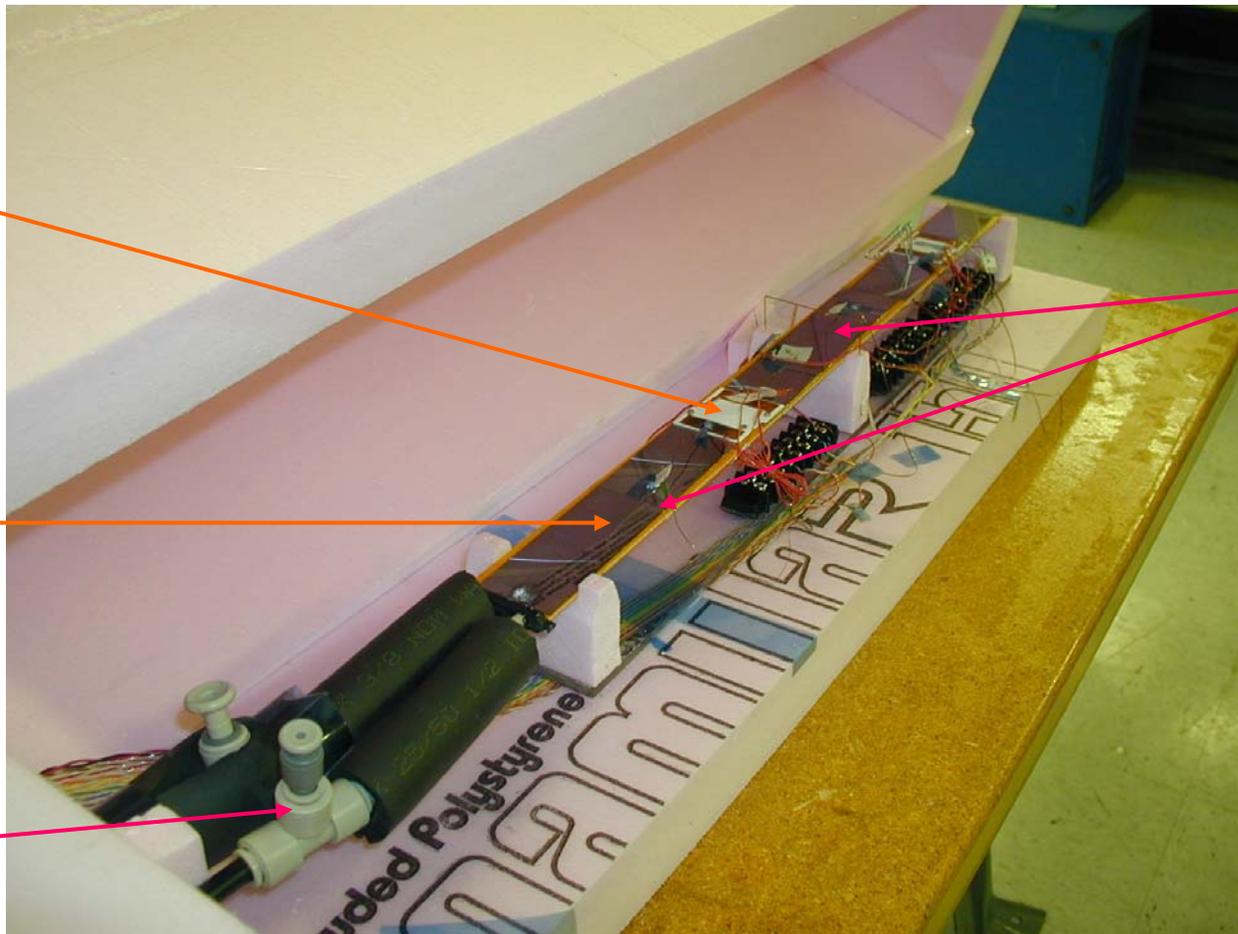
Prototype Mechanical Stave

Prototype mechanical stave being thermally tested at SiDet
Dec 18 '02 integration milestone met

Aluminum-ceramic hybrid (dummy)

Stereo silicon, axial mounted underneath

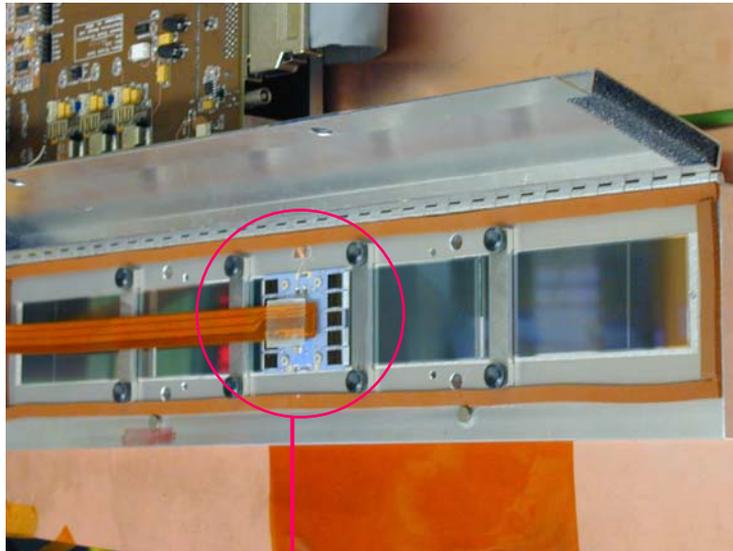
Input cooling channel



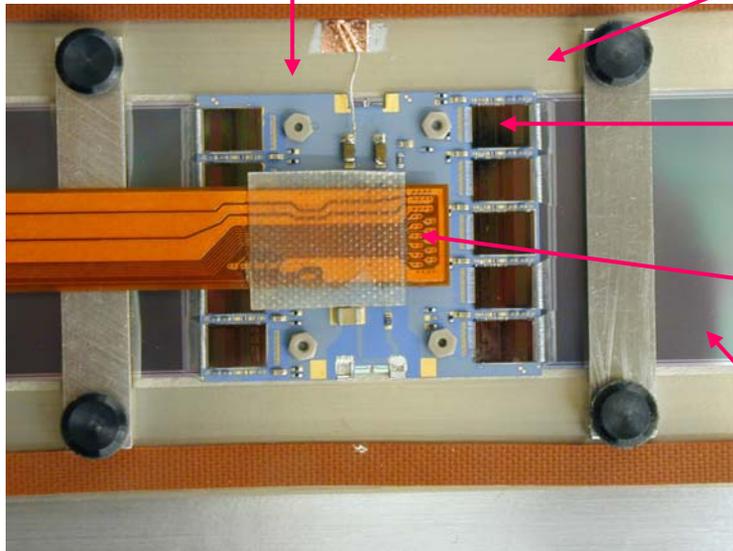
10/10 (upper)
20/20 (lower)
mechanical modules, concatenated



Outer Layer Silicon Module Prototypes



20/20 axial module



20/20 axial hybrid

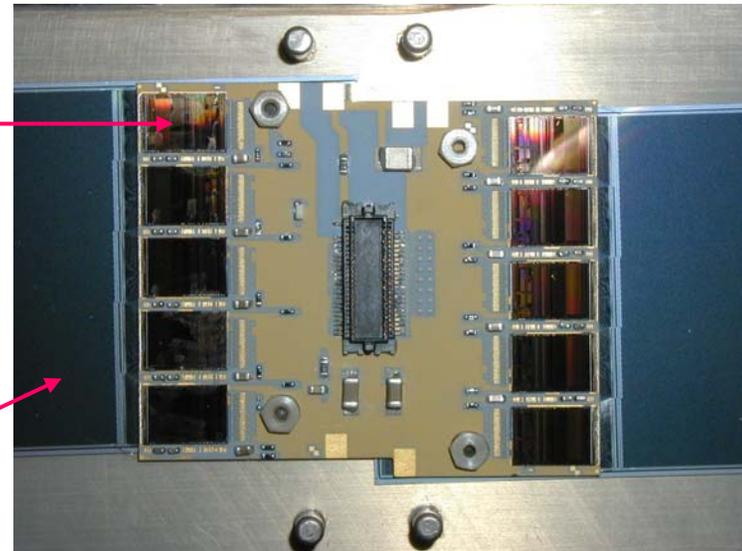
SVX4 readout chip

Digital cable

Silicon sensors

- First outer layer electrical-grade ("20/20") prototypes fabricated
- Two types: axial & stereo readout
- Each are 12 sensors long, ~100 mm in length
- Stereo angle obtained by rotating sensors
- Testing underway

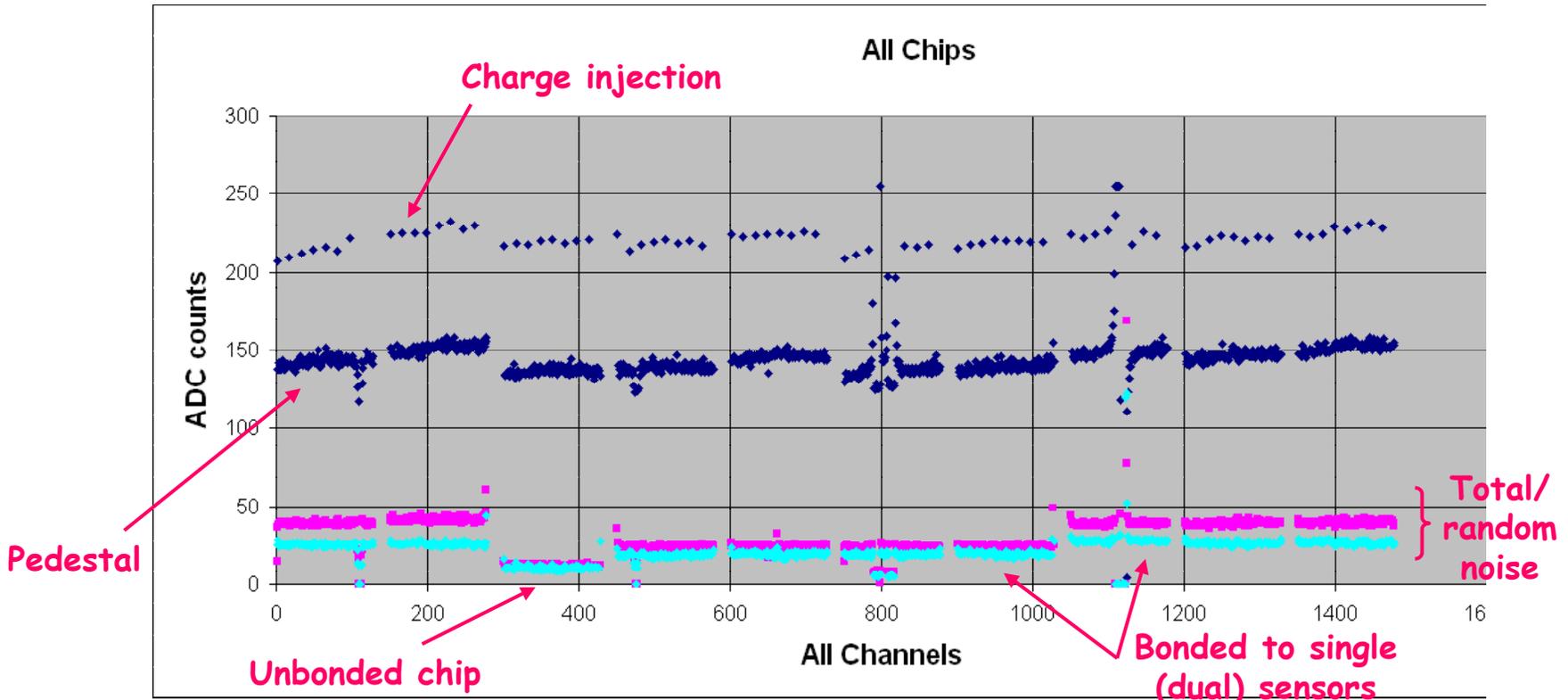
20/20 stereo hybrid





Silicon Prototype Module Test Results

Electrical tests of 20/20 axial module (10 chip readout)



Represents performance milestone that integrates most major outer-module components: SVX4, hybrids, digital cable, wire-bonds, prototype silicon sensors, grounding,...



Silicon Status

Component	Vendor	Design	First Prototype		Second Prototype	
			Ordered	Delivered	Ordered	Delivered
L0 Sensors	ELMA	✓	✓	✓		
	HPK	✓				
L1 Sensors	ELMA	✓	✓	✓		
	HPK	✓	✓	✓		
L2 Sensors	HPK	✓	✓	✓		
Analogue Cable	Dycx	✓	✓	✓	✓ ✓	✓ ✓
L0 Hybrid	Amitr.	✓	✓			
L1 Hybrid	CPT	✓	✓	✓		
L2A Hybrid	CPT	✓	✓	✓		
	Amitr.	✓	✓	✓		
L2S Hybrid	CPT	✓	✓	✓		
Digital Cable	Honey	✓	✓	✓	✓	✓
	Basic	✓	✓	✓	✓	✓
Junction Card		✓	✓	✓		
Twisted Pr. Cable		✓	✓	✓	✓	
Adapter Card		✓	✓	✓		
Purple Card		✓	✓	✓	✓	✓
Test Stand Elctr.		✓	✓	✓		



University Involvement in Silicon Sub-Project

- Mechanical design and fabrication
 - ◆ University of Washington: Layer 0, 1
- Sensor Testing
 - ◆ Kansas State University
 - ◆ Stony Brook
 - ◆ CINVESTAV (Mexico), Moscow State University
- Electronics
 - ◆ Kansas State University
 - ▲ Digital cables, Adapter card, Junction card, Test card
 - ◆ University of Kansas, Fresno University
 - ▲ Hybrid testing
 - ◆ Louisiana Tech
 - ▲ Digital cable testing
- Quality Assurance
 - ◆ University of Illinois (Chicago), Northwestern University
- Monitoring
 - ◆ Radiation monitoring, NIKHEF
 - ◆ Temperature Monitoring, Rice University

Major commitments from many institutions
Recruitment ongoing



WBS 1.2: Trigger Upgrades

Level 1 projects underway

- Level 1 Calorimeter
- Level 1 Cal-track matching
- Level 1 Tracking
- Trigger simulations

Level 2 projects

- Level 2 Beta upgrade & Silicon Track Trigger (STT) upgrade
- Later start in schedule
- VTM's procured for STT (part of larger order)

WBS 1.2: Trigger Upgrade
H. Evans (Columbia), D. Wood (Northeastern)

WBS 1.2.1: Level 1 Calorimeter
M. Abolins (MSU), H. Evans (Columbia),
P. LeDu (Saclay)

WBS 1.2.2: Level 1 Cal-track match
K. Johns (Arizona)

WBS 1.2.3: Level 1 Tracking
M. Narain (Boston)

WBS 1.2.4: Level 2 Beta upgrade
R. Hirosky (Virginia)

WBS 1.2.5: Level 2 STT upgrade
U. Heintz (Boston)

WBS 1.2.6: Trigger Simulation
M. Hildreth (ND), E. Perez (Saclay)



WBS 1.2: Run IIB Trigger Upgrade

System	Problems	Solutions
Cal	1) Trigger on $\Delta\eta \times \Delta\phi = 0.2 \times 0.2$ TTs \Rightarrow slow turn-on curve 2) Slow signal rise \Rightarrow trigger on wrong crossing	<ul style="list-style-type: none"> Clustering Digital Filter
Track	1) Rates sensitive to occupancy 2) Limited match to calorimeter	<ul style="list-style-type: none"> Narrower Track Roads Improve Cal-Track Match
Muon	No Additional Changes Needed!	<ul style="list-style-type: none"> Requires Track Trigger

Trigger	Example Physics Channels	L1 Rate (kHz) (no upgrade)	L1 Rate (kHz) (with upgrade)
EM (1 EM TT > 10 GeV)	$W \rightarrow e\nu$ $WH \rightarrow e\nu jj$	1.3	0.7
Di-EM (1 EM TT > 7 GeV, 2 EM TT > 5 GeV)	$Z \rightarrow ee$ $ZH \rightarrow eejj$	0.5	0.1
Muon (muon $p_T > 11$ GeV + CFT Track)	$W \rightarrow \mu\nu$ $WH \rightarrow \mu\nu jj$	6	0.4
Di-Muons (2 muons $p_T > 3$ GeV + CFT Tracks)	$Z \rightarrow \mu\mu, J/\Psi \rightarrow \mu\mu$ $ZH \rightarrow \mu\mu jj$	0.4	< 0.1
Electron + Jets (1 EM TT > 7 GeV, 2 Had TT > 5 GeV)	$WH \rightarrow e\nu+jets$ $tt \rightarrow e\nu+jets$	0.8	0.2
Muon + Jet (muon $p_T > 3$ GeV, 1 Had TT > 5 GeV)	$WH \rightarrow \mu\nu+jets$ $tt \rightarrow \mu\nu+jets$	< 0.1	< 0.1
Jet+MET (2 TT > 5 GeV, Missing $E_T > 10$ GeV)	$ZH \rightarrow \nu\bar{\nu}b\bar{b}$	2.1	0.8
Muon + EM (muons $p_T > 3$ GeV + CFT track + 1 EM TT > 5 GeV)	$H \rightarrow WW, ZZ$	< 0.1	< 0.1
Single Isolated Track (1 Isolated CFT track, $p_T > 10$ GeV)	$H \rightarrow \tau\tau, W \rightarrow \mu\nu$	17	1.0
Di-Track (1 isolated tracks $p_T > 10$ GeV, 2 tracks $p_T > 5$ GeV, 1 matched with EM energy)	$H \rightarrow \tau\tau$	0.6	< 0.1

Level 1 systems

Core Run IIB trigger menu, simulated at 2E32, 396 ns

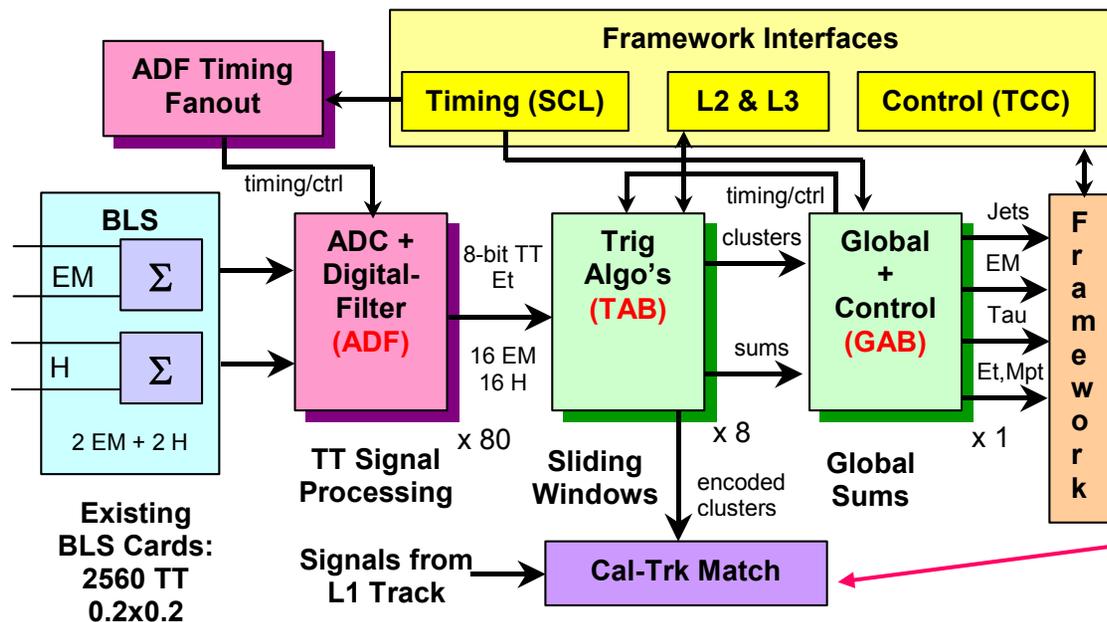


Total output rate with (without) L1 trigger upgrade = 3.2 (~30) kHz
Available L1 bandwidth budget: 5 kHz



WBS 1.2.1: Calorimeter Trigger Upgrade

- **Saclay**
 - ◆ ADC+Digital Filter (ADF)
 - ◆ ADF timing distribution board
 - ◆ Analog splitter (for in-situ tests)
 - ◆ ADF Crate/backplane
- **Nevis**
 - ◆ Trigger algorithm board (TAB)
 - ◆ Global Algorithm Board (GAB)
 - ◆ Crates for TAB/GAB
 - ◆ Test system for ADF-to-GAB cables
- **Michigan State**
 - ◆ Interfacing to existing system, framework
 - ◆ Infrastructure



L1 Cal/Track Match:
University of Arizona



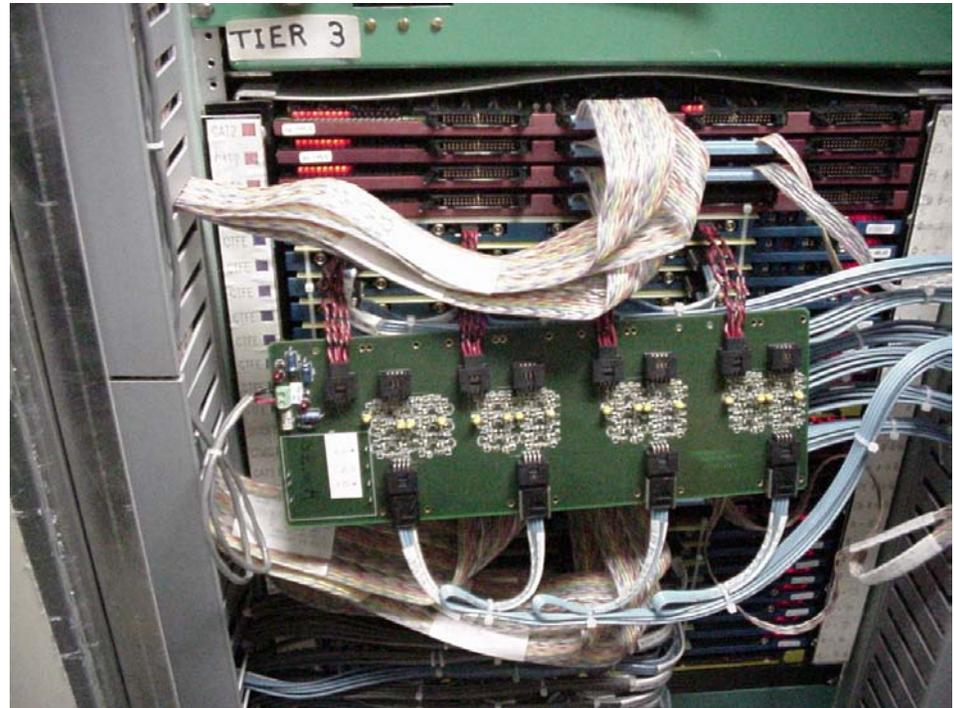
Level 1 Trigger Highlights

- Prototype design phase concluded in January for three major boards in Level 1 trigger upgrade:
 - ◆ Level 1 Calorimeter Trigger
 - ▲ ADC-Digital Filter Board (ADF) - Saclay
 - ▲ Trigger Algorithm Board (TAB) - Columbia University
 - ◆ Level 1 Calorimeter/Track Match
 - ▲ Flavor Board (MTFB)
 - ◆ Layouts begun
- Analog splitter installed during January shutdown in Level 1 Cal rack at DZero Assembly Building, Movable Counting House
 - ◆ Picks off in-situ signals from four trigger towers
 - ◆ Data will be taken, analyzed during next few months
 - ◆ Preparation for tests of full L1 Cal prototype chain (ADF, TAB, GAB), beginning this summer



Analog Splitter: Saclay & MSU

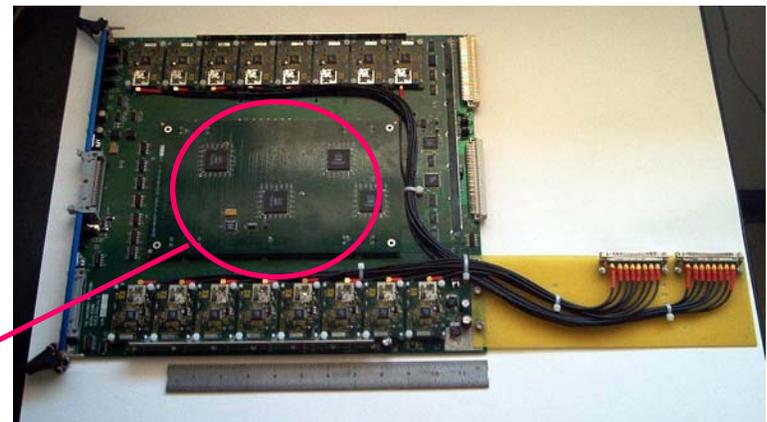
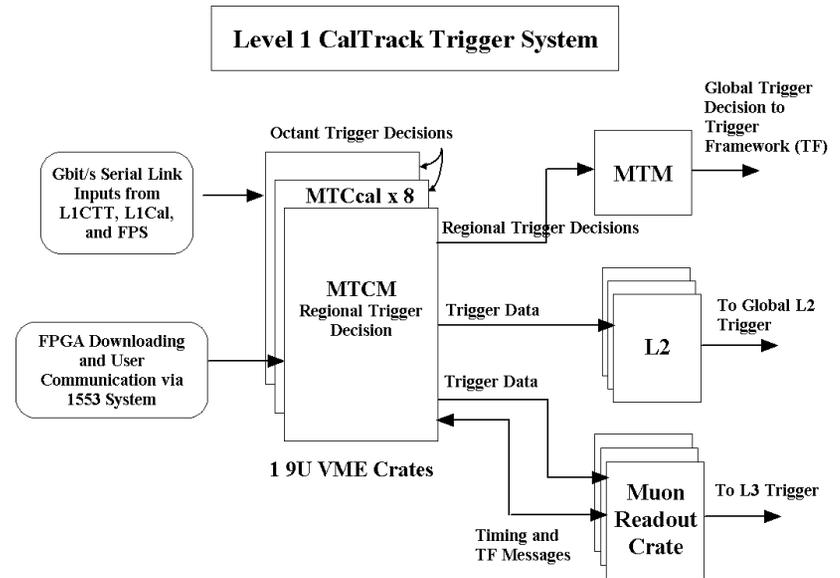
- Analog splitter: allows in-situ test of digital filtering with real signals
 - ◆ Designed and tested at Saclay
 - ◆ Shipped to MSU Dec 20th: tested there
 - ◆ Installed in DØ L1Cal trigger (Run IIa) during current shutdown
 - ◆ Noise tests in progress
 - ◆ Tests with beam (w/ splitter vs. w/o splitter) to follow





WBS 1.2.2: Cal-Trk Match: Arizona

- Uses "L1mu" electronics, apart from specialized daughter "flavor board"
- Flavor board (MTFB) prototype design >90% complete
- Some procurements anticipated for next month
- Approval was essential for keeping this on track



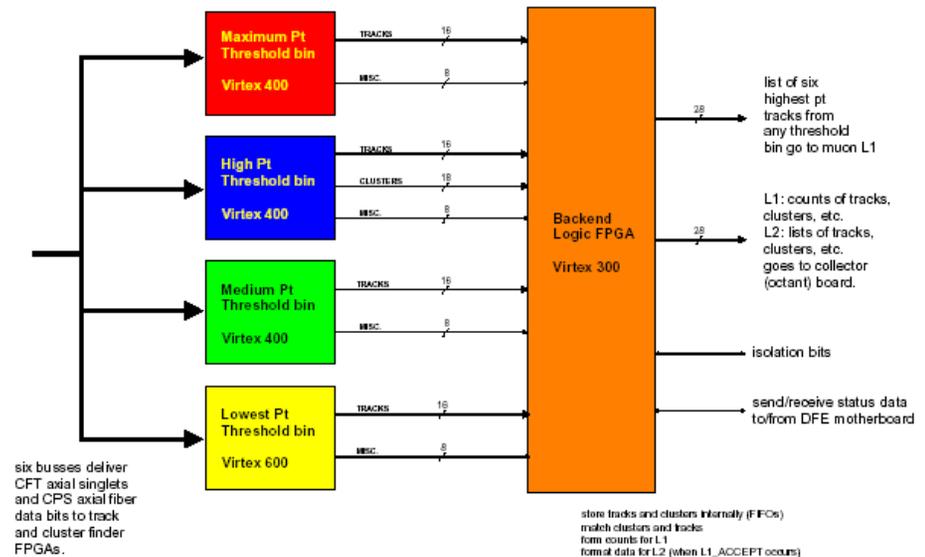
Run IIa MTFB
(scint flavor)



WBS 1.2.3: L1 CTT: Boston Univ.

- Firmware design for target algorithm began in November
- "Front end" and "back end" code from Run IIa rewritten - latency reduced
- Ongoing work on maps of single fibers

CFT/CPS AXIAL Trigger Daughter Board Dataflow





WBS 1.2.4, 1.2.5: Run IIB Level 2 Trigger Upgrade

- Modest upgrades to two components:

- ◆ Silicon Track Trigger

- ▲ Vital for triggering on b-quarks

- $ZH \rightarrow \nu\nu bb$
- $Z \rightarrow bb$ (top mass jet energy scale)

- ▲ Improves track trigger

- Sharper p_T turn-on
- Reduced fake rate

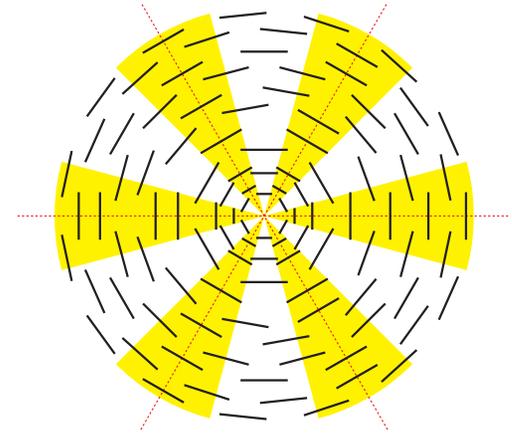
- ▲ Upgrade needed to accommodate design of new silicon detector

- Instrumenting 5 of 6 Run IIB silicon layers
 - See report submitted to June PAC

- ◆ Level 2β processors

- ▲ More processing power required to retain same Level 2 rejection

- ▲ Add 12 additional processors



Trigger upgrades centered at collaborating universities & laboratories, US and foreign



Trigger Upgrade Project Institutions

Sub-project	Institution(s)
Calorimeter: ADF	Saclay, MSU
Calorimeter: TAB	Columbia
Track trigger	Boston U., FNAL
Cal-Track match	U. of Arizona
Simulation & algorithms	Notre Dame, Saclay, Kansas, Manchester, Brown
Online software & integration	MSU, Northeastern, FSU, Langston
Level 2 β	Orsay, Virginia, MSU
STT upgrade	Boston, Columbia, Stony Brook, FSU

- Strong, active institutions
- Largely University-driven
- Combination of RunIIa experience and new ideas
- Engineering, technical and physicist manpower identified for delivering upgraded trigger
- Other institutions expressing interest



WBS 1.3: DAQ/Online

System	Items	Need
Level 3 filter nodes	96 more L3 Farm nodes	Match to rates and processing requirements
DAQ HOST system	Linux data logging nodes and buffer disk arrays	Replace existing systems with higher performance nodes
ORACLE systems	Database nodes, disk arrays, and backup systems	Adopt lab standard ORACLE platform
File Server systems	Linux server nodes, disk arrays, and backup systems	Provide increased storage capacity
Slow Control system	VME processors for control and monitoring of detector	Improve monitoring performance for extended run

Upgrades to DAQ/Online systems required for long-term, high rate running during Run IIb

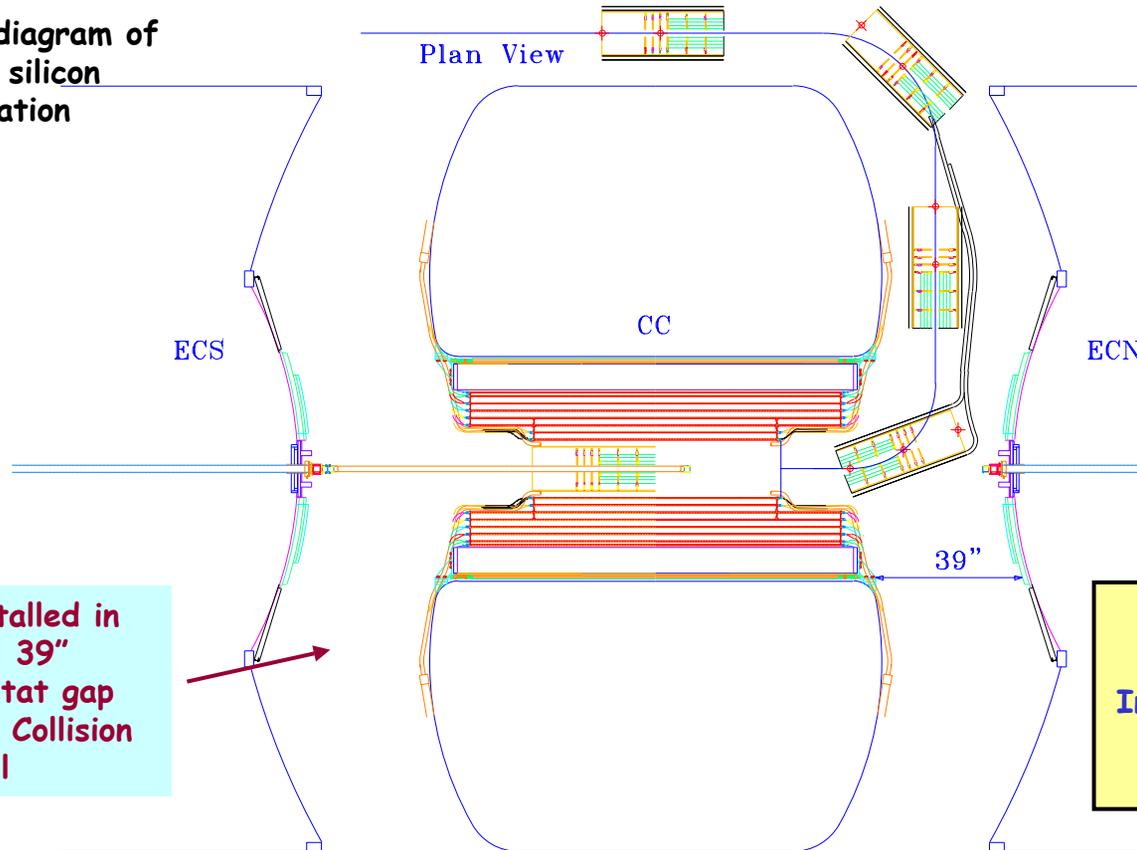
Developed, implemented by in-house Fermilab group(s)



WBS 1.5: Installation

Installation sub-project contains integrated plan for silicon, trigger installation and commissioning
Activity in Collision Hall dominated by silicon installation, hookup
Split-silicon design allows installation in Collision Hall
Detector platform not rolled out - much reduces time, effort, risk

Conceptual diagram of Run IIa silicon installation



Silicon installed in nominal 39" intercryostat gap available in Collision Hall

Ready for Beam:
Oct 25, 2006
 Includes pre-beam commissioning of silicon, trigger
 Shutdown duration: 7 months



Subset of Project Manager's Milestones for Silicon Subproject

ID	Milestone	2002				2003				2004				
		Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
985	Release Of Silicon Reconstruction Code	★	9/12											
446	Successful Readout of Hybrid With SASEQ Test Stand					★	8/1							
15	Sensor Probing Equipment Setup And Certification Complete									◆	11/14			
437	Successful Readout Of More Than 1 Silicon Hybrid									◆	12/5			
563	Silicon Prototype Mechanical Stave Built									◆	1/6			
33	Choose L0 Silicon Sensor Technology									◆	2/20			
69	Choose L1 Silicon Sensor Technology									◆	2/20			
91	L2-L5 Silicon Sensors Released For Production									◆	3/24			
262	Silicon L2-L5 Digital Jumper Cables Released For Production									◆	4/29			
38	L0 Silicon Sensors Released For Production									◆	5/13			
70	L1 Silicon Sensors Released For Production									◆	5/13			
399	Silicon High-mass Cables Ready									◆	5/29			
994	Release Silicon Unpacking And Translation Packages									◆	6/2			
999	Release Silicon Examine Package									◆	7/11			
844	Silicon Cylinders Released for Production									◆	7/21			
451	Successful Readout Of Silicon Single-unit Full-chain									◆	7/25			
1004	Release Silicon Event Display Package									◆	9/11			
237	Silicon L0 Flex Cables Released For Production									◆	9/12			
677	Begin 20cm Gang Production									◆	9/17			
798	Successful Fabrication of an Electrical-grade Pre-production Silicon Stave									◆	10/10			
138	SVX4 Released For Production									◆	10/20			
41	1st L0 Silicon Sensor Delivered									◆	10/24			
71	1st L1 Silicon Sensor Delivered									◆	10/24			
97	25% L2-L5 Silicon Sensors Delivered And Tested									◆	11/18			
194	Silicon L1 Hybrids Released For Production									◆	11/20			
358	Silicon SASEQ Test Stands Ready									◆	11/20			
225	Silicon L2-L5 Hybrids Released For Production									◆	12/10			

Milestones tightly span the time frame;
allow for close managerial oversight



GANTT Chart of Director/DOE Level 2 PM's Milestones for All Subprojects

ID	Task Name	2003				2004				2005				2006				2007
		Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1
1	Silicon																	
2	Silicon Prototype Mechanical Stave Built		■ 1/6															
3	L2-L5 Silicon Sensors Released For Production			■ 3/24														
4	SVX4 Released For Production					■ 10/20												
5	Successful Readout Of Full Silicon Stave						■ 1/29											
6	Silicon Module Production Begun							■ 5/17										
7	All Silicon Sensors Delivered And Tested									■ 12/9								
8	All SVX4 Chips Produced And Tested									■ 12/21								
9	All Silicon Hybrids Produced And Tested										■ 3/3							
10	Silicon Stave Production Begun										■ 3/8							
11	Silicon Module Production And Testing Complete														■ 7/22			
12	Downstream Silicon Readout Ready for Installation On Platform														■ 10/25			
13	Silicon Stave Production Complete														■ 12/22			
14	South Silicon Complete														■ 2/10			
15	North Silicon Complete															■ 5/4		
16	Silicon Ready To Move To DAB															■ 5/25		
17	Trigger																	
18	L1 Trigger Cal-Trk Match Production and Testing Completed										■ 9/23							
19	L2 Silicon Track Trigger Production and Testing Complete														■ 10/17			
20	L1 Calorimeter Trigger Production And Testing Complete														■ 1/5			
21	L2 Beta Trigger Production And Testing Complete														■ 1/5			
22	L2 Trigger Upgrade Production and Testing Complete														■ 1/5			
23	L1 Central Track Trigger Production And Testing Complete														■ 1/10			
24	L1 Trigger Upgrade Production and Testing Complete														■ 1/10			
25	Online																	
26	Online System Production and Testing Complete														■ 10/7			



DOE Level 1 Milestones

Milestone	DOE Level 1 Milestone Date
All silicon sensors delivered and tested	12/09/04
Online System Production and Testing Complete	10/07/05
Silicon stave production complete	12/22/05
Level 2 Trigger Production and Testing Complete	01/05/06
Level 1 Trigger Production and Testing Complete	01/10/06
Silicon ready to move to D0 Assembly Building	05/25/06
CD-4: DOE Approval of Project Closeout	11/06

Shutdown begins March 30 '06
Ready for beam October 25 '06



Silicon Milestones - One Year Window

Run IIb Silicon Milestones (1 Year Window 11/02-10/03)			2004																		
ID	Name	Forecast	Baseline	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec	Jan	Feb	Mar	
136	First Chip Ready For Hybrid	7/8/02	7/8/02																		
446	Successful Readout of Hybrid With SASEQ Test Stand	8/1/02	8/1/02																		
437	Successful Readout Of More Than 1 Silicon Hybrid	11/22/02	12/5/02	★																	
15	Sensor Probing Equipment Setup And Certification Complete	12/6/02	11/14/02	★																	
565	Silicon Prototype Mechanical Stave Built	12/18/02	1/6/03	★																	
33	Choose L0 Silicon Sensor Technology	1/31/03	2/20/03																		
69	Choose L1 Silicon Sensor Technology	1/31/03	2/20/03																		
91	L2-L5 Silicon Sensors Released For Production	2/18/03	3/24/03																		
262	Silicon L2-L5 Digital Jumper Cables Released For Production	3/6/03	4/29/03																		
38	L0 Silicon Sensors Released For Production	4/11/03	5/13/03																		
70	L1 Silicon Sensors Released For Production	4/11/03	5/13/03																		
399	Silicon High-mass Cables Ready	5/8/03	5/29/03																		
846	Silicon Cylinders Released For Production	6/6/03	7/21/03																		
237	Silicon L0 Flex Cables Released For Production	7/2/03	9/12/03																		
996	Release Silicon Unpacking And Translation Packages	7/23/03	6/2/03																		
800	Successful Fabrication of an Electrical-grade Pre-production Silicon Stave	7/24/03	10/10/03																		
138	SVX4 Released For Production	8/19/03	10/20/03																		
679	Begin 20cm Gang Production	8/20/03	9/17/03																		
1006	Release Silicon Event Display Package	8/25/03	9/11/03																		
41	1st L0 Silicon Sensor Delivered	9/3/03	10/24/03																		
71	1st L1 Silicon Sensor Delivered	9/3/03	10/24/03																		
1001	Release Silicon Examine Package	9/4/03	7/11/03																		
194	Silicon L1 Hybrids Released For Production	9/17/03	11/20/03																		
358	Silicon SASEQ Test Stands Ready	9/17/03	11/20/03																		
451	Successful Readout Of Silicon Single-unit Full-chain	9/18/03	7/25/03																		
97	25% L2-L5 Silicon Sensors Delivered And Tested	9/19/03	11/18/03																		
147	Silicon L0 Hybrids Released For Production	10/10/03	1/5/04																		
225	Silicon L2-L5 Hybrids Released For Production	10/13/03	12/10/03																		
439	Successful Readout Of Full Silicon Stave	10/17/03	1/29/04																		
587	Stave Shells For South Silicon Complete	10/17/03	1/30/04																		
250	Silicon L0-L1 Digital Jumper Cables Released For Production	10/24/03	1/22/04																		
137	SVX4 Wafers Delivered	10/29/03	2/5/04																		

Solid Diamonds: Baseline
Open Diamonds: Current Forecast

Insufficient software personnel, has been addressed

Project: Run IIb Silicon Schedule
 Status Date: 12/31/02
 Print Date: 1/24/03

Current Forecast ◇ Baseline Milestone ◆ Completed Milestone ★

Current forecast remains ahead of baseline dates



US National Science Foundation MRIs for Run IIb

- Silicon MRI submitted Feb '01, awarded July '01
 - ◆ Brown, California State (Fresno), U Illinois (Chicago), Kansas, Kansas State, Michigan State, Stony Brook, Washington, (Moscow State, CINVESTAV)
 - ▲ Principal Investigator: A. Bean
 - ▲ Co-PIs: R. Demina, C. Gerber, R. Partridge, G. Watts
 - ◆ \$1.7M + \$0.7M matching = \$2.4M total
- Level 1 Trigger MRI submitted Jan '02, partial award granted July '02
 - ◆ Arizona, Boston, Columbia, Florida State, Langston, Michigan State, Northeastern, Notre Dame, (Saclay)
 - ▲ Principal Investigator: M. Narain
 - ▲ Co-PIs: H. Evans, U. Heintz, M. Hildreth, D. Wood
 - ◆ \$456k + \$113k matching = \$569k total
 - ◆ Funds will go toward Central Track Trigger upgrade
 - ◆ Considering submission of Silicon Track Trigger, Level 1 Calorimeter during next review cycle
- DO universities playing major role throughout Run IIb Project



Total Project Cost in AY k\$

Includes G&A, contingency, & escalation

AY k\$	Base	Cont %	Cont	Total
Silicon	15986	31	4904	20890
Trigger	3276	37	1216	4492
Online	1062	31	332	1393
Administrative	1463	25	366	1829
TOTAL PROJECT COST	21787	31	6818	28604

Cost by subsystem

AY k\$	M&S +				Cost+				Total					
	R&D		Cont		Cont		M&S +		Labor		Cont		Total	
	Cost	G&A	%	Cont	Total	R&D	FNAL	G&A	%	Cont	Total	Labor	Total	
Silicon	8589	1082	32	3084	11673	12755	4910	1405	29	1820	6730	8135	20890	
Trigger	2877	223	37	1151	4028	4251	137	39	37	65	202	241	4492	
Online	652	116	29	223	874	990	229	66	37	109	338	404	1393	
Administrative	126	22.3	25	37	163	185	1022	293	25	329	1351	1644	1829	
TOTAL PROJECT COST	12243	1442	33	4495	16738	18180	6298	1803	29	2323	8621	10424	28604	

Cost broken out into M&S + R&D, FNAL labor

Fermilab escalation, G&A rates applied

FNAL ESCALATION RATES		FY01	FY02	FY03	FY04	FY05	FY06
EQUIPMENT	BY YEAR	-2.9%	N/A	2.3%	2.8%	2.7%	2.6%
	CUMULATIVE	0.971	1	1.023	1.052	1.080	1.108
LABOR	BY YEAR	-4.0%	N/A	4.0%	4.0%	4.0%	4.0%
	CUMULATIVE	0.960	1	1.040	1.082	1.125	1.170

	EQUIPMENT	LABOR
G&A	17.72%	28.62%

Total Project Cost = \$28,604k
Includes total contingency of 31% (\$6,818k)



Funding Need in AY k\$

Includes G&A, contingency, & escalation

TPC, Obligation Profile In AY k\$	FY01	FY02	FY03	FY04	FY05	FY06	TOTAL
Silicon (incl. Cont + G&A)	17	1326	4860	7165	3443	230	17040
Trigger (incl. Cont + G&A)	0	468	1363	946	1630	56	4462
Online (incl. Cont + G&A)	0	0	84	407	499	404	1393
Administration (incl. Cont + G&A)	0	0	343	499	516	471	1829
Total (excl. R&D)	17	1794	6650	9016	6088	1160	24724
R&D (incl. Cont + G&A)	0	1360	2519	0	0	0	3880
Total Project Cost	17	3154	9169	9016	6088	1160	28604
DOE M&S	0	0	4025	4160	2507	367	11060
DOE SWF	0	0	1045	2999	2325	617	6986
DOE G&A	0	0	631	1038	730	176	2575
TOTAL DOE EQ	0	0	5701	8197	5563	1160	20621
DOE M&S R&D	0	649	926	0	0	0	1575
DOE SWF R&D	0	464	1171	0	0	0	1635
DOE G&A R&D	0	248	422	0	0	0	670
TOTAL DOE R&D	0	1360	2519	0	0	0	3880
In Kind - Foreign	0	258	201	90	49	0	599
In Kind - MRI silicon	17	1326	495	631	0	0	2469
In Kind - MRI trigger	0	0	112	57	430	0	599
In Kind - US base	0	210	141	39	47	0	437
Total In-Kind contributions	17	1794	948	819	526	0	4104
Forward Funding			0			0	
Total Project Cost	17	3154	9169	9016	6088	1160	28604

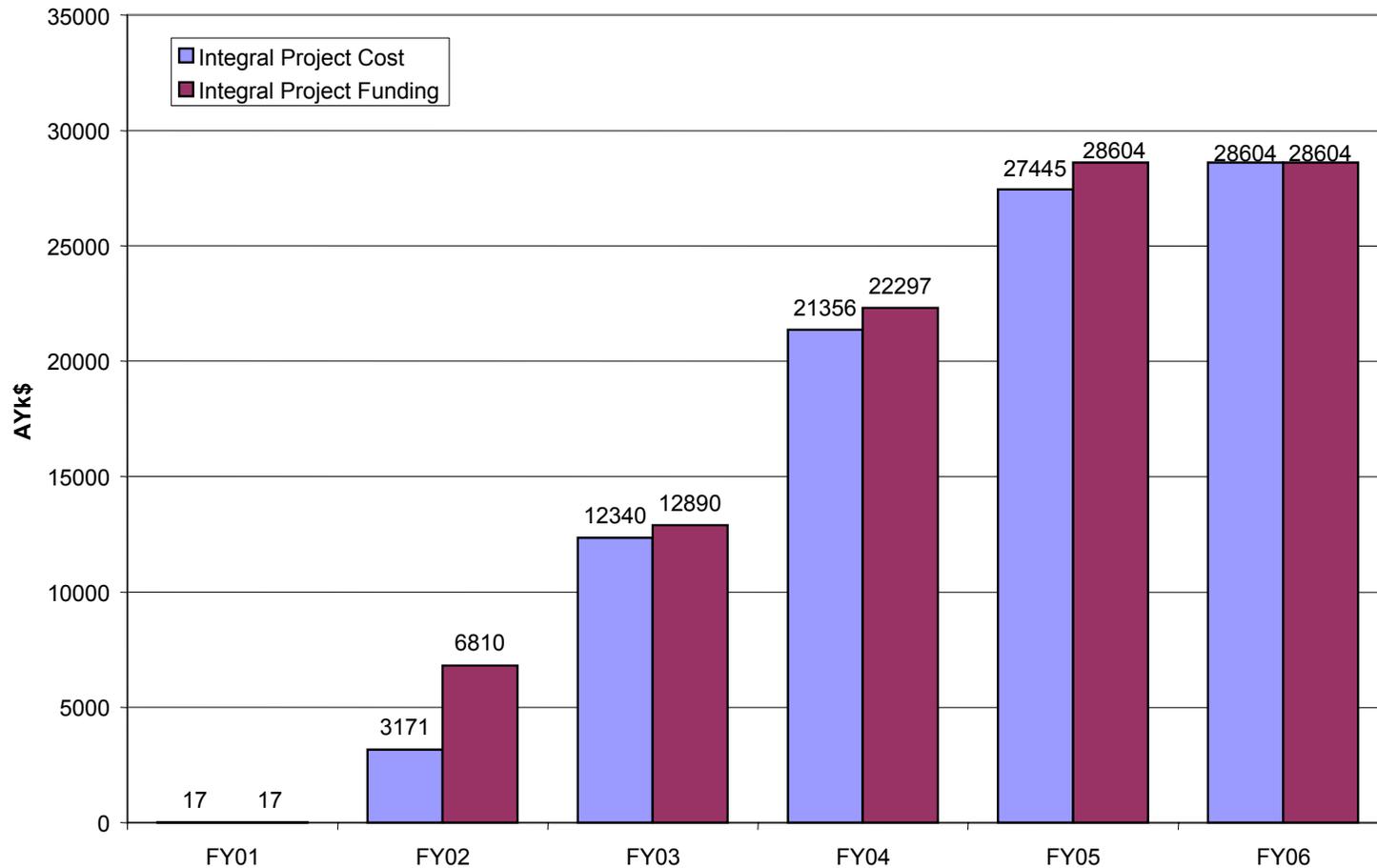
Funding need broken out by source

Contingency on DOE Equipment Portion = 46%



Integral Project Cost & Funding

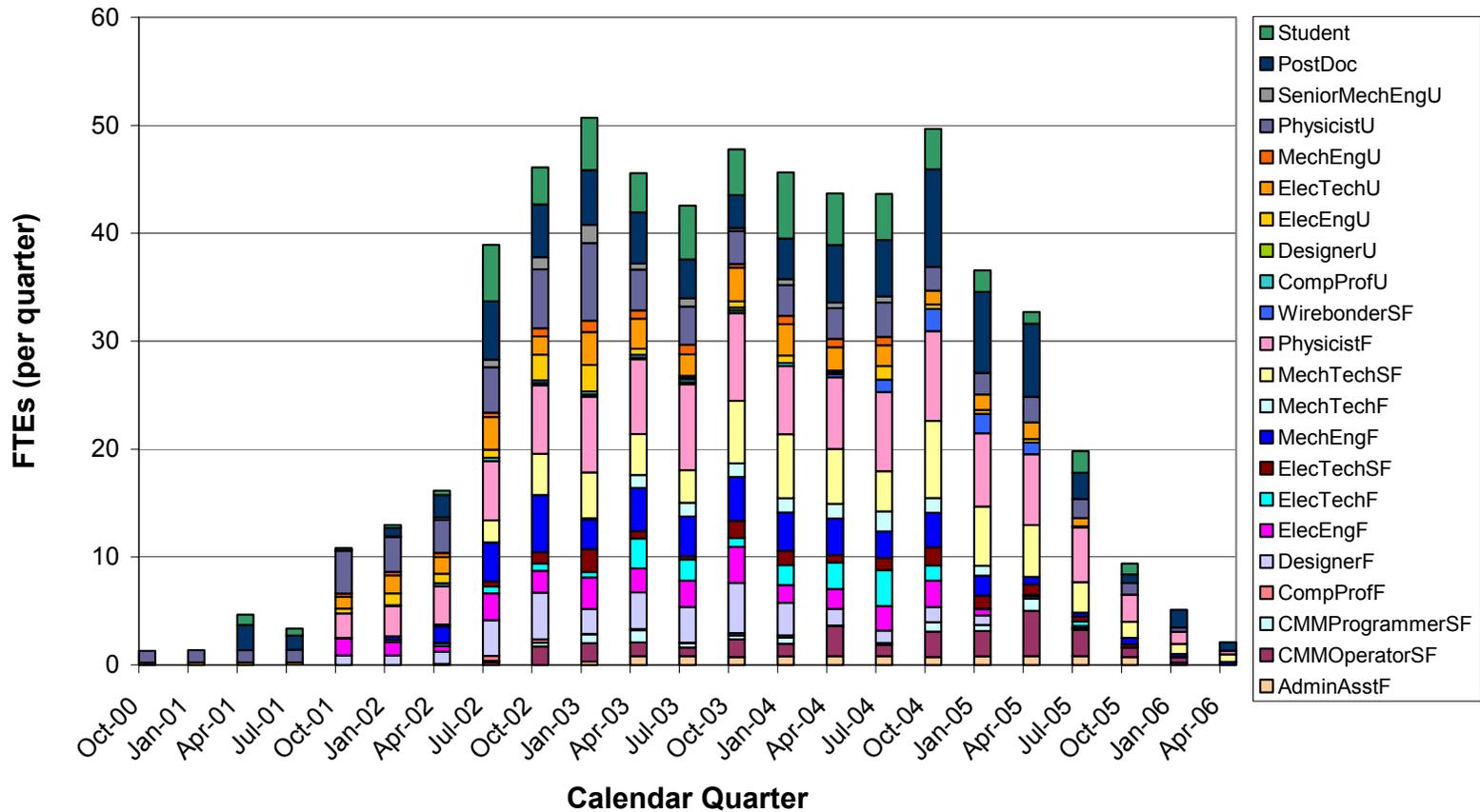
D0 Run IIb Project
Integral Cost & Funding





Total Silicon Labor

Silicon Labor



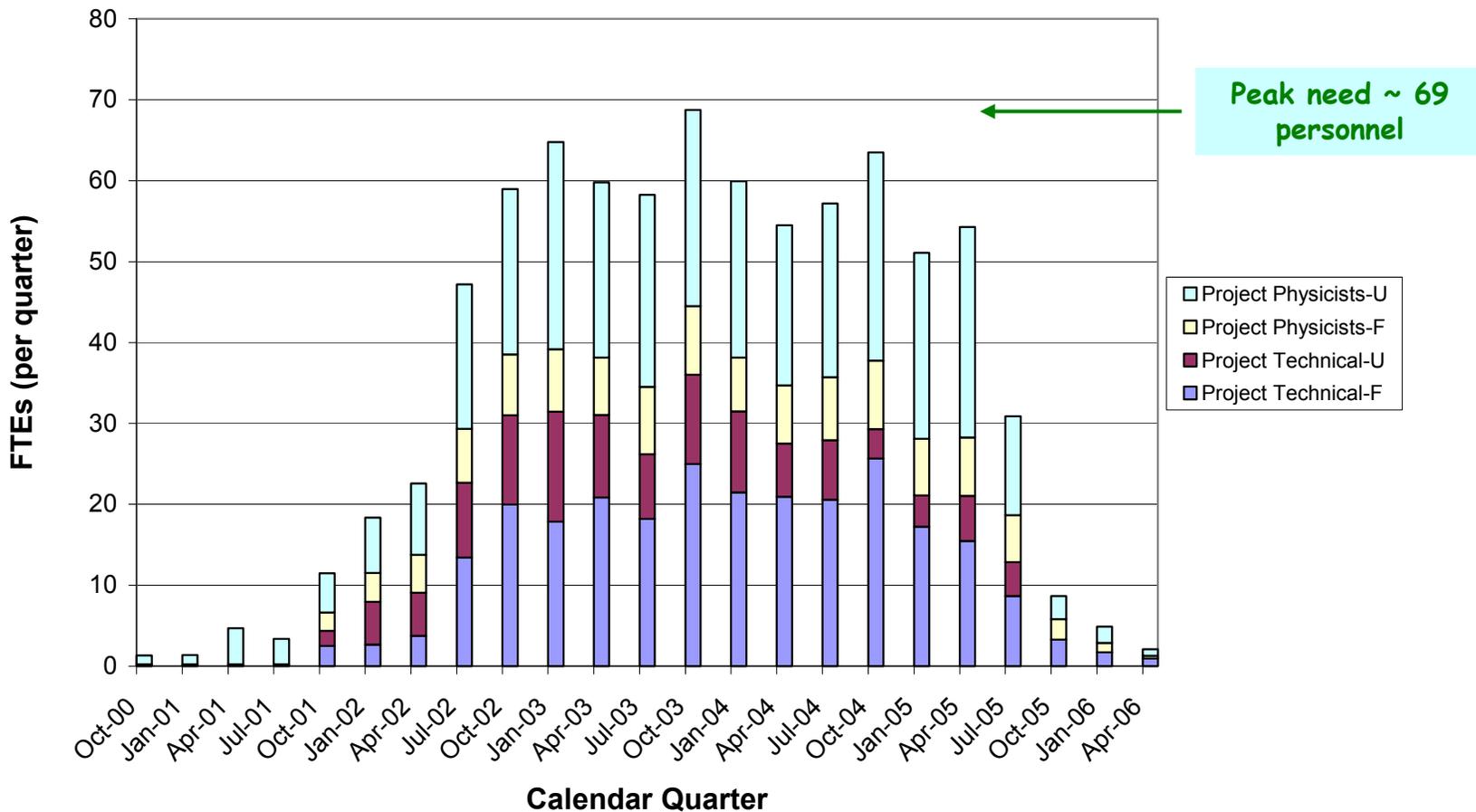
Includes all personnel, all categories - physicists, technical, and administrative - required to deliver silicon detector

Base need only - contingency not included



Total Project Labor

Project Labor



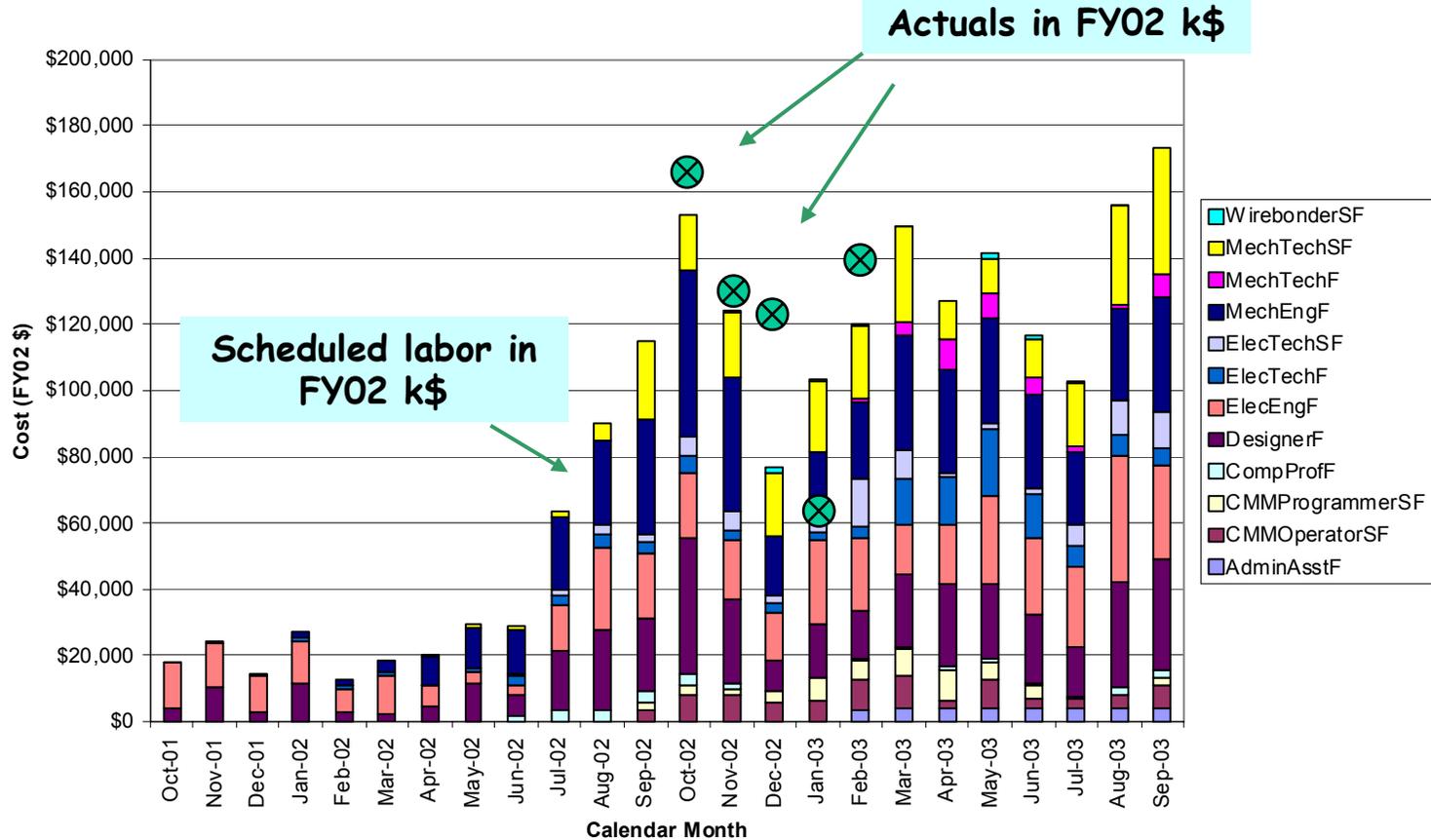
Total required to deliver silicon and trigger+online projects, divided into Fermilab and university components



Labor Cost Extracted from Schedule vs. Actuals (R&D)

Through Feb '03

FNAL Technical Labor
All Funding Sources
FY02 & FY03



Actual labor costs track those in schedule



Large Near-Term Procurements

Silicon Procurements Over \$100k

Item	Cost (FY02 k\$)	Production Start Date
SVX4 2 nd Prototype Chip	158	02/27/03
L2-L5 Sensors	1,453	03/24/03
L2-L5 Digital Jumper Cables	263	04/30/03
L0 Sensors	161	5/14/03
L1 Sensors	155	5/14/03
Analog Cables	167	9/15/03
SVX4 Production Chips	475	10/21/03
L2-L5 Production Hybrids	382	12/11/03
Twisted Pair Cables	256	12/7/04

Req signed, await final simulation cross checks

Req in process, anticipate meeting milestone date

Trigger, DAQ/Online sub-projects contain no procurements over \$100k in FY03

Total silicon procurements in FY03: \$3.1M



Conclusions

- Run IIb upgrade has developed into technically mature project, with a well-based, thoroughly vetted project plan.
- Prototyping continues at rapid pace, has been extremely successful. Will greatly facilitate smooth transition to production.
- Obtaining approval for equipment spending in FY03 was essential to remaining on track. Funding must continue unabated in FY04 and beyond if schedule is to be met.
- Project team, and collaboration as a whole, remain committed to successful, timely project completion and unique physics program to follow.