DØ Run IIb Upgrade Status

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for the DØ Run IIb Upgrade Project

DOE Annual Revew
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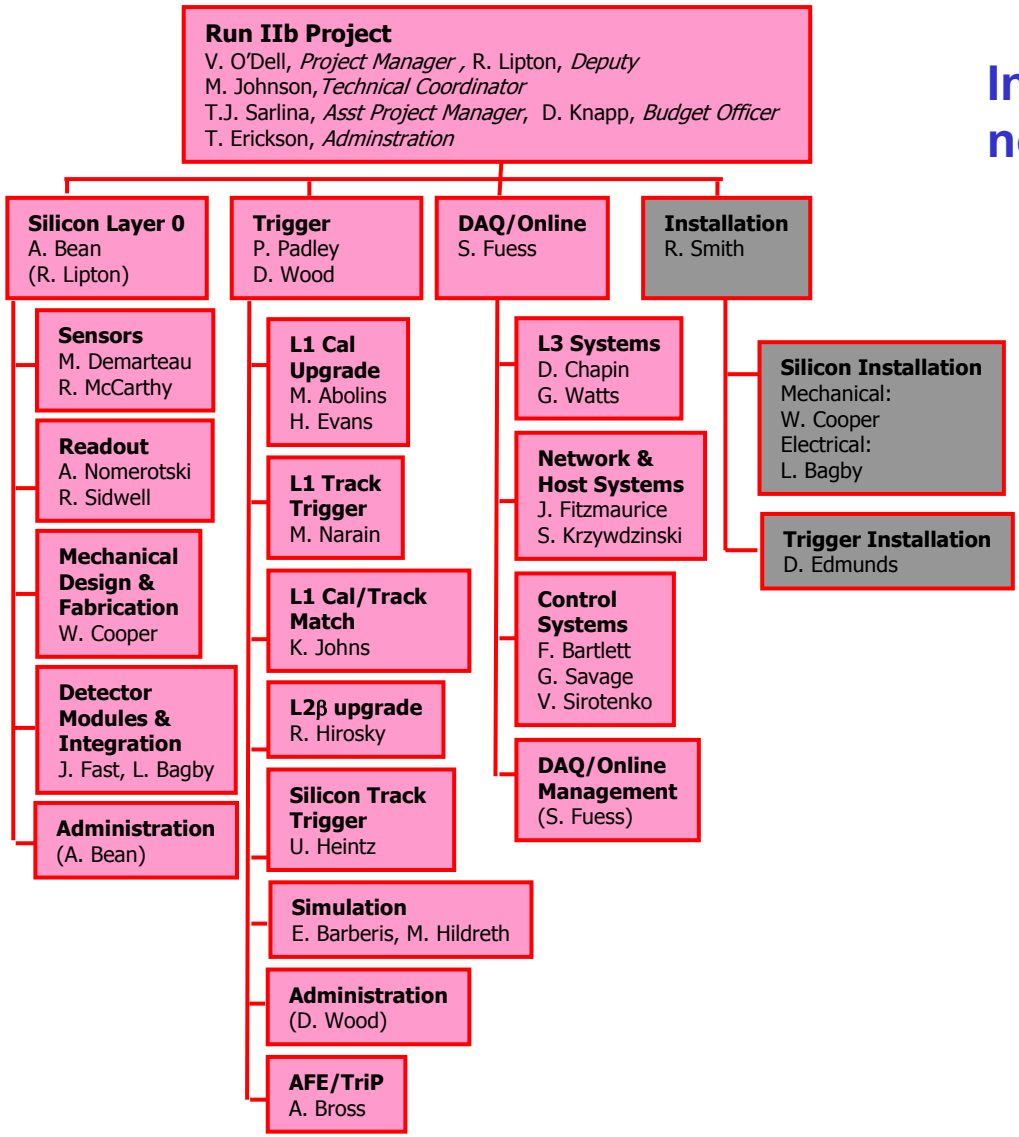
Run IIb Upgrade Project

- Project Status Overview
- Technical progress
  - Silicon Layer Ø detector
  - Trigger/DAQ
- Installation/Commissioning plans
- Cost & Schedule
- Summary

Run IIb upgrade

- Project consists of:
  - New Silicon Layer Zero detector
    - inner layer of silicon
      - Mitigate tracking losses due to radiation damage and detector failure
      - Provide more robust tracking and pattern recognition for higher luminosities
      - Improve impact parameter resolution
  - Trigger Upgrade
    - Complete upgrade program to keep trigger rates down as luminosity increases
      - L1 upgrades (Calorimeter, Central Track Trigger, Cal Trk-Match)
      - L2 upgrades (Silicon Track Trigger, L2 β processors)
    - Additional readout electronics R&D continues
      - New electronics for central fiber tracker
      - Helps tracking efficiency in higher luminosity/occupancy environment
      - Final decision to be made after first full prototype tested - ~7/04
  - DAQ/Online upgrade
    - Upgrade level 3 processing power, database & host servers, control systems

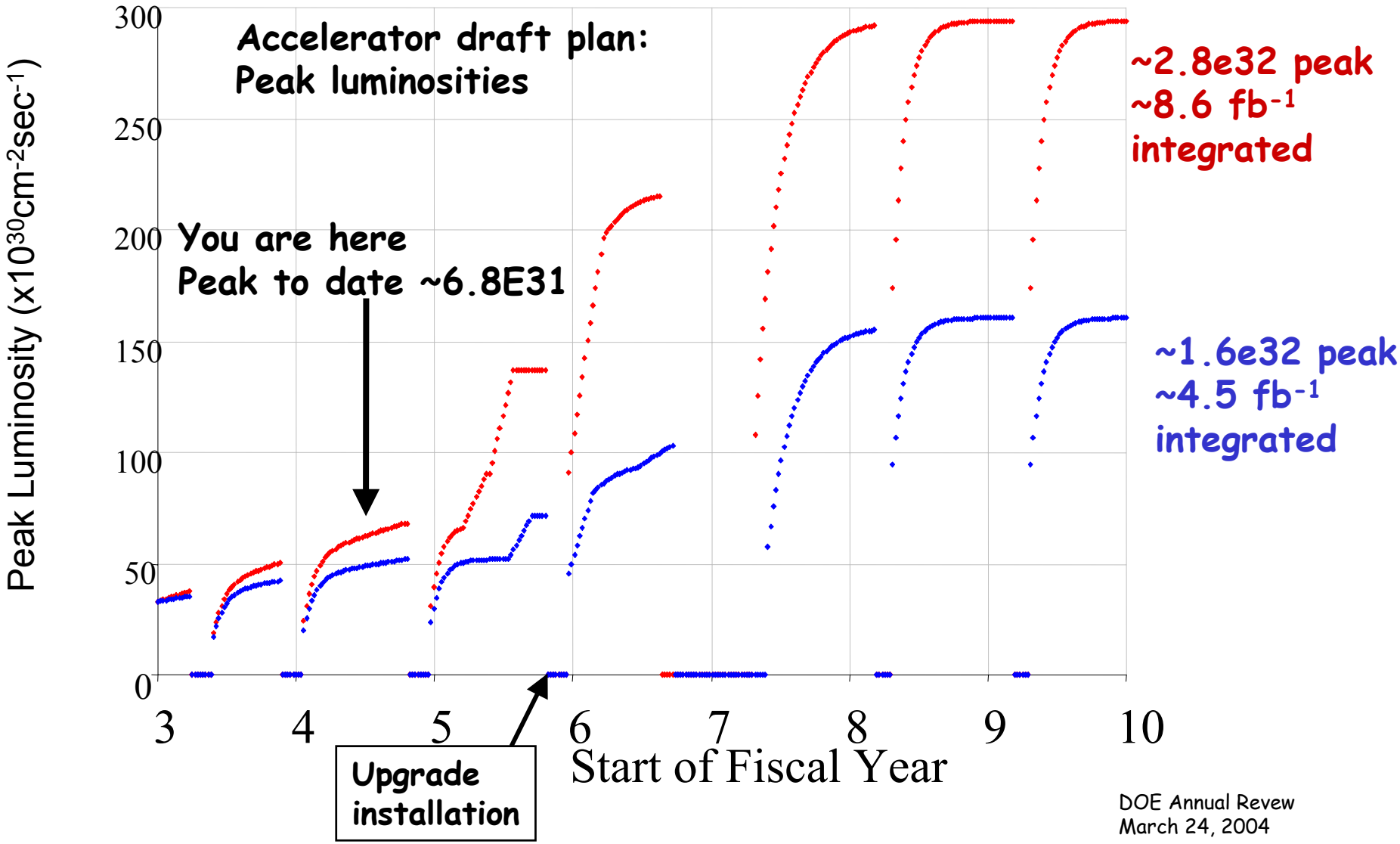
Run IIb Upgrade Organization



Installation /commissioning not formally part of the project

- **Clearly important**
- **We have a structure in place working on this**
- **More on this later in this talk**

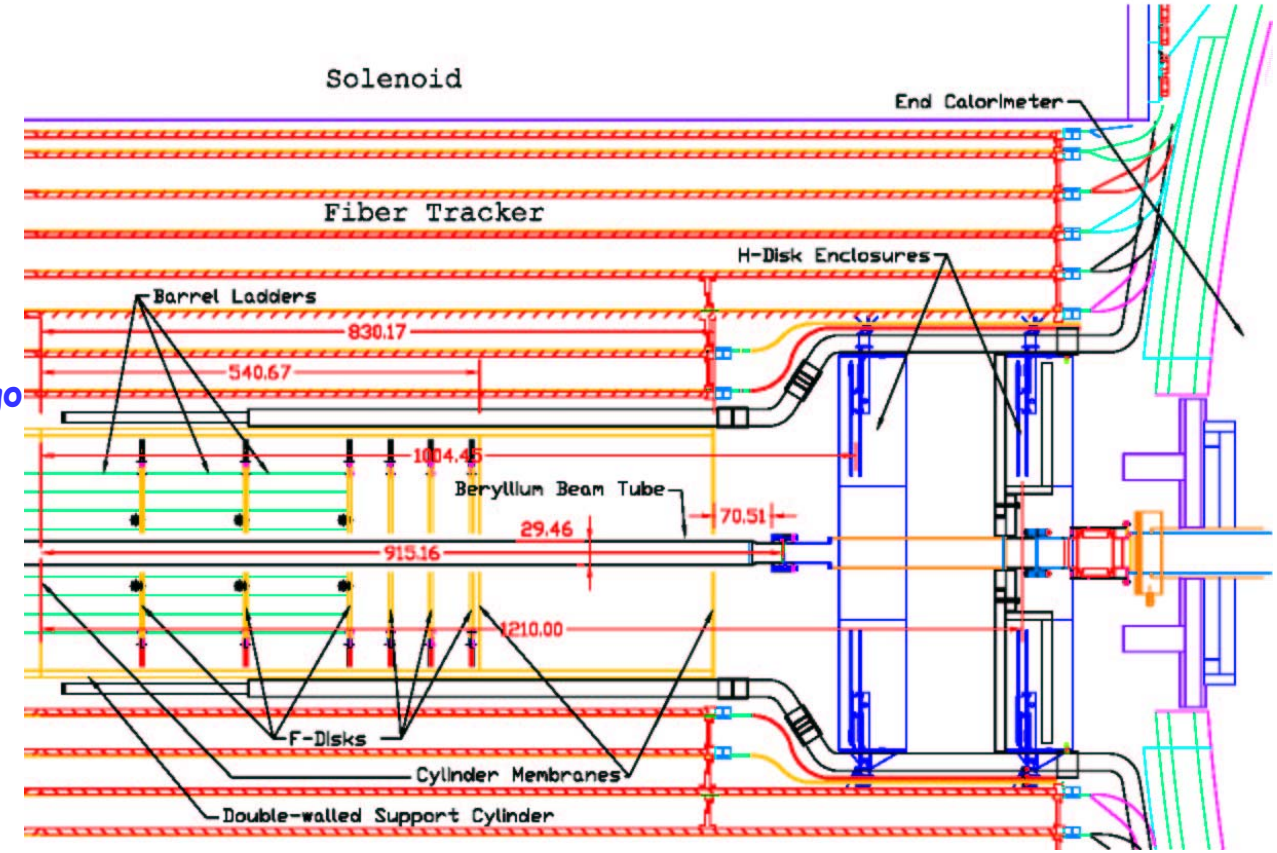
Run IIb Luminosity Projections



Silicon Layer Ø

Universities on DØ-LØ

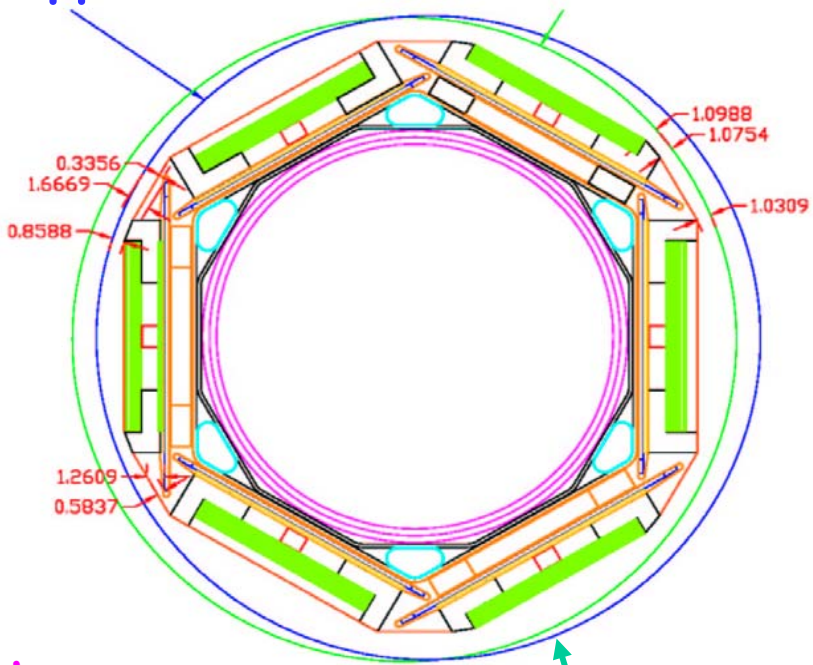
Brown
California State,Fresno
CINVESTAV Mexico
Fermilab
University of Illinois Chicago
Kansas State University
Kansas University
Louisiana Tech University
Michigan State University
Moscow State University
Northwestern University
Rice University
University of Rochester
SUNY-Stony Brook
University of Washington



Large NSF MRI grant (~$650k)
Additional in-kind university support

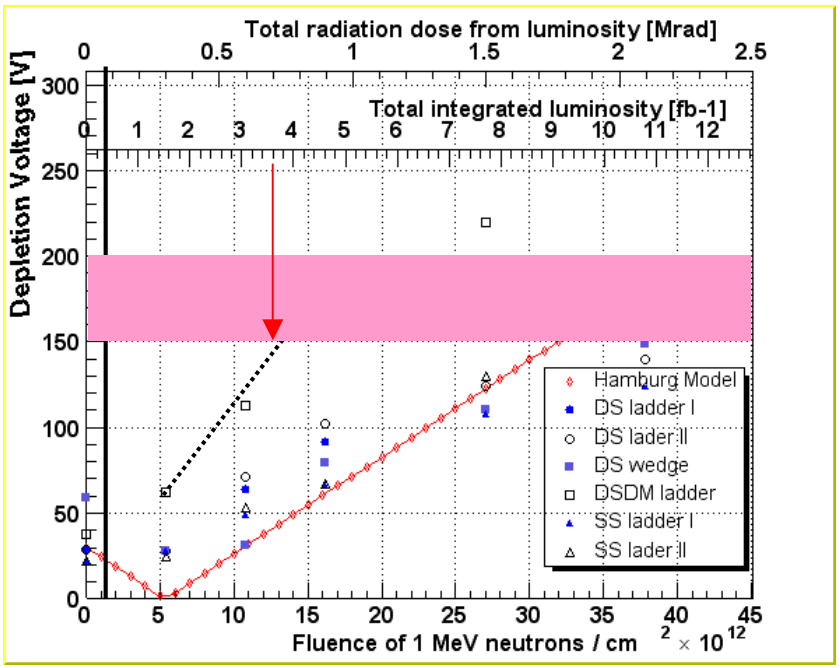
Layer Ø Design

- Design – use as much of the Run IIb R&D as possible
- Detector must fit in 22.8 mm SMT support structure opening
  - Six phi segments – match STT
  - Eight z segments 2x7,2x12cm
  - Analog cables – low mass
  - 48 HDIs x 256 channels
  - SVX4 chips (96)
- Replace at least outer H disks
- Sensor pitch – 71 μm (inner), 81 μm (outer)
  - Increases phi acceptance to 98.4%
  - Equal (71μm) pitch limits acceptance to 93.1%
  - Can be read out with one cable type

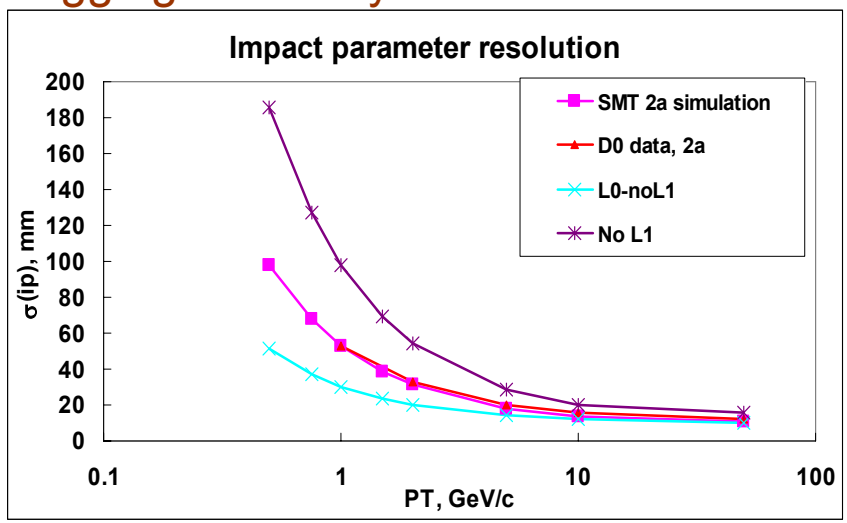


Need for Layer Ø

- We expect layer 1 Micron sensors to begin to fail at exposures of ~ 3.6 fb^{-1} (+- 50%)
- We are seeing continuing failures of readouts in the current detector (~85-90% currently good)



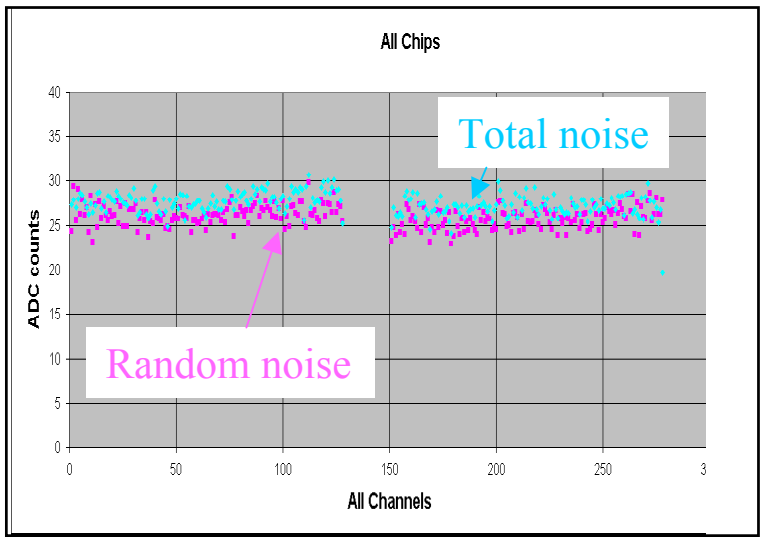
- Improvement in impact parameter resolution,especially at low momentum
- Translates directly into enhanced b tagging efficiency



Layer Ø Status

- Support and module design complete
- Fabricated small prototypes of carbon fiber support sections
- Grounding mesh and jumper circuits design complete
- Beginning work on production fixturing

Run2b prototype support with prototype L0 modules installed



Assembled/tested 12 proto L0 hybrids

Noise 1 ADC count/Flat pedestals

Assembled/mounted 4 Run2b layer 0 modules

No visible coherent noise w/o Faraday cage

New Layer 0 predicted S/N = 14:1

Order Status

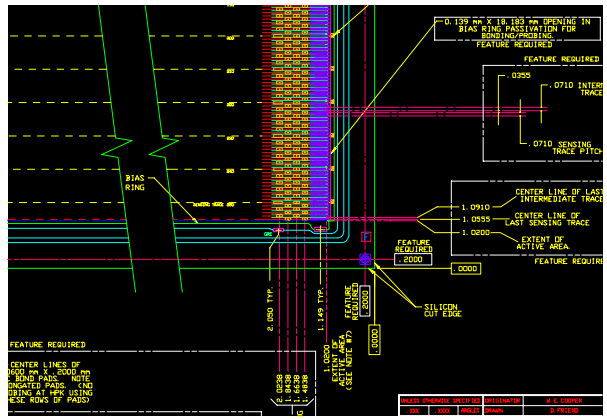
Major Orders:

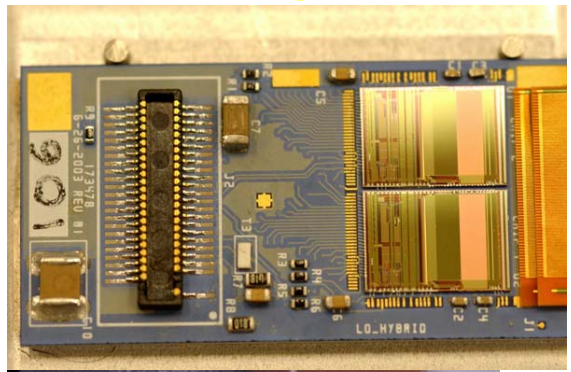
- Sensors from Hamamatsu
  - (due Jul 31)
- Hybrids from Amitron
  - (due July 15-Aug 15)
- Analog cables from Dyconex
  - (in progress, 4-5 week delivery)

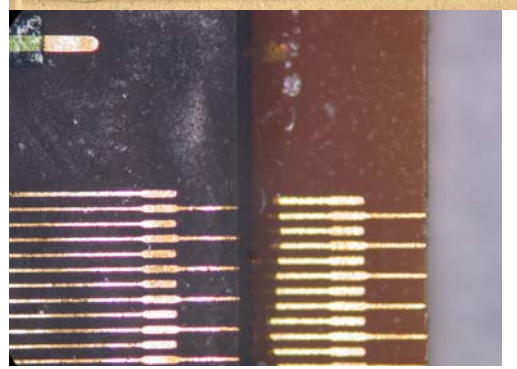
Smaller items:

- Pitch adapter prototype ordered
  - Received 3/22/04
- Formed PEEK tubing

2-3 months ahead of schedule for receipt of major components



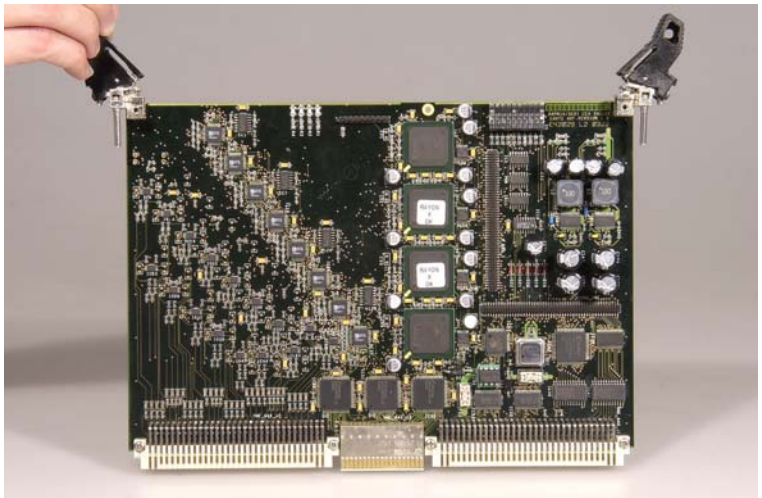


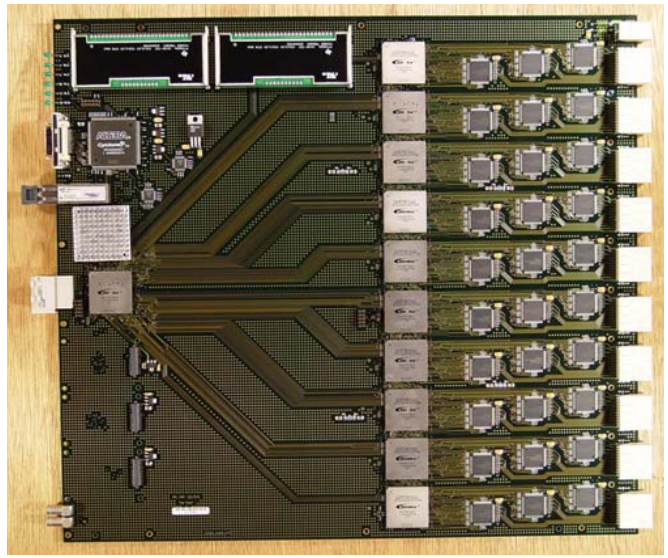


Ingredients of the Trigger Upgrade

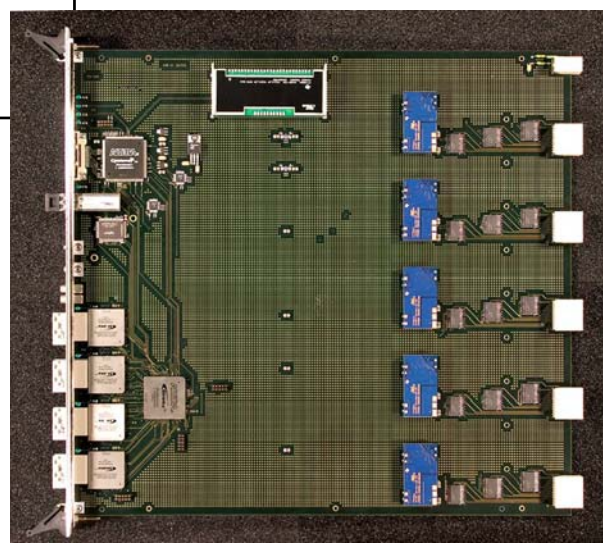
- Level 1
  - Calorimeter trigger upgrade
    - sharpens turn-on trigger thresholds
    - more topological cuts
  - Calorimeter track-match
    - fake EM rejection
    - tau trigger
  - L1 tracking trigger upgrade (CTT)
    - improved tracking rejection especially at higher occupancies
- Level 2
  - L2 Processor upgrades for more complex algorithms
  - Silicon Track Trigger expansion
    - More processing power
    - use trigger inputs from new silicon layer Ø
- New Readout Electronics for Central Fiber Tracker

Prototypes of All L1 Calorimeter Boards in Hand





ADF Prototype board
- Prototype testing done
- Working on v2 ADF layout

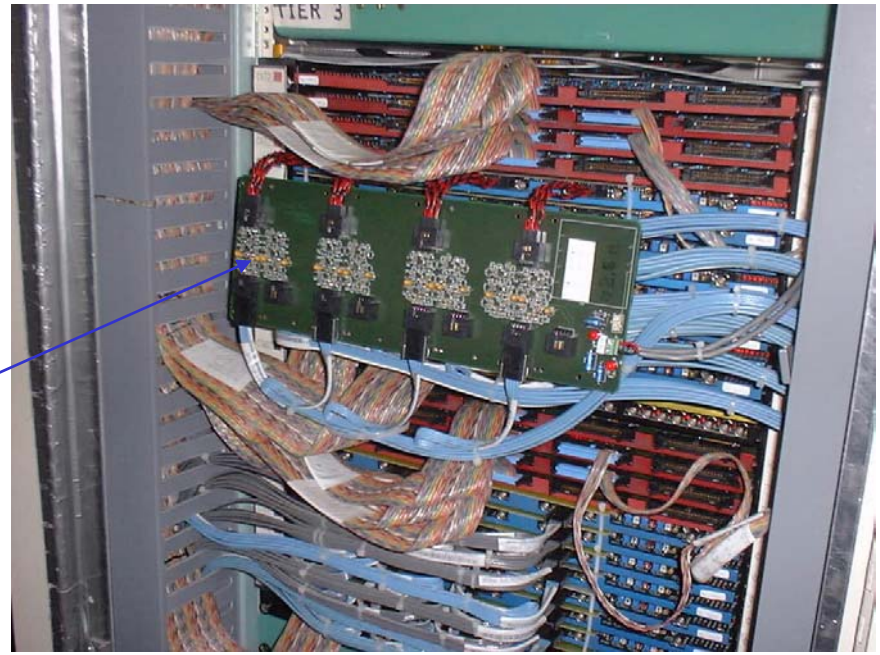


TAB prototype board
- Fully tested except L2/L3 output
- Nearly production ready

GAB prototype board
- Prototype in hand
- Bench testing begun

Signal Splitter

- Access to Real Trigger Tower Data using "Splitter" Boards
  - designed/built by Saclay
  - active split of analog signals at CTFE input
  - 4 Trigger Towers per board
  - installed: Jan. 2003



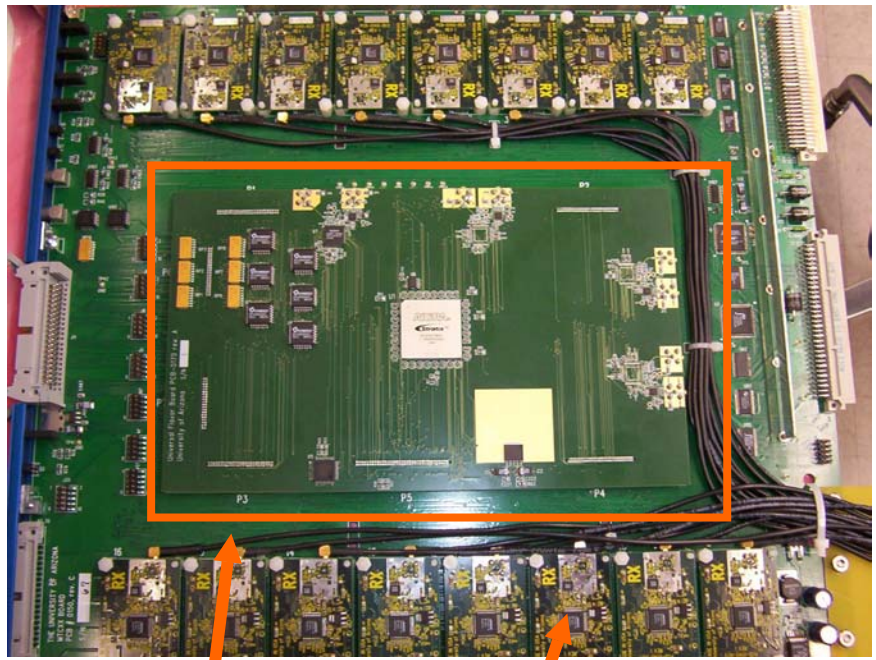
- Splitter Data
  - no perturbation of Run IIa L1Cal signals
  - allows tests of digital filter algorithm with real data

L1 Cal Trigger Prototype Integration Tests

- Set up semi-permanent Test Area outside of Movable Counting House
  - connection to SCL, split data signals
  - allows L1Cal tests without disturbing Run IIa data taking
- Tests with ADF + TAB prototypes
  - SCL → VME/SCL → TAB, ADF
  - BLS (real Calorimeter) data (from splitters) → ADF → TAB
  - TAB → L1MU (L1Cal-Track substitute)
- GAB prototype first testing at NEVIS
  - In test crate, powered on, downloaded firmware, testing functionality
- Need to test TAB → L2/L3 before TAB production begins
  - This is happening during the "mini-shutdown" now
  - If we don't succeed during the shutdown, we have all the pieces at FNAL and will schedule tests during machine studies, etc.
    - This testing is ~ 6 months ahead of schedule

L1 Cal Track Match

- UFB (Flavor Board)
  - Prototypes in hand
  - L1MU "05" algorithm implemented in Stratix EP1S20F780C7
  - $H \rightarrow \tau\tau$ algorithm successfully implemented and tested
- Infrastructure
  - VME crates, processors, power supplies, cables in hand
  - L1CTT to L1CalTrack cables installed

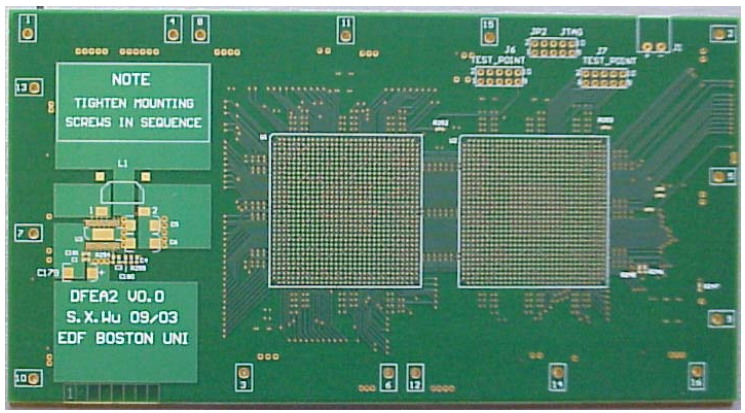


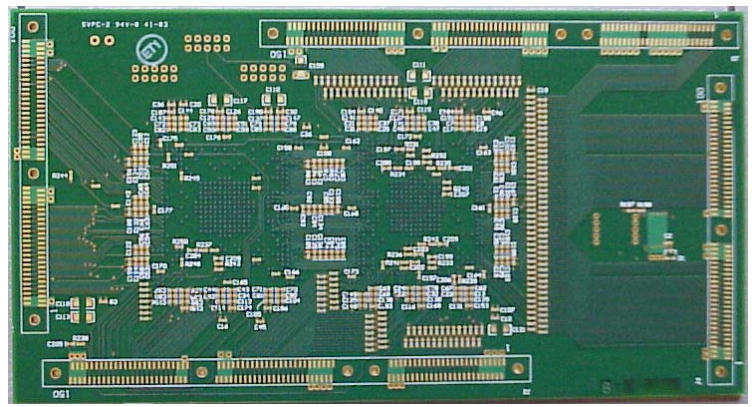
MTCxx (mother)
Run IIa version

Universal Flavor board (daughter)
Run IIb prototype

L1 Central Track Trigger

- Digital Front End Axial (DFEA) daughter cards redesigned with larger FPGA's (Xilinx Virtex-II XC2V6000)
  - Allows more complicated equations for using narrower roads
- Implemented prototype firmware (Boston U)
  - Includes equation files from all 4 momentum bins
  - DFEA logic is implemented in two FPGAs
  - Prototype board functionality tested
- Detailed system design changes to make the upgrade easier to commission in progress
  - Review scheduled beginning of April





Central Fiber Tracker readout upgrade (AFE II)

- AFE II + TriPT will
  - Improve noise floor and pedestal stability which will allow for consistent and reliable threshold setting at the level of 1.5 pe
    - Better hit efficiency and point resolution
  - Readout architecture much more flexible
    - Less deadtime
    - With additional memory, buffers can be added to greatly increase L1 capability
  - Added functionality of the TriPT (z information)
    - Large reduction in track reconstruction time
  - Elimination of SIFT, SVXIIe, and MCM in readout should greatly reduce board maintenance load
- R&D for AFE is going well
  - Expect prototype AFE + TRiP late spring/early summer
  - This part of the project is only conditionally approved
    - Plan to test prototype, compare with simulations
    - Hold DØ internal review – this is the decision branch point
    - If (Yes) {Hold laboratory review}
  - If all reviews positive, then will go ahead with project

DAQ/Online

System	Items	Need
Level 3 filter nodes	96 more L3 Farm nodes	Match to rates and processing requirements
DAQ HOST system	Linux data logging nodes and buffer disk arrays	Replace existing systems with higher performance nodes
ORACLE systems	Database nodes, disk arrays, and backup systems	Adopt lab standard ORACLE platform
File Server systems	Linux server nodes, disk arrays, and backup systems	Provide increased storage capacity
Slow Control system	VME processors for control and monitoring of detector	Improve monitoring performance for extended run

Upgrades to DAQ/Online systems required for long-term, high rate running during Run IIb

Upgrade Installation/Commissioning

- Resource loaded installation/technical installation plan for full upgrade (LØ, Trigger, Online)
- Some upgrade pieces require access to complex
  - LØ installation requires long access to collision hall
  - L1Cal/CTT shadows LØ (decommissioning current trigger)
- Other upgrade pieces do not require access (or very short access)
  - Some done "adiabatically" (AFE, L2β, etc.)
- Collaboration wide standing committee has been formed to examine in detail the installation to physics commissioning plan for each upgrade part
  - Formal internal review process to determine installation readiness
  - Committee formed with both project and nonproject people
  - Goal is to ***maximize physics***

Upgrade Trigger Installation/Commissioning Plans

- L1 Cal trigger: Summer '05
  - L1 Cal trigger pre-tested on sidewalk
  - Installation/commissioniong ~ 10 weeks
    - use 2 weeks with beam to verify trigger
    - Precision calibration in parallel with data taking, ~ 1 month
- L1cal-track
  - System commissioned with L1mu modules, then replaced with real L1cal-track modules
  - Ready in advance for L1cal inputs
- L2 STT
  - installed/technically commissioned during Layer Ø installation
- L1 CTT (Summer '05)
  - System redesign with ease of commissioning in mind
- L2β can be upgraded earlier - whenever necessary

Total MIE Project Cost

Project Total Equipment Cost (DOE MIE)

DOE TEC, by subsystem in AYk$	Total	Cont. only	EQ base	G&A only
Silicon	1824	893	735	196
Trigger	5595	1676	3268	651
DAQ/Online	1389	327	881	181
Project Administration	1151	227	729	195
TOTAL	9959	3124	5613	1222

Contingency fraction on MIE portion = 45%

- Total DOE cost (fully burdened, AY$)
- Does not include MRI (Trigger, Silicon LØ) or University in-kind
- Includes AFE II upgrade

Director's Milestones

D0 Detector Upgrade
Director's Milestones
Forecast Dates

Fiscal Year

Task Name	Forecast Date
1.6 Layer 0 Silicon	
Freeze Mechanical Parameters	12/16
Release Sensors for Production	3/19
Release Hybrids for Production	3/26
Release Analog Cables for Production	3/26
All Analog Cables Delivered and Tested	9/29
All Sensors Delivered and Tested	11/17
All L0 Hybrids Delivered, Stuffed, and Tested	1/19
All Adapter Cards Delivered and Tested	2/23
Silicon L0 Module Production Complete	3/24
Layer 0 Silicon Detector Ready to Move to DAB	7/21
1.2 Trigger	
L1 Calorimeter Trigger TAB/GAB Prototyping Complete	3/1
Start Production TAB Fabrication	10/25
L1 Trigger Cal-Trk Match Production and Testing Completed	10/29
L2 Silicon Track Trigger Production and Testing Complete	1/31
L1 Central Track Trigger Production And Testing Complete	2/23
L2 Beta Trigger Production And Testing Complete	2/28
L2 Trigger Upgrade Production and Testing Complete	2/28
L1 Calorimeter Trigger Production And Testing Complete	7/5
L1 Trigger Upgrade Production and Testing Complete	7/5
1.3 Online	
Online System Production and Testing Complete	6/17

planning to finish July 05 for a summer/fall 2005 installation

Conclusions

- Project is making impressive technical progress
  - Trigger solidly in prototype testing phase
    - All major calorimeter trigger boards testing prototypes
      - Major L1 Cal integration milestones met using real data
      - Permanent integration stand installed and commissioned
  - Layer Ø is springboarding off of Run IIb R&D and moving quickly
    - All high lead time components have been ordered
    - Project is on schedule for Summer/Fall '05 installation
- Installation/Commissioning plans firming up
  - Planning to install during 2005 summer/fall shutdown