Status of Electronics Components & Bump Bonding Procurement

CMS FNAL PMG

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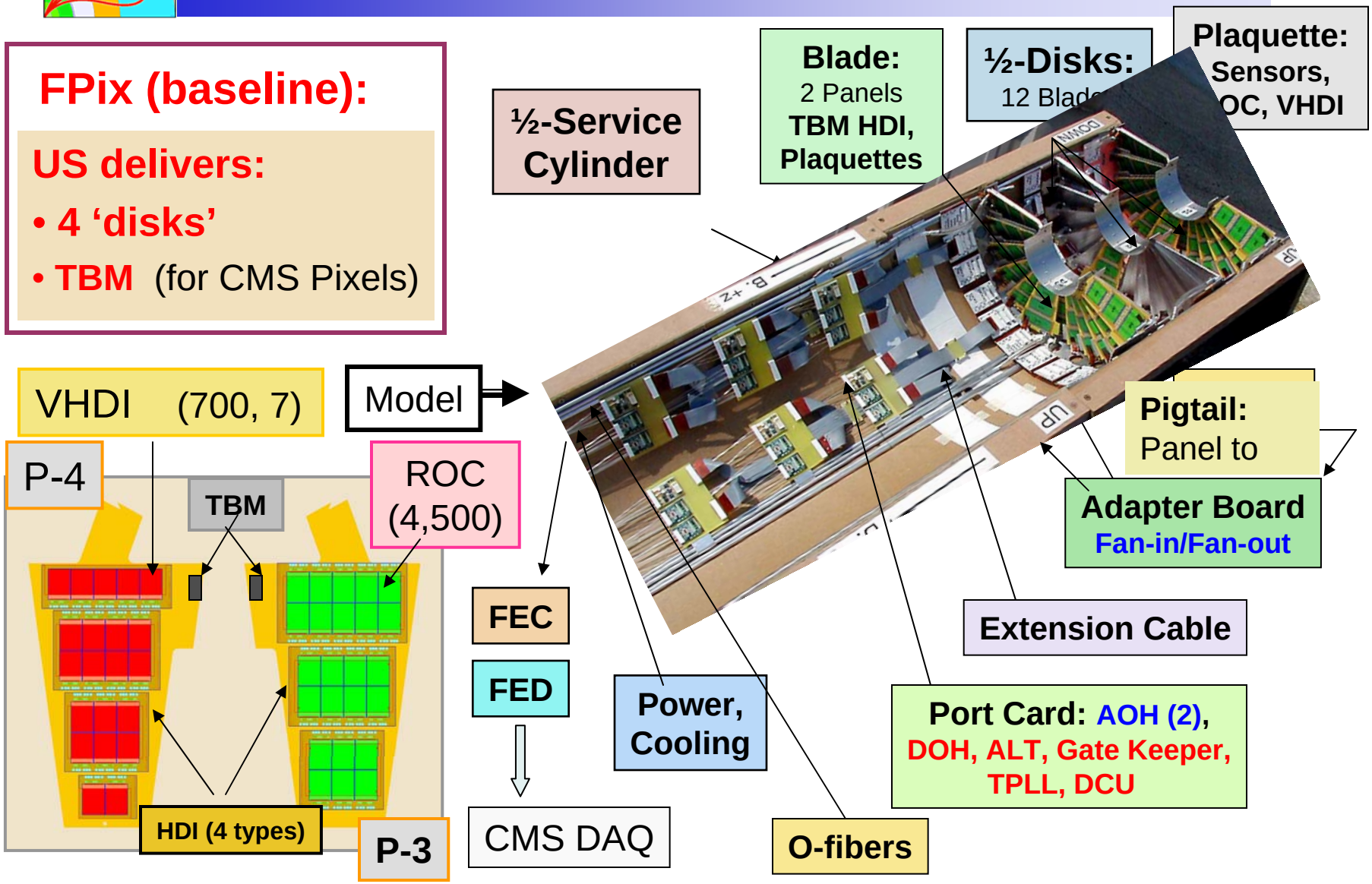
September 29, 2006

Overview of the CMS Pixel Disks

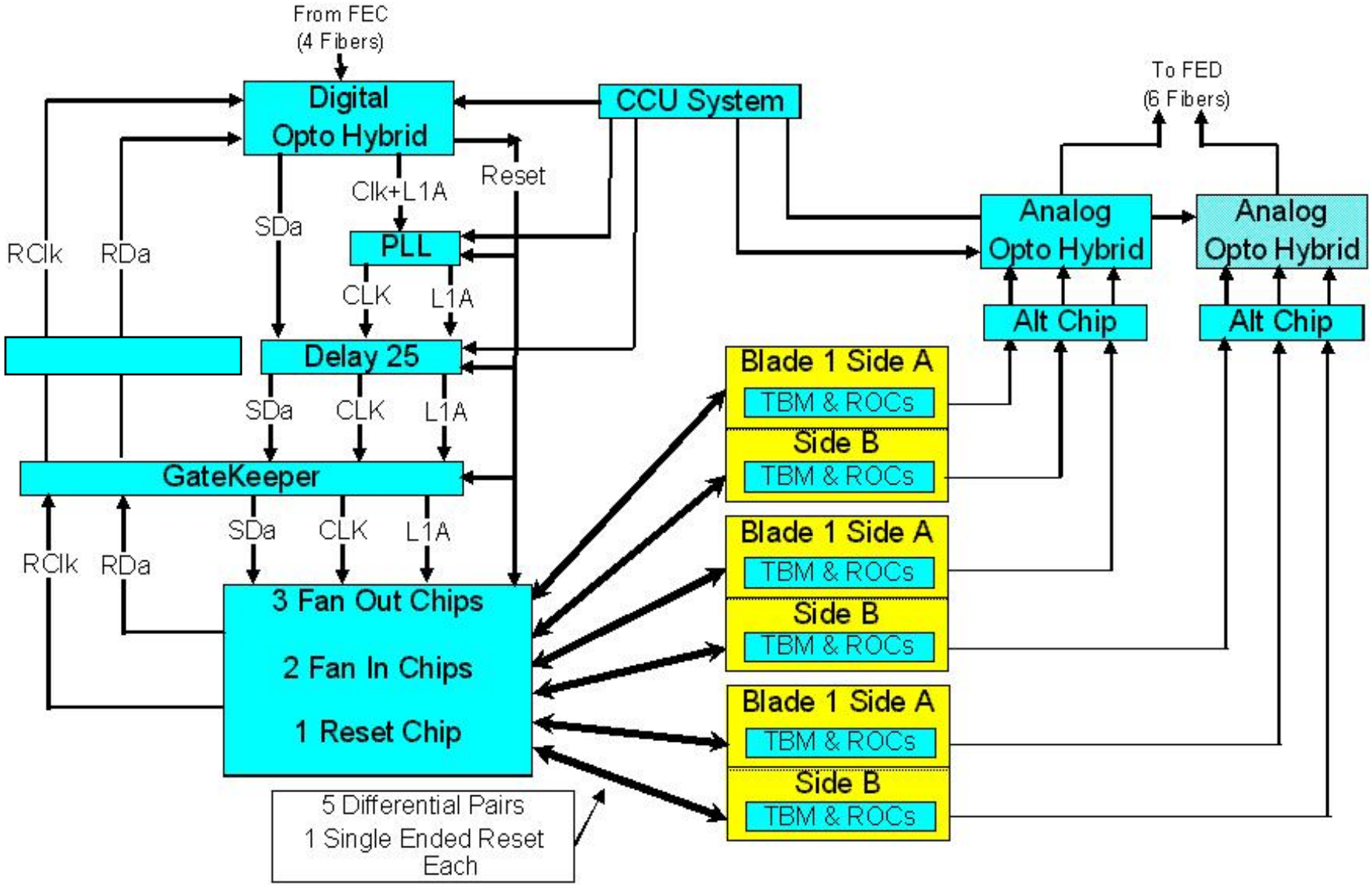
FPix (baseline):

US delivers:

- **4 'disks'**
- **TBM** (for CMS Pixels)



Front-end Electronics



Pixel Detector Control

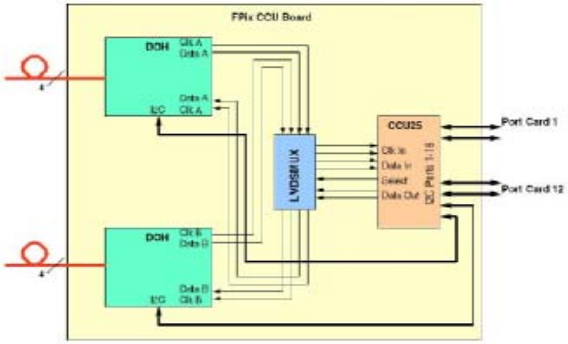
- **Pixel system has two paths for controlling and configuring the front-end electronics**
- **Pixel FEC (PSI2C or fast I2C: 40 MHz serial channel) to communicate with the ROCs and TBMs**
  - **Control**
    - CMS clock and trigger provided by the TTC system
  - **Configuration**
    - fast download of the registers (DACs, trim/mask)
    - Readback of the TBM registers (diagnostics)

  - **Pixel FEC -> optical fibers->pixel DOH (Port card) (protocol: serial) (1 FEC channel to one DOH)**
  - **Port card-> extension cable ->Adapter board**
  - **Adapter board thru fan-in/fan-out chips communicate with 3 blades (6 panels)**
- **PLL: recover clock + control global timing**
- **Delay 25: align SDA wrt clock**
- **Gatekeeper:**
  - **LVDS-LCDS converter**
  - **Blocks SDA idle pattern**

Pixel Control (2)

- The other path uses the “tracker FEC” and standard I2C protocol to communicate with components such as AOH, DOH, CCU, Delay25, PLL etc.
- Tracker FEC -> optical fibers -> tracker DOH -> CCU -> port card

Forward Pixel CCU Boards



- DCU is being read out via an I2C communication channel, originating on a CCU board
- CCU board’s I2C is used to program other ASICs on the Port Card (TPLL, DOH, AOH) as well.

Components

- **ASICS**
  - ROC (PSI46v2) (procurement and wafer probing)
  - TBM (design, procurement, test, dicing)
  - Other chips (gatekeeper, fan-in, fan-out, Delay25, TPLL, DCU, CCU, ALT etc….) (varies)

DONE

- **Printed circuits**
  - VHDI (design, procurement, and acceptance test)
  - HDI (design, procurement and acceptance test)
  - Adapter board (design, procurement and test)
  - Port card (design, procurement and test)
  - CCU (design, procurement and test)
  - Power filtering/interface boards (design, procurement, assembly, and acceptance test)
- **Modules and boards from CERN/Europe (Procurement)**
  - FEC (firmware and software)
  - FED (software)
  - DOH
  - AOH

DONE

- **Test stand**
  - Plaquette test
  - Panel test
  - Burn-in

DONE

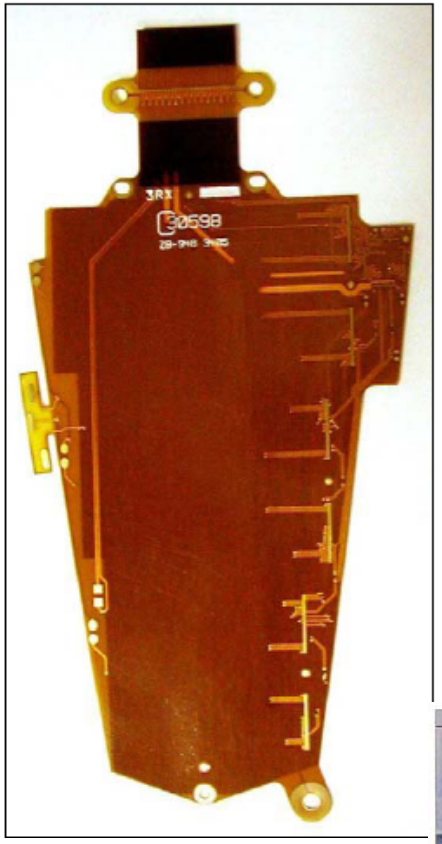
- **Other hardware (Procurement)**
  - Power supplies
  - Cables (optical fibers, power cables, extension cables)
  - VME crates and bridges
  - Slow control system

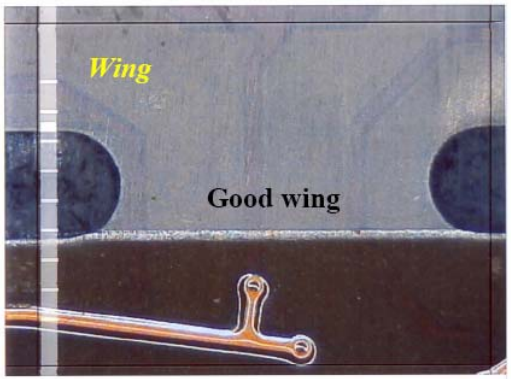
Status of Electronics

- Completed
  - All ASICS.
  - VHDIs
  - RH-HDIs
  - Port card
  - Two versions of the Adapter boards (-z/inner and outer)
  - Optohybrids – DOHs, AOHS
  - Power filtering boards
  - FEC
  - TTC modules
  - VME crates and optical-PCI bridges
  - All test stands (testing plaquettes, panel, burn-in)
  - Optical fibers, HV cables
- Waiting for Delivery
  - HDI-4L
  - Extension cable
  - Power supplies
  - Slow control system
- Still to be submitted
  - HDI-3L
  - CCU production board
  - Two versions of adapter board (+z/inner and outer)

HDI

- 4 versions : LH and RH, 3 plaugettes and 4 plaquettes (HDI_3RX, HDI_4RX, HDI_4LX and HDI_3LX)
- HDI_3RX an HDI_4RX laminated and tested
- HDI_3LX and 4LX submitted to CERN TS-DEM early June
- About 40+ circuits of each received on August 10
- Problems on thickness in the folded-wing area; showed delamination after thermal cycling
- CERN TS-DEM tried plasma etching
- Thickness reduced from 150um to about 65 um and tests showed that the circuits do not delaminate; electrical tests also show good results except:
- HDI-3LX: layout mistake leading to unacceptable noise
- Needs modification to the layout and new submission; work started yesterday and expected to complete early next week; expect 4-5 weeks for delivery
- HDI-4LX (20+ circuits have been plasma etched at CERN and shipped to Fermilab on Monday
- We will ship back the 40+ circuits that we have to CERN for plasma etching





CCU

- At the last PMG, we reported the status and results of our system test. At that time, we did not have a CCU board. For slow I2C, we used a commercial device (no tracker FEC and DOH)
- Proto-CCU test board was made which has one tracker DOH and one CCUM board from the TEC
- Connected by optical fibers to tracker FEC (VME crate) and to the port card
- Can communicate with CCU using the tracker FEC
- Successfully configured port card via one I2C channel of the CCU. E.g. enable the delay chip, read DCU etc
- For the pilot run detector commissioning, we will use this board and don't need to use commercial I2C interface any more.
- Work has started on a production CCU board which will have two DOHs and a ring of CCUs. We got from our barrel colleagues their schematic. Our design will be simialr to theirs.
- Expect to have this production board available for testing around end of November.

Key Procurements

WBS#	Item	Base Cost K$	Contingency	PO date	PO Amount (K$)
5.22.1.1.4.3	TBM	30	5%	11/10/05	31
5.22.2.1.2.2.2	VHDI	51	15%	12/09/05	57
5.22.2.2.2.2	HDI	64	15%	1/19/06	22(RH) 28 (LH)
5.22.3.1.2.4.2	ROC	88 (40 wafers)	20%	11/17/05	65 (29 wafers)
5.22.4.2.2.5	Power Supplies	93	10%	CERN	93
5.22.4.6 & 5.22.4.7	FEC & FED	84	15%	From Europe	Expect ~75

Remaining Procurement

- **HDI-3LX: about $10K**
- **CCU: about $1.5K**
- **Adapter board: $14K including assembly charges**
- **Still need to pay CERN and collaborating institutes: (Money has been committed in the sense that we have either received the parts or be part of a big CERN order)**
  - Power supplies $92K
  - Slow control hardware $22K
  - FED, FEC, optohybrids: $75K

Labor

From Effort Report : July 2005 – March 2006

Engineers

Name	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep
Baldin	.50	.50	.50	.50	.50	.50	.50	.10	.30
Gingu	.8	.75	.8	.50	.50	0.0	.50	.25	0.0
Los	.80	.80	.80	.80	.80	.80	.80	.80	0.8
Matulik	.60	.60	.70	.25	0.0	.60	.50	0.0	.10

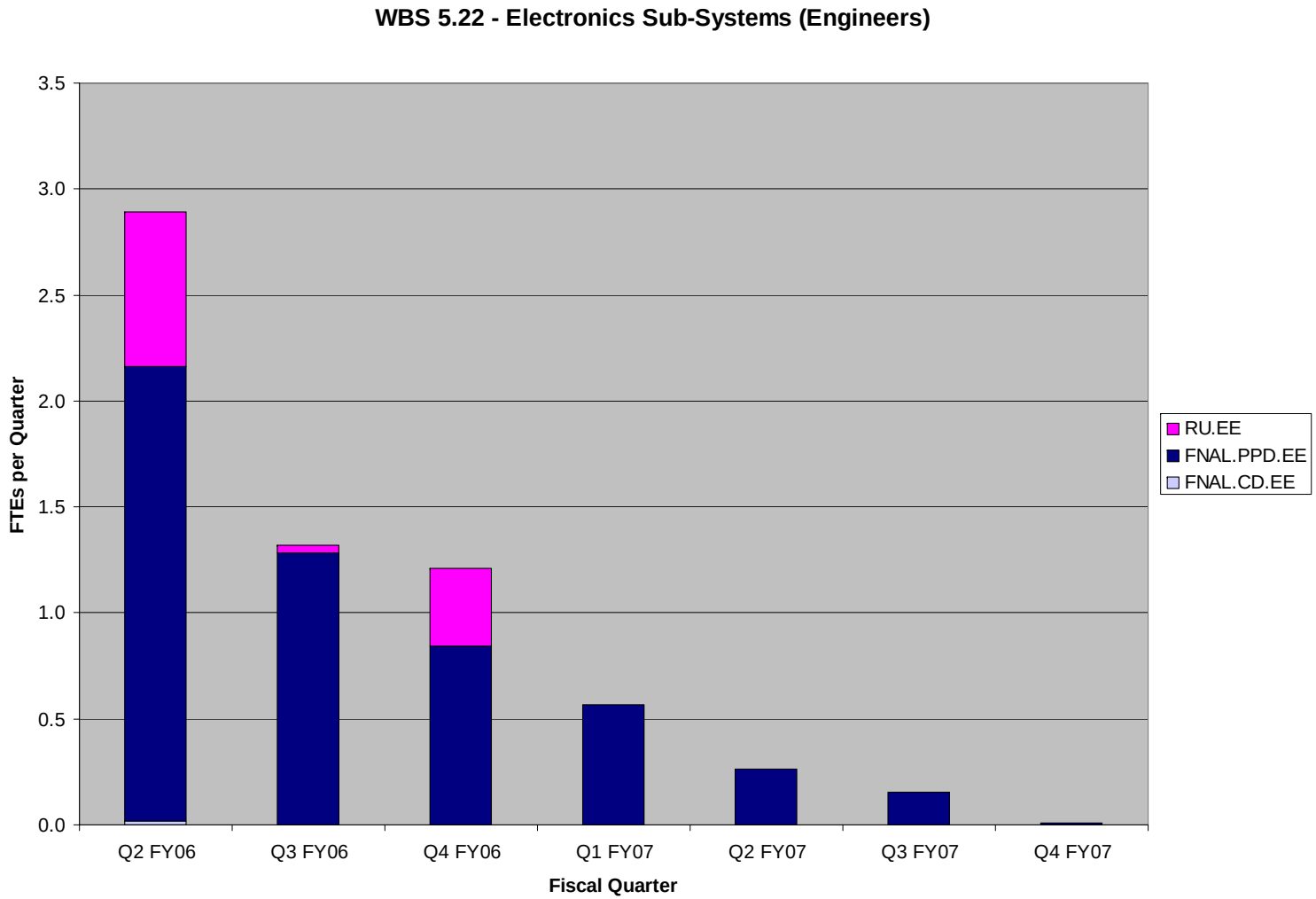
Technicians:

Consistently ~ 0.5 FTE until April, a spike of 1.5FTE (HDI, assembly of burn-in boards) in May and then drop back down to 0.8 in June. Since then at 0.3 FTE level

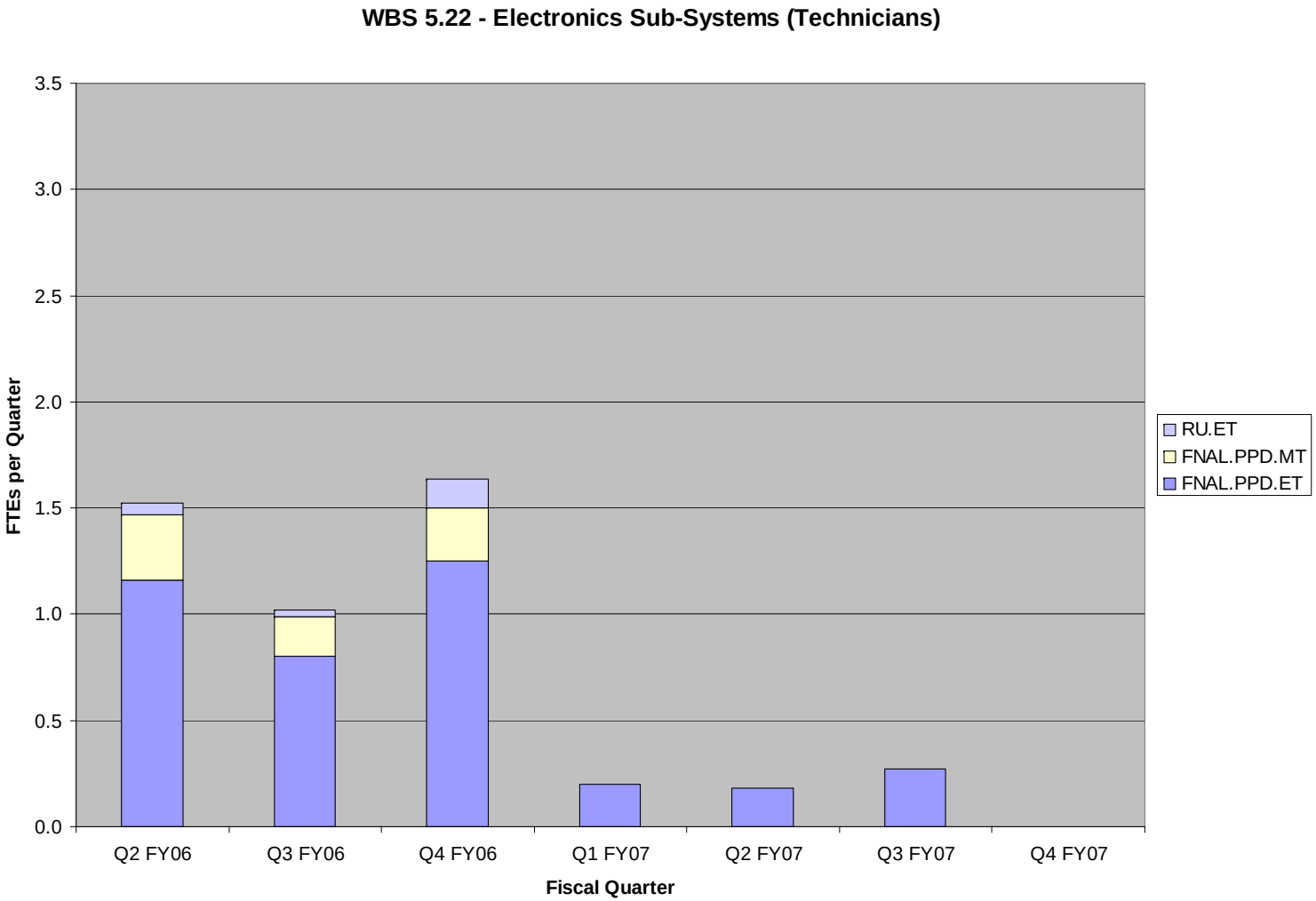
Manpower Estimate

- Our manpower need is winding down! (most of the tasks have been done)
  - Revised layout of HDI and grounding strip
  - Design of two remaining versions of the adapter board and CCU
  - Complete the assembly of the power filtering boards
- EEs are needed to support Plaquette, panel, burn-in test and System test. These are covered in WBS5.23.3 and 5.23.4.

Labor


WBS 5.22 - Electronics Sub-Systems (Engineers)
FTEs per Quarter
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
Q2 FY06
Q3 FY06
Q4 FY06
Q1 FY07
Q2 FY07
Q3 FY07
Q4 FY07
Fiscal Quarter
RU.EE
FNAL.PPD.EE
FNAL.CD.EE

Labor (Technicians)



Remaining Tasks

- **HDI (Matulik) (Q4- Q1/FY07)**
  - Revise LH-3LX HDI design, prepare Gerber file, final check and submission
  - Acceptance test of final product
- **Adapter Board (Los) (Q1-Q2/FY07)**
  - Design and layout for the +z versions and procurement
  - Acceptance test
- **CCU board (Turqueti/Los) Q1/FY07**
  - Design and layout of the production version, procurment and testing

Bump Bonding: Overview of Process

- All vendors use Pb/Sn solder
- ROC wafers: UBM, Bumping, thinning to required thickness, dicing
- Sensor wafers: UBM, dicing
- Flip-chip bonding: reflow process
- Wafers processed in batches
- Plaquettes will be delivered in batches
- Test on wafers, devices, control samples for QA

Details of the steps

Sensor wafers

- Design/finish of pad mask basing on GDS file supplied by us.
- Manufacturing of glass mask
- Sputter deposition of the plating-base
- Lithography of the resist layer
- Electroplating of the bond pads
- Stripping of resist and plating-base
- Dicing of wafers into sensor modules
- Cleaning, inspection and sorting

ROC wafers

- Design/finish of pad mask basing on data supplied by the customer (GDSII format).
- Manufacturing of glass mask
- Sputter deposition of the plating-base
- Lithography of the resist layer
- Electroplating of the PbSn bumps
- Stripping of resist and plating-base
- Reflow of bumps
- Preparing for wafer thinning
- Wafer thinning to 180-200 µm
- Dicing of wafer into dies
- Cleaning, inspection and sorting

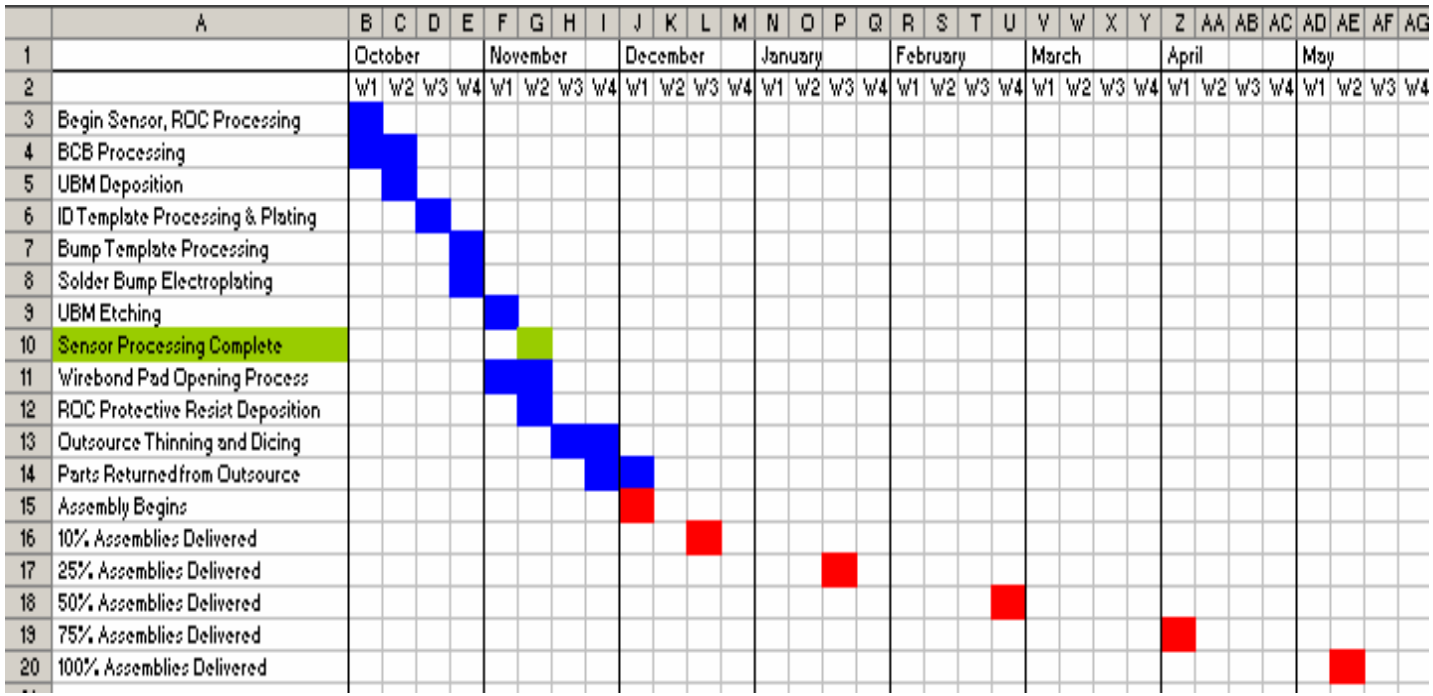
Procurement Plan

- Production in two phases
- Phase 1: 10% each to two vendors
- Phase 2: based on phase 1 results, may decide to go with one or two vendors.
- Decision based on technical quality, schedule requirements, and cost
- Phase 1 contracts were awarded to IZM (Berlin, Germany) and RTI (NC, USA)
- Phase 1 delivery completed around August 10.
- Reminder: we need 672 modules for the two-disk forward pixel detector (7 types of modules)

RTI

- Received from RTI 83 modules (Phase 1 Production)
- Test results showed acceptable yield
- Purchase Order for phase 2 production at RTI placed last Friday
- Contract will be for 48 1x2s, 1x5s, 2x5s, and 96 2x3s and 2x4s. Total = 336 modules + 20 single-chip detectors (cf 672 working modules needed for the forward pixel detector)
- They have 237 good ROCs (bumped, thinned and diced) and 4 sensor wafers left over from Phase 1
- Need about 11 ROC wafers and 50 sensor wafers
- Their batch size: 5-6 wafers for ROCs and 15 wafers for sensor
- Send them ROC wafers in two batches and sensor wafers in 3 batches
- First batch of wafers shipped to RTI on Tuesday
- Expect delivery of modules starting December 10
- Have an option to produce 20% more

Preliminary RTI Schedule



Wafers were shipped earlier this week to RTI

Expected first batch of modules will be delivered around mid-December

IZM

- PO placed end of July
- First batch of ROC and sensor wafer shipped on August 10
- Contract is for 294 modules with an option to go for an extra 20%.
- Expected delivery of modules starting mid-October
- Summing all the orders, our contracted number of modules= 168+294+336 or 798 modules

IZM Production

Schedule

	A	D	E	F	G	H
1	Schedule IZM bumping phase 2 for the USCMSFPIX project					
2						
3	week	sensors batch1-12 wafer	ROC batch1 - 4 wafer	sensors batch2 - 20 wafer	ROC batch2 - 8 wafer	sensors batch3 - 10 v
4	1	cleaning, inspection, sputtering	cleaning, inspection, sputtering			
5	2	lithography	lithography			
6	3	plating	plating			
7	4	plating	plating			
8	5	inspection after plating	inspection, bump protection resist		cleaning, inspection, sputtering	
9	6	dicing	thinning	cleaning, inspection, sputtering	lithography	
10	7	(module assembly with remaining preproduction ROC	dicing	lithography	plating	
11	8		resist removal, single chip inspection	lithography	plating	
12	9	module assembly		plating	inspection, bump protection resist	
13	10	module assembly		plating	thinning	
14	11	module assembly		inspection after plating	dicing	
15	12	module assembly		dicing	resist removal, single chip inspection	cleaning, inspection, spu
16	13			module assembly		lithography
17	14			module assembly		plating
18	15			module assembly		plating
19	16			module assembly		inspection after plati
20	17			module assembly		dicing
21	18			module assembly		
22	19			module assembly		
23	20			module assembly		
24	21					module assembly
25	22					module assembly
26	23					module assembly
27	24					module assembly

Cost

Company	Production Phase 1	Phase 2
RTI	$88,777	$372,101
IZM	$109,000	$273,000

This is still the major cost driver for the whole project
It is also the schedule driver
Because of schedule concerns, we have decided to keep two vendors for phase 2. Based on delivered modules from phase 1, both meet our specification and schedule, but there are areas that need improvements. We have detailed discussion and work plan with both vendors in place including re-work of some of the modules that failed our acceptance criteria. Initial results from IZM on re-work are very promising. RTI is in the process of doing the re-work.

Summary

- **Technical Progress is excellent**
  - **Production has completed for most of the electronics components**
  - **Production Bump bonding has entered into phase 2**
  - **Orders for most big ticket items have been completed or placed**
- **Our cost estimate (both M&S and labor) has been fairly accurate and we don't expect big cost overruns**