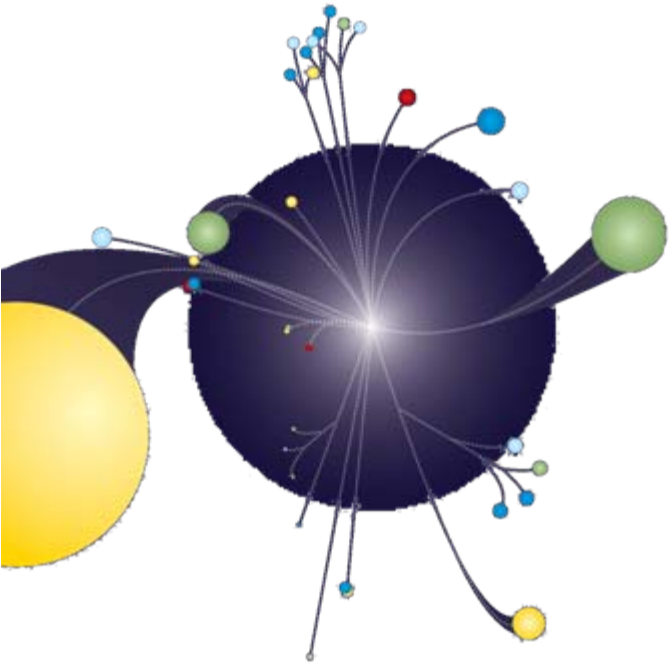
# Detector R&D Initiatives at Fermilab

# New Silicon Technologies and their Applications



Marcel Demarteau

ANL-Chicago-Fermilab Collaboration Meeting
January 23 2009
Fermilab

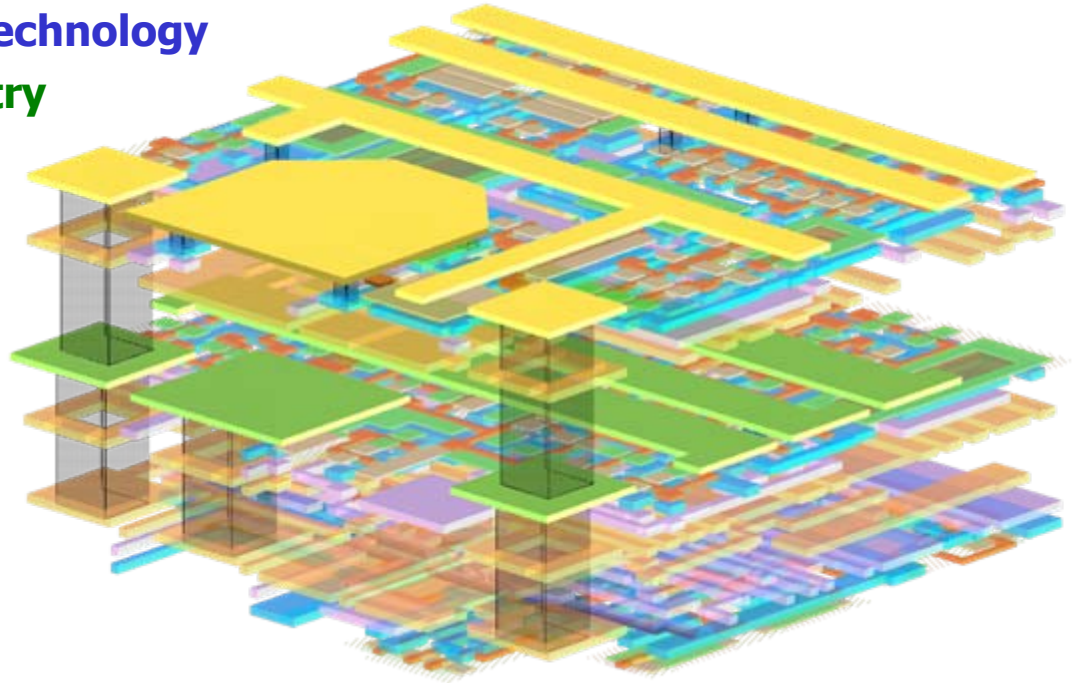
# Collaborative Efforts

- **Strategic Collaborative Initiatives (SCI) awarded in 2008 in the detector area:**
  - **"The Development of Ultra-Fast Timing Detectors"**
    ***Henry Frisch (UofC), Erik Ramberg (Fermilab), Karen Byrum (ANL)***
  - **"Absolute Measurement of Air Fluorescence Yield for Ultra-High Energy Cosmic Rays"**
    ***Paolo Privitera (UofC), Carlos Hojvat (Fermilab)***
- **MoU put in place with Argonne to have access to Fermilab Electrical Engineering Department**
- **Regular discussions between the institutions**
  - **Discussion January 21 between ANL ALS group and Fermilab EE group**
- **Ongoing collaborative efforts**
  - **Design of the DCAL chip for digital hadron calorimetry**
  - **...**

# Outline

- **Vertical Integrated Silicon and Bonding Technology**
  - **3D Vertical Integrated Silicon Technology**
  - **Bonding Technologies**
  - **Applications**
    - FE Electronics
    - Pixel Detectors and Trackers
    - Imaging

- **Pixelated Photo-Detector Technology**
  - **Dual Readout Calorimetry**
  - **Muon Detection**
  - **Particle-Astrophysics**



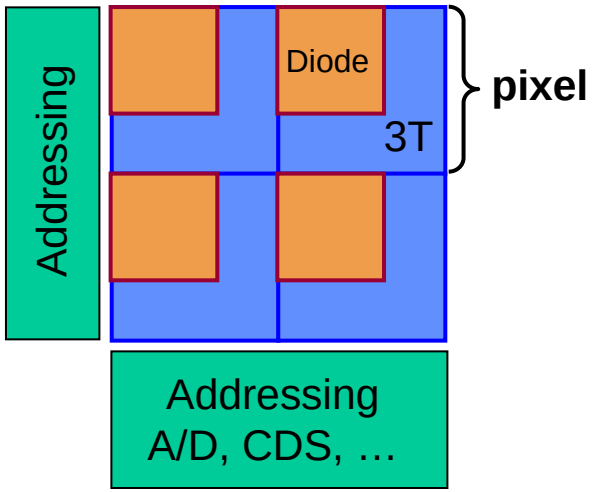
# Vertical Integrated Circuits – 3D

- "Conventional MAPS"
  - Pixel electronics and detectors share area
  - Fill factor loss
  - Co-optimized fabrication
  - Control and support electronics placed outside of imaging area

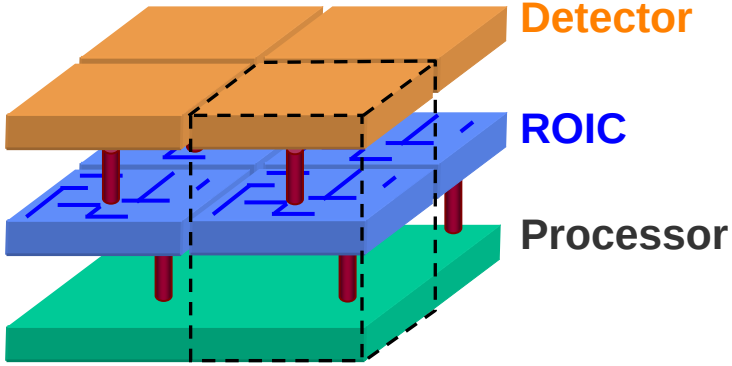
- 3D Vertical Integrated System
  - Fully active sensor area
  - Independent control of substrate materials for each of the tiers
  - Fabrication optimized by layer function
  - Local data processing
  - Increased circuit density due to multiple tiers of electronics
  - 4-side abuttable

- Technology driven by industry
  - Reduce R, L, C for higher speed
  - Reduce chip I/O pads
  - Provide increased functionality
  - Reduce interconnect power, crosstalk

**Conventional MAPS**

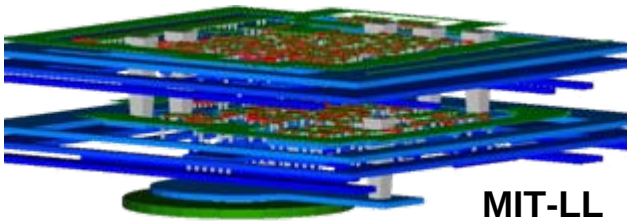



**3-D Pixel**

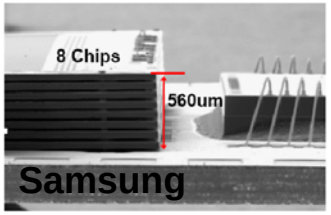


# Industry and 3D Integration

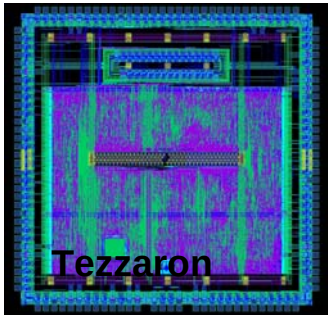
- **Pixel arrays for imaging**
  - **Pixel arrays with sensors and readout are well suited to 3D integration; signal processing can be placed close to the sensor**
- **Memory**
  - **All major memory manufactures are working on 3D memory stacks; lower cost**
- **Microprocessors**
  - **A major bottleneck is access time between CPU and the memory. Memory caches are used as an interface but the area required is significant. 3D will use Logic to Memory, and Logic to Logic stacking**
- **FPGAs**
  - **Wire delays are an inherent problem is 2D FPGAs. 3D integration can improve performance by removing the programmable interconnect from the logic block layer and moving it to another tier.**



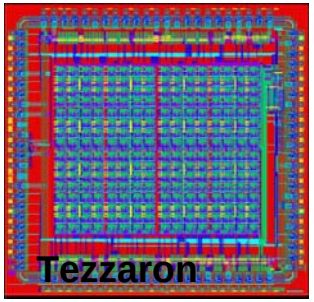

3D Laser Radar Imager




CPU and 220 MHz memory Stack

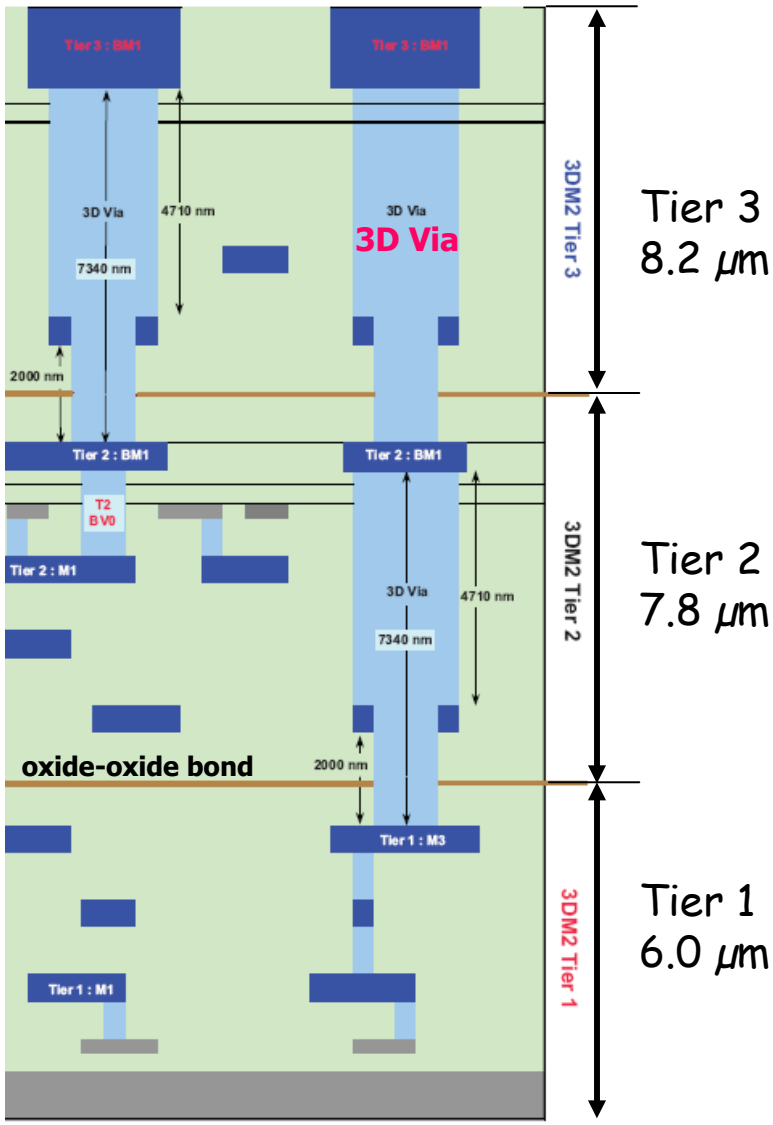



FPGA – 12 vi's per logic block



# 3D Demonstrator Chip

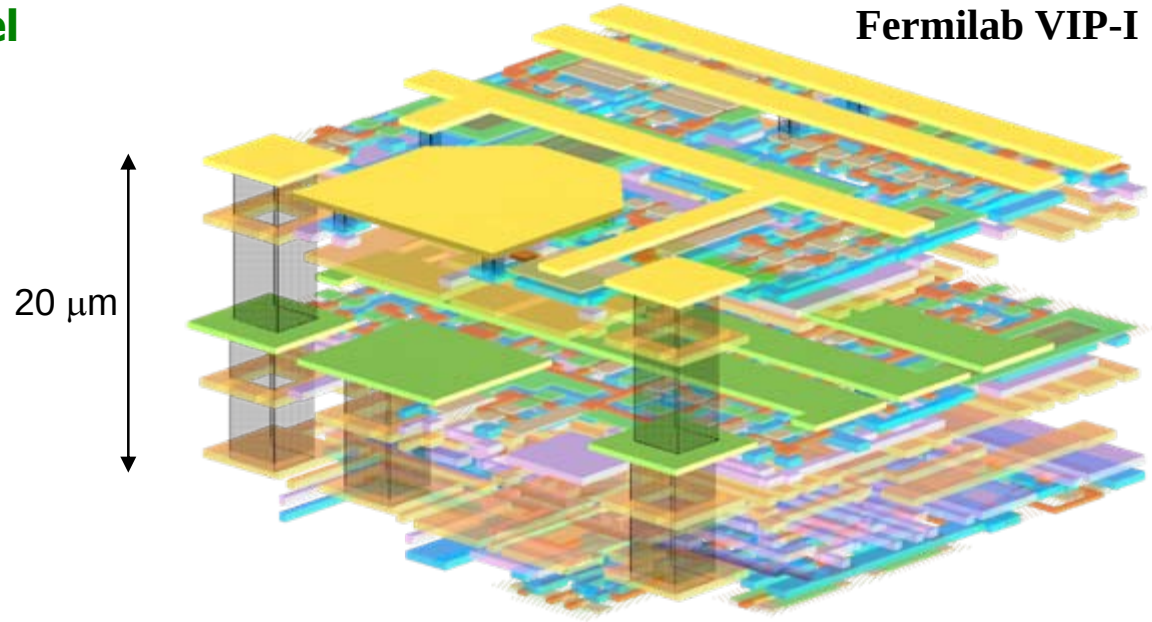
- Fermilab started to actively pursue the 3D technology in early 2006
- MIT Lincoln Laboratories (MIT-LL) had developed the technology that enables 3D integration
  - Demonstrated the 3D technology through fabrication of imaging devices
  - Has infrastructure to allow for 3D Multi-Project Run fabrication
- MIT-LL offers DARPA funded three-tier multi-project run
  - 3D design laid out in MIT-LL 0.18 μm SOI process
    - SOI provides additional advantages: BOX, full isolation, direct via formation, enhanced low-power operation
  - 3 levels of metal in each layer
- Designed Vertical Integrated Pixel (VIP) readout chip for ILC pixel detector
  - Pixel size 20 x 20 μm
  - 64 x 64 pixel array
  - No integrated sensor



# VIP Architecture

- Pixel array 64x64, 20x20 $\mu m^2$ pixels; design for 1000 x 1000 array
- Provides analog and binary readout information
- 5-bit Time stamping of pixel hit (ILC environment)
- Token passing scheme with look-ahead for addressing and to reduce data output (200 ps/cell)
- Sparse readout performed row by row with x- and y-address stored at end of row and column
- Chip divided into 3 tiers
  - ~ 7 $\mu$m / tier
  - 175 transistors / pixel

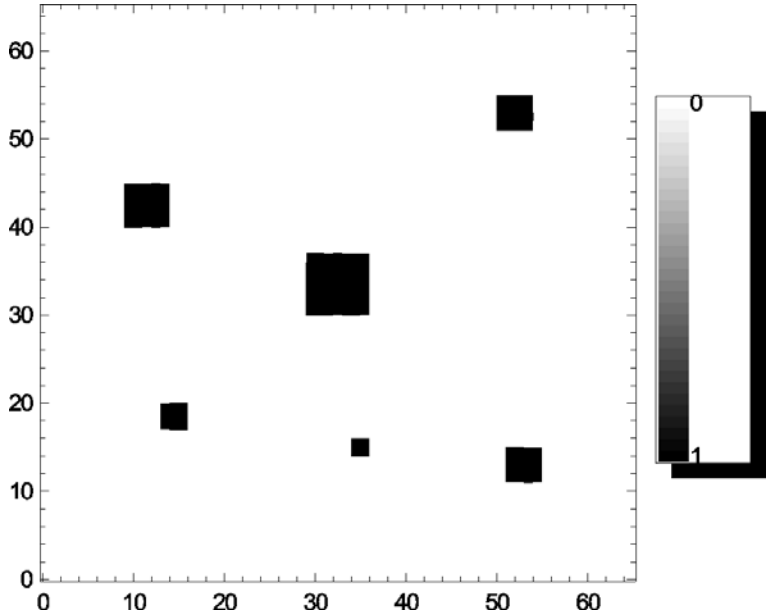
Fermilab VIP-I



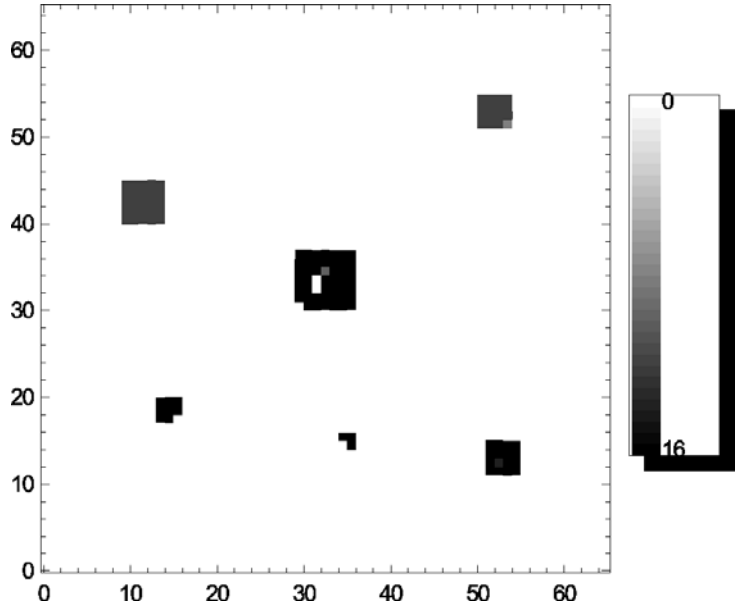
# VIP-1 Chip Test Results

- **VIP-1 chip submitted Oct. 2006; ~20 devices delivered late 2007**
- **Chip works !**
- **Major breakthrough in the development of advanced ASICs and integrated detector systems**

- **Data readout out using data sparsification scheme on full array**




Preselected injection pattern of pixels to the front-end amplifiers

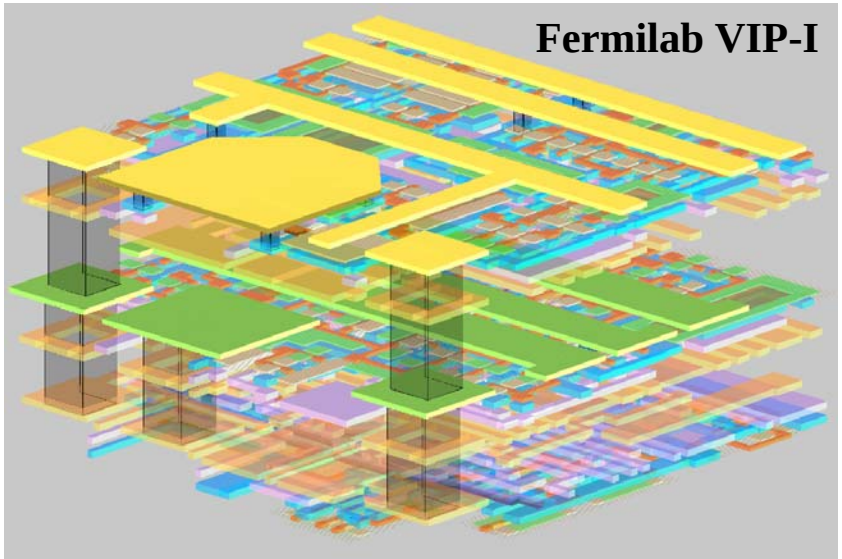



Readout pattern of pixels from the preselected injection pattern reported as hit

# VIP-2a

- **MIT-LL run has been very successful and has provided a proof of principle**
- **Work is proceeding on an improved version of VIP1 to be submitted to MIT-LL on October 13, 2008 (150nm, SOI, 3 tiers): VIP-2a**
  - **Different power and grounding layout**
  - **Redundant vias and larger traces in critical paths**
  - **Added diagnostics**
  - **More bits in digital time stamp (7 bits)**
  - **Redesign of current mirrors**
  - **Removal of dynamic logic due to leakage problems**

- **MIT-LL process does have some shortcomings**
  - **Processing and design problems**
  - **Significant chip-to-chip variations**
  - **Yield is poor, reasons not understood**
  - **Measurements disagree with simulations**
  - **Long turn-around time**
  - **Not a commercial process**



# Tezzaron

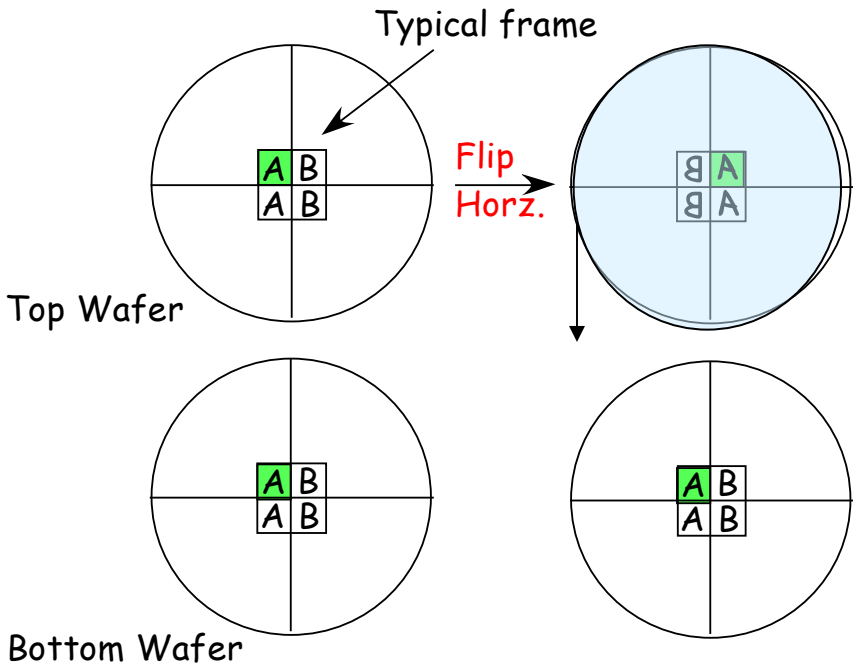
- **Fermilab started an initiative with a local vendor who is one of the leaders in 3D: Tezzaron, based in Naperville (and Singapore)** http://www.tezzaron.com/
- **Tezzaron has fabricated 3D chips for commercial customers**
  - **Memory devices and CMOS sensors**

- **Process Characteristics/Flow**
  - **Wafers with "Via First" process are made at a commercial foundry: Chartered Semiconductor in Singapore**
  - **Wafers bonded in Singapore by Tezzaron**
    - Facility can handle up to 1000 wafers/month
  - **Bonded wafers are finished by Tezzaron**
    - (Bump) Bond pads

- **Potential Advantages**
  - **Existing rules for vias and bonding**
  - **Lower cost and faster turn around**
  - **One stop shopping**
  - **Process is available to customers from all countries**

# Fermilab 3D Multi-Project Run

- **Fermilab will be hosting a 3D multi project run with Tezzaron**
- **There will be only 2 layers of electronics fabricated in the Chartered 130 nm process, using only one set of masks. (Useful reticle size is 16 x 24 mm)**
- **The wafers will be bonded face to face**

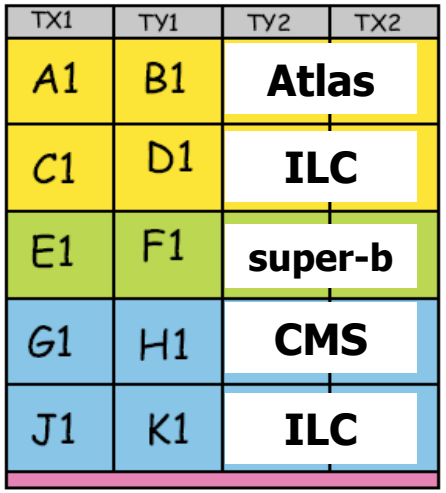



Note: top and bottom wafers are identical.

- **Participants in MPW run:**
  - **Fermilab, Batavia**
  - **University at Bergamo**
  - **University at Pavia**
  - **University at Perugia**
  - **INFN Bologna**
  - **INFN at Pisa**
  - **INFN at Rome**
  - **CPPM, Marseilles**
  - **IPHC, Strasbourg**
  - **IRFU Saclay**
  - **LAL, Orsay**
  - **LPNHE, Paris**
  - **CMP, Grenoble**
- **Discussions with:**
  - **BNL (NSLS)**

# Candidate Projects for 3D MPW Run

- **Possible four-way split of the reticle**
  - **Fermilab**
    - *Redesign of the VIP chip, adopted to 2 tiers VIP-2b*
    - *New 3D chip to explore the advantages of 3D for the sCMS pixel detector (LHC)*
  - **France**
    - *CPPM has expressed interest in converting the current 0.25 um ATLAS pixel design to a 3D structure with 2 tiers in the Chartered 130 nm process (LHC)*
    - *Strasbourg proposes to work with Fermilab to develop a simple 3D MAPS device with 7 bits of time stamping (ILC)*
  - **Italy**
    - *Bergamo proposes to work with Fermilab to develop a 3D version of a MAPS device using deep n-well with sparsification and time stamping (ILC/Super b-factory)*




Frame layout

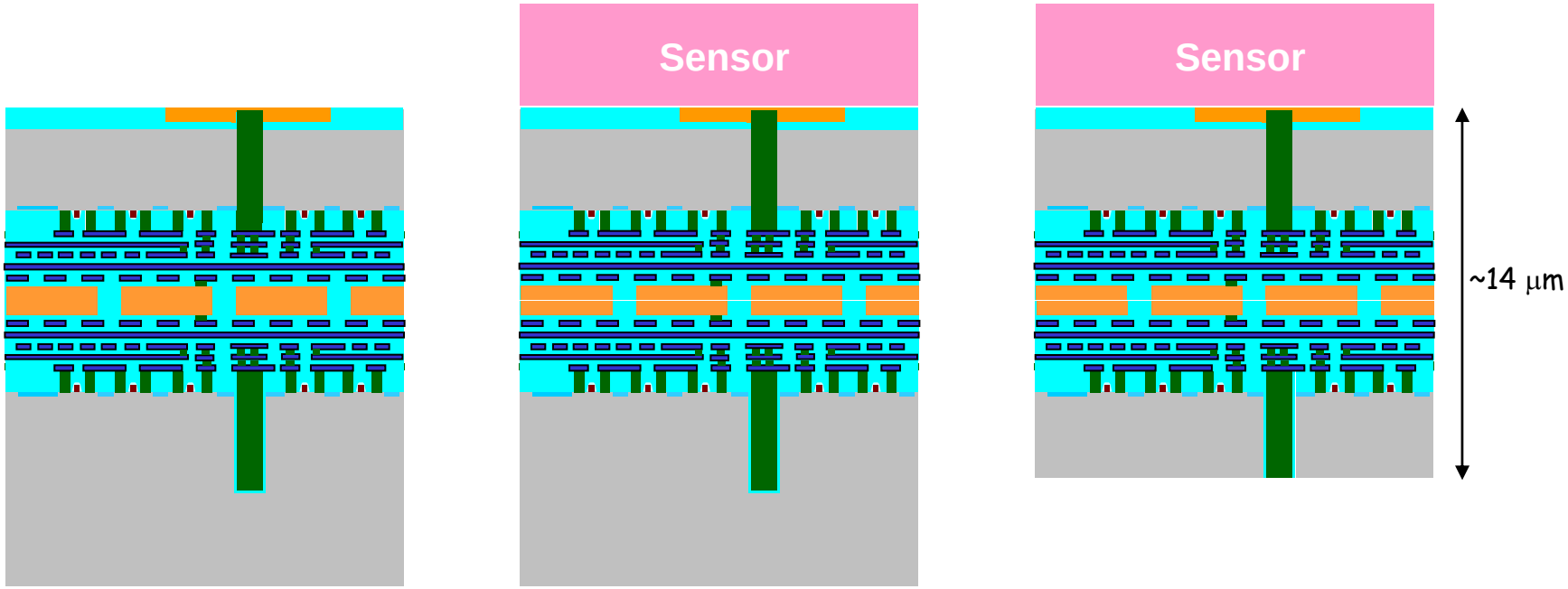
Yellow = France
Green = Italy
Blue = USA
Magenta = alignment
Grey = test chips

- **Truly generic detector development with international base using standard commercial CMOS processing**

# Integrating Detectors

- **Ultimate goal is to have integrated unit of front-end electronics and thin (~50μm thick) fully depleted detectors with very fine pitch**

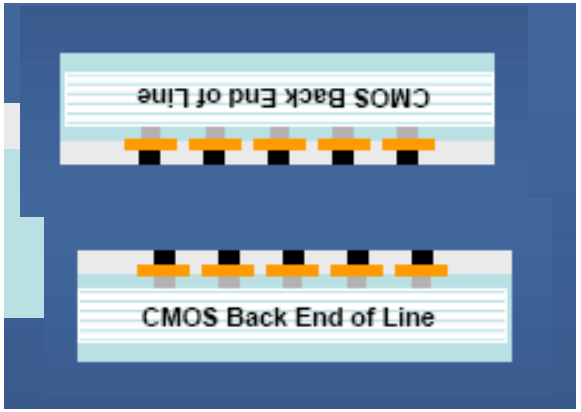
- **Two tier stack -> Bond sensor -> Backgrind**




- **How to bond sensor to readout electronics at 20 μm pitch at low mass?**

# Direct Bond Interconnect

- **Direct Bond Interconnect (DBI) process (Ziptronix, NC)**
  - **Planarization of wafers**
  - **Oxide bonding at room temperature**
  - **Metal connection by thermo-compression.**
  - **Robust mechanical connection –sensor/IC**
  - **Can be ground and thinned after bonding.**
  - **3 µm pitch achieved.**
  - **Die to wafer, wafer to wafer**
- **Readout ICs can be placed onto sensor wafers with 10 µm gaps**
- **Pave the way towards thinned full coverage detector planes**
- **We also explored CuSn and SnPb bump bonds**




**DBI:**

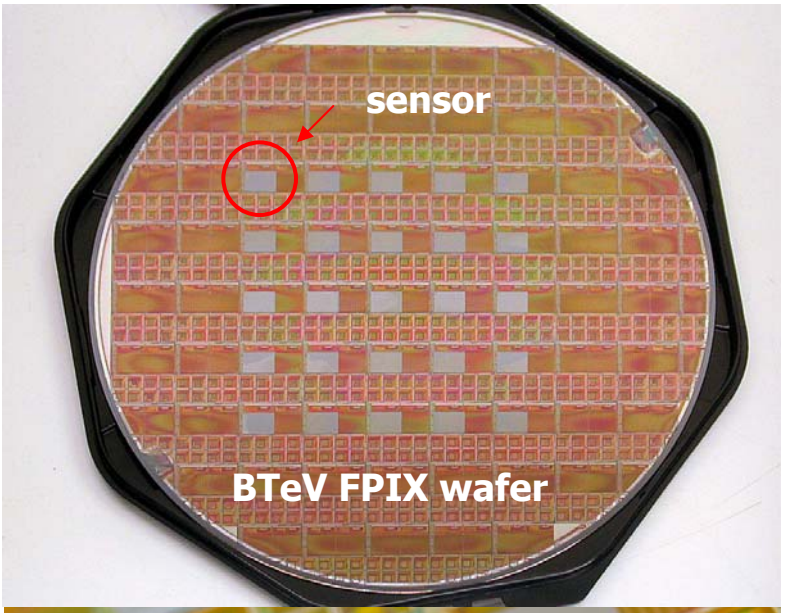
- **Plate DBI (magic) metal**
- **Deposit oxide, terminate surface with amine group**
- **Bring surfaces in contact**
  - $Si–NH_2 + Si–NH_2 \rightarrow Si\text{-}N\text{-}N\text{-}Si + 2H_2$
  - Bonding occurs at RT
  - Bond strength increase with t
- **After oxide bond is strong enough, wafers are heated to form thermo compression bond between Magic Metal implants.**

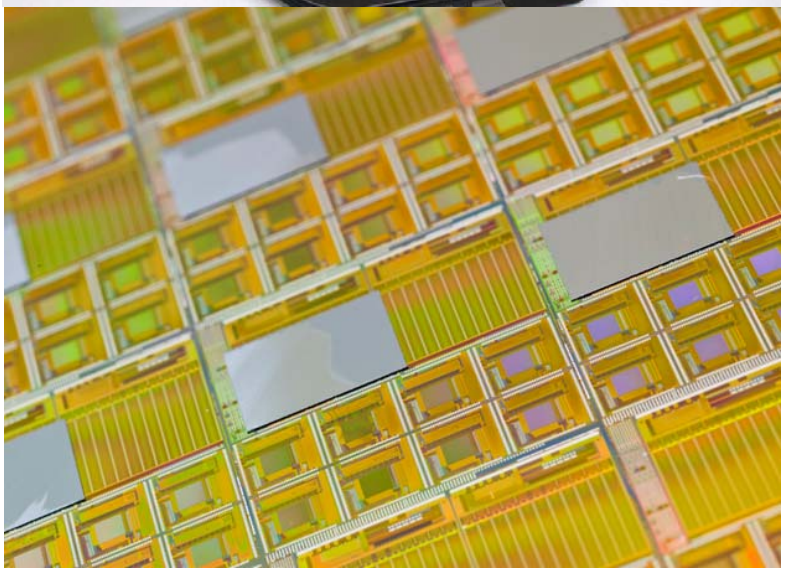
# DBI Prototype Sensor and Readout

- **Edgeless trenched pixel sensors:**
  - **p+ diodes on n-bulk (ρ=5kΩ·cm);**
  - **50 µm deep n++ trench at the edge**
  - **Masks designed at Fermilab**
  - **Fabricated by MIT-Lincoln Lab**

- **BTeV FPIX2.1 readout chips**
  - **22x128 pixel cells of 50x400 µm;**
  - **Designed for e-signals (3 bits ADC), can work with small hole signals**

- **Above two items DBI bonded and then sensor thinned to 100 µm**



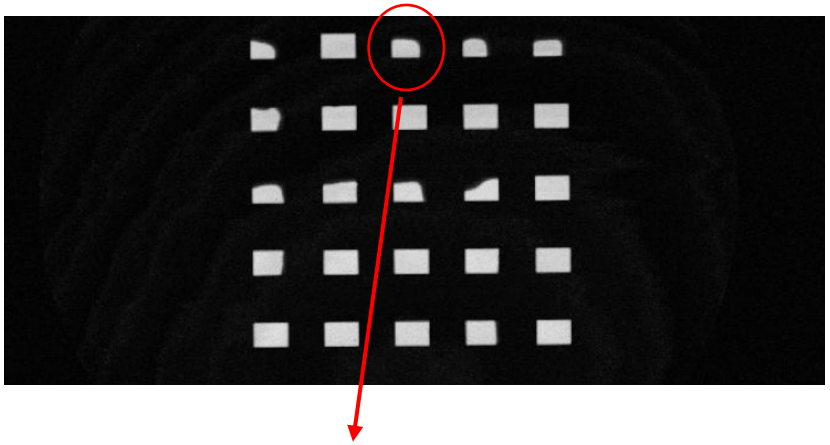



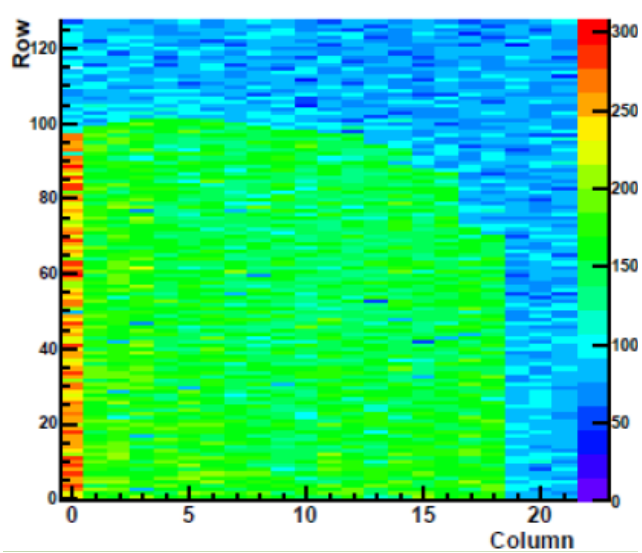
# DBI Performance

- 50 MIT-LL sensors DBI bonded to two FPIX wafers by Ziptronix and thinned to 100 µm after bonding

- 30 good devices in the end
  - 16 with bond voids indicated by Scanning Acoustic Microscope . Normal yield is claimed to be 80-90%

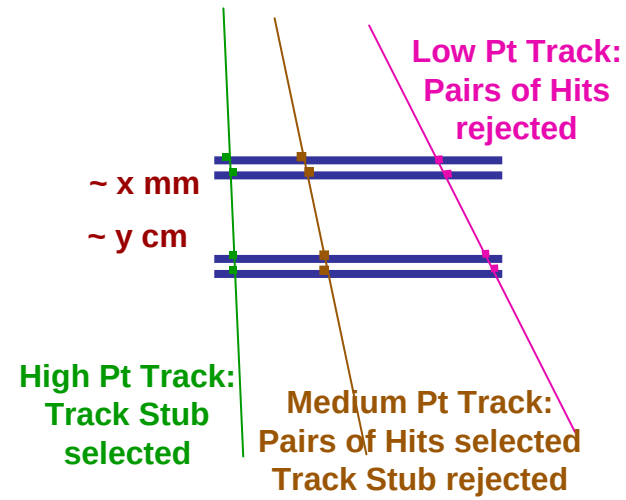
- Voids due to warp and planarization
  - Pedestal distribution of pixel matrix readout indicating the "void"

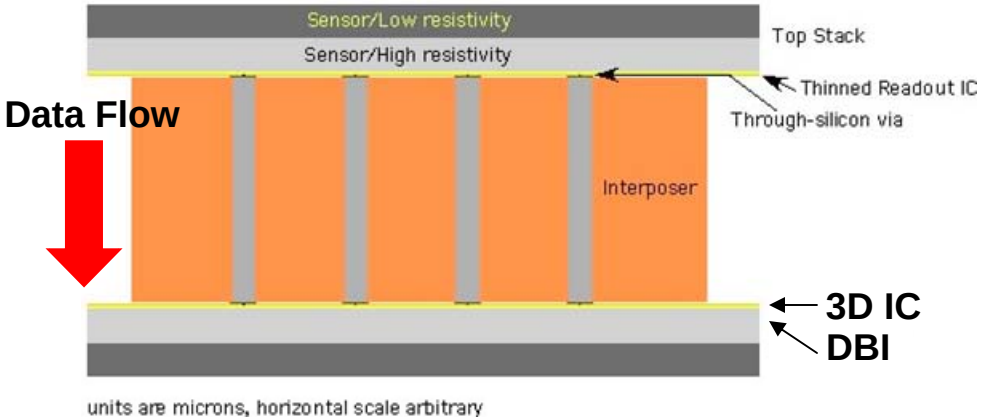




# Example: Energy Frontier

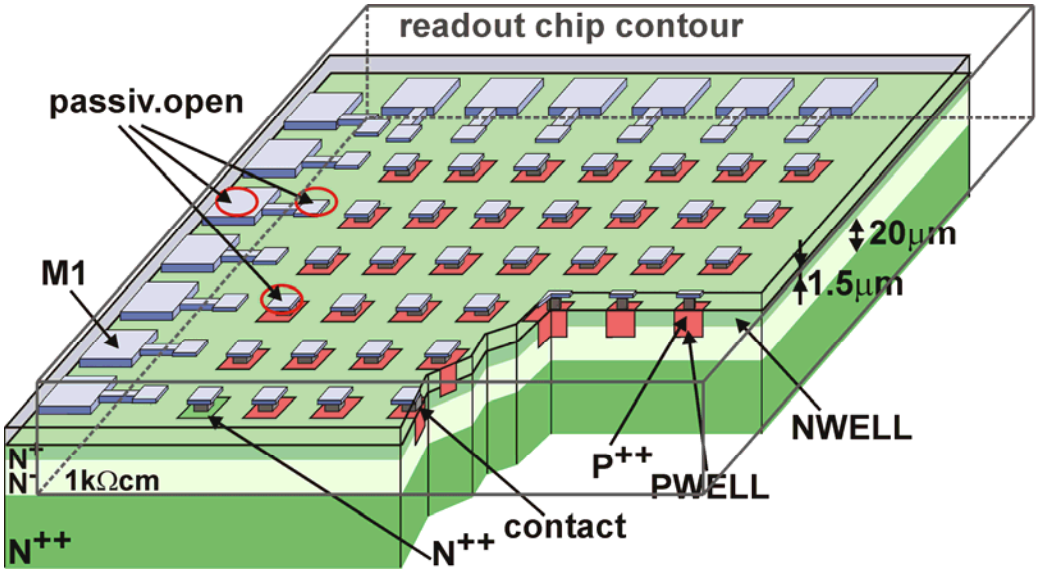
- sLHC: from $10^{34}cm^{-2}s^{-1} \rightarrow 10^{35}cm^{-2}s^{-1}$
  - At least 10 times higher event rate, 10–20 times higher occupancy
  - Cannot sacrifice efficiency and background rejection
- Move tracker information to 1st Level trigger (CMS) for
  - Local Occupancy Reduction
  - Local $p_T$ Discrimination
- Possible pair of sensor planes for local $p_T$ measurement
  - High $p_T$ tracks point towards the origin
  - low $p_T$ tracks point away from the origin
- Data flow is "vertical" !



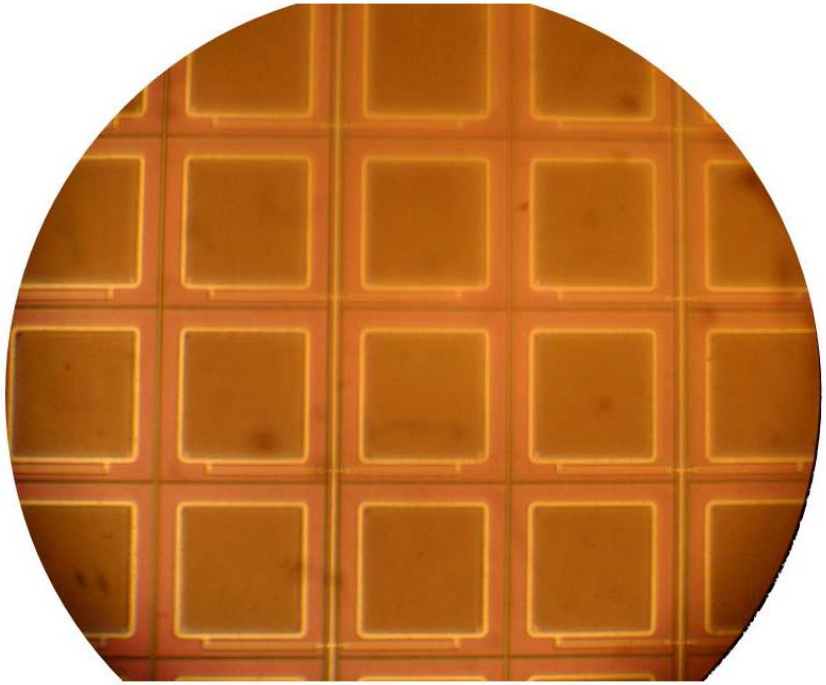



# Example: Imaging

- In collaboration with BNL, evaluating application for X-ray correlation spectroscopy
  - calculate autocorrelation function per pixel
- Current design
  - 100x100 $\mu m^2$ pixels
  - $\gamma$ flux: 1000 $\gamma$/pixel/s
  - time stamping of ~10 $\mu$s
- Estimation for logic density of ~1500 transistors/pixel
  - Two tier 3D chip design
- Possible application at APS?



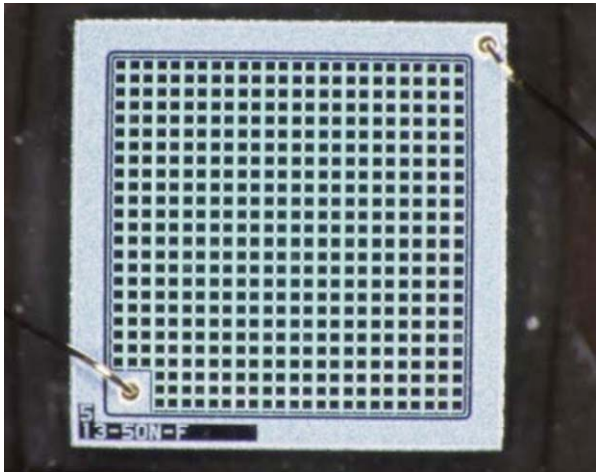

- Proposal
  - Sensor fabricated at BNL
  - 3D ASIC developed at Fermilab
    - Two tiers: analogue and digital
      - front-end with per pixel threshold
      - sparsified readout layer
  - DBI bond to sensor

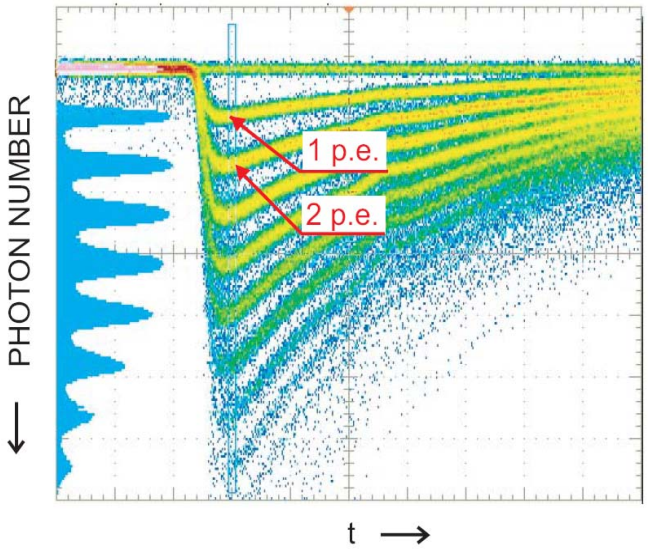


# Pixelized Photon Detectors

# PPD

- **Pixelized Photon Detector (PPD) is avalanche photodiode operating in Geiger-mode**
  - **Array of pixels connected to a single output**
  - **Signal = Sum of all cells fired**
    - Very compact, High PDE (15~20% for 1600 pix)
    - Low bias voltage operation
    - High thermal noise rate, x-talk and after-pulsing
    - Insensitive to magnetic field
  - **Portrayed as potential replacement of PMT**



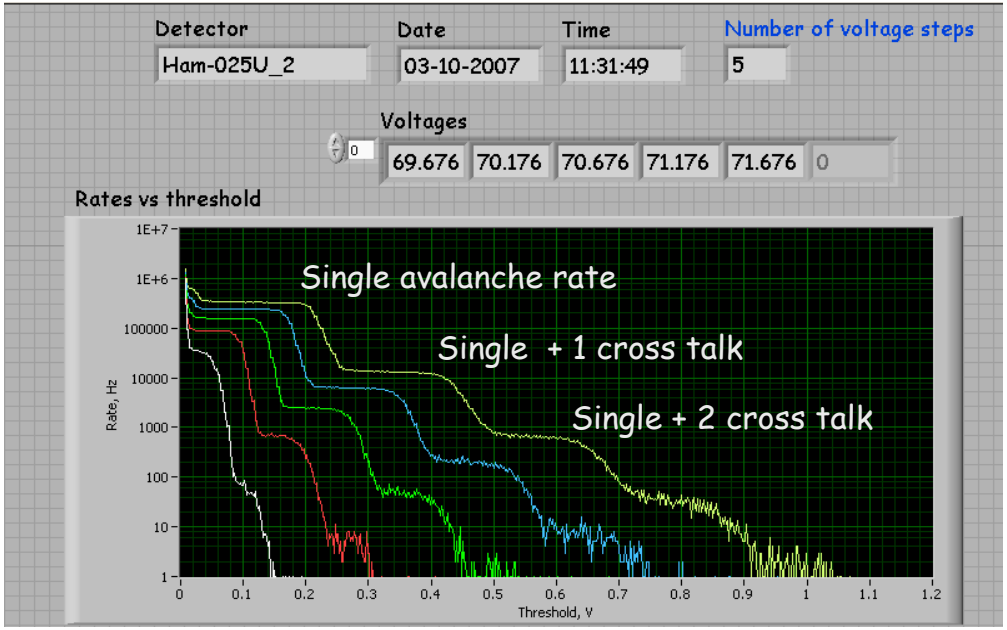



- PPD is generic name; device also known as
  - SiPM (Silicon Photo-Multiplier)
  - MRS-APD (Metal Resistive Semiconductor APD)
  - SiPM (Silicon Photo-Multiplier)
  - MPGM-APD (Multi-Pixel Geiger-Mode APD)
  - AMPD (Avalanche Micro-pixel Photo-Diode)
  - SSPM (Solid State Photo-Multiplier)
  - GM-APD (Geiger-Mode APD)
  - SPAD (Single Photon Avalanche Diode)
  - MPPC (Multi-Pixel Photon Counter)

- **It is an enabling technology for many applications**

# PPD Characterization

- **Environment for characterization of PPDs set up**
  - **Measurements "in the dark"**
  - **Characterization of response to a calibrated light pulse**
  - **Microscopic studies of the photo-detector**




- **Try to relate some of the characteristics to the detector design and construction and provide feedback to vendor**

- **Broad active research area:**
  - **Extended blue sensitivity (Čerenkov light, dual readout calorimetry)**
  - **Increased PDE ( muon detectors)**
  - **Reduced crosstalk (improved noise factor)**
  - **Improved timing (PET)**
  - **Large area**
  - **Increased dynamic range (Calorimeters)**
  - **Lower cost**

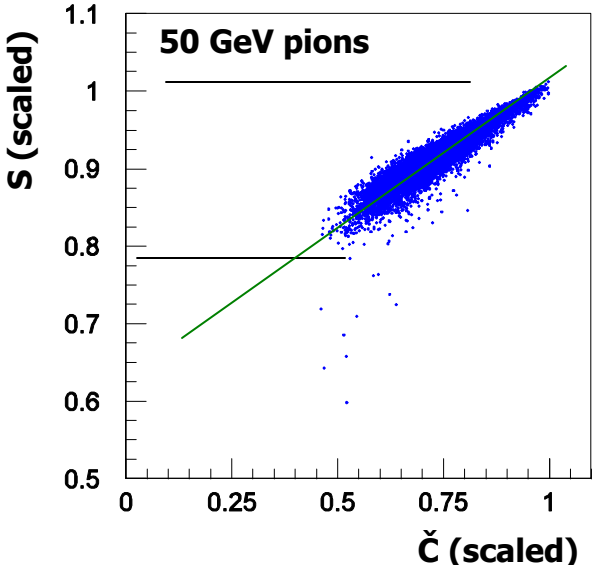
# Dual Readout Calorimetry

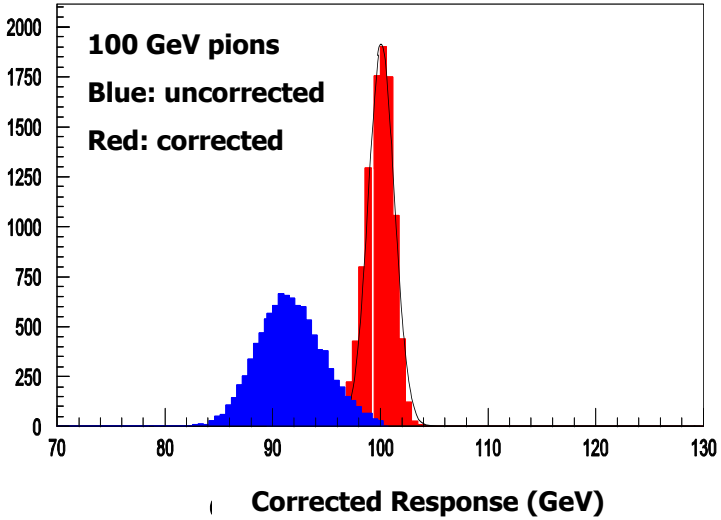
- **Dual-readout calorimetry: measure every shower twice**
  - **Scintillation light: from all charged particles**
  - **Čerenkov light: $\beta$=1 particles, mainly EM**

- **Correct on a shower-by-shower basis using the correlation of the total observed ionization (S) and Cherenkov (Č) light**

- **Monte Carlo shows:**
  - **Gaussian response**
  - **Energy resolution (0.2-0.25)/√E**
  - **No constant term up to 200 GeV**

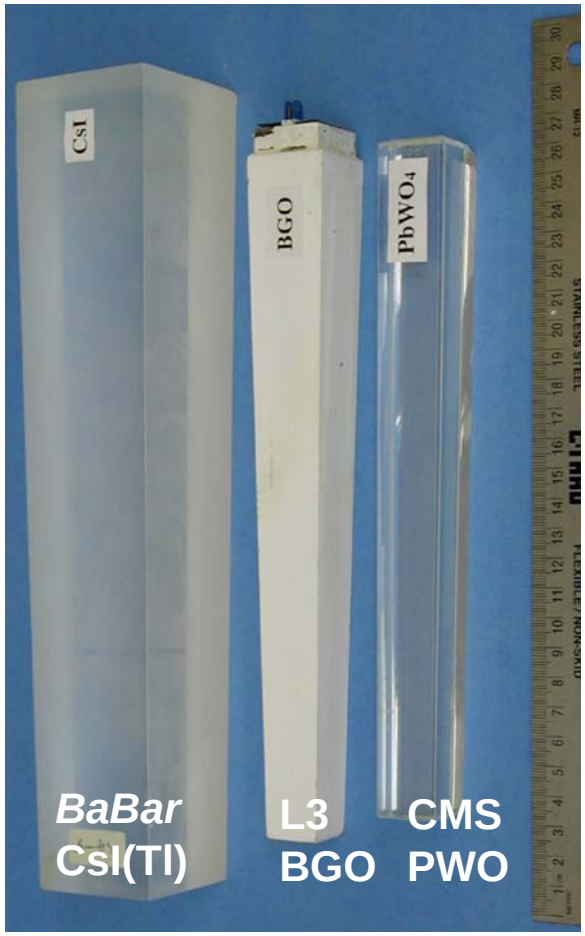
- **Why no total absorption calorimetry to date ?**
  - **Too big to be practical: too expensive**
  - **Difficulty in light collection and signal readout (especially in high B-field)**
  - **No suitable crystals**
  - **Poor energy resolution**



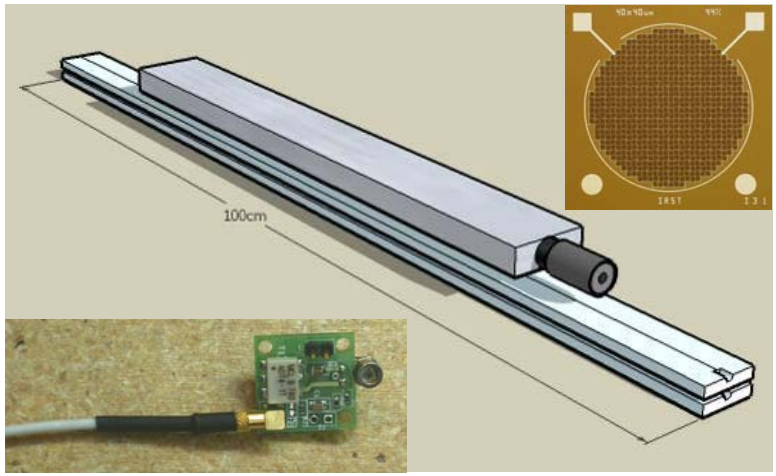
# Total Absorption Dual Readout Calorimetry

- Objections to this technology are no longer valid thanks to a combination of technological breakthroughs
  - Heavy scintillating crystals
  - Silicon photo-detectors
- Crystals
  - Develop crystals suitable for scintillation – Čerenkov light separation
- Light collection with PPDs
  - Separation Č-light and scintillation light
  - Yield, wavelength,
  - uniformity, # SiPM
  - Simulation of scintillation and Č-light
- Initiating R&D program to study viability of concept for collider experiment
  - Beam tests of small prototypes moving towards 1 $m^3$

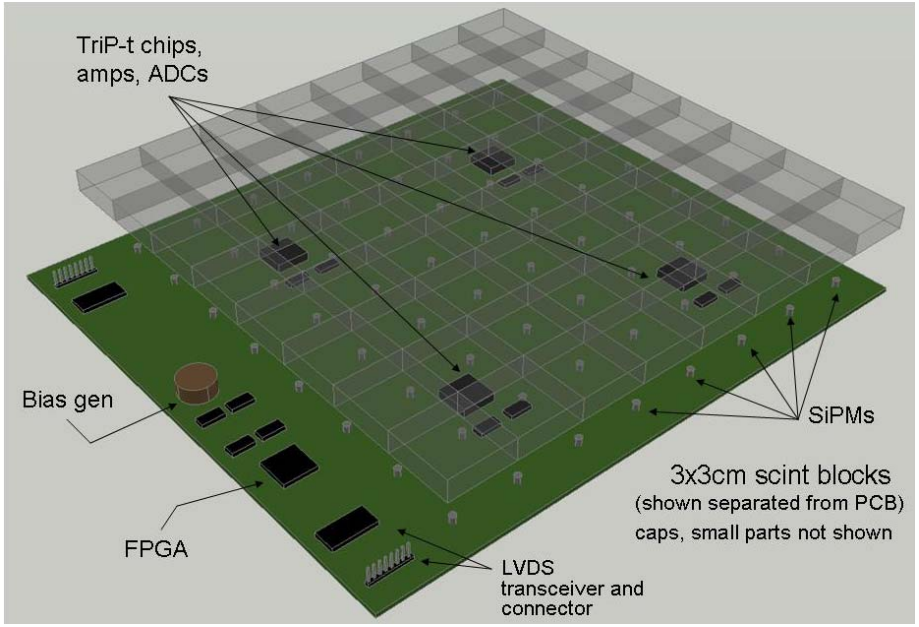


# Scintillator Readout

- **Readout of scintillator strips with WLS fiber 1.2mm**
  - **Bench tests with single trigger paddle with PMT placed above**
  - **Beam tests**
- **Devices with geometry optimized for fiber coupling tested**
  - **Geometry: circular**
  - **diameter: 1.2 mm**



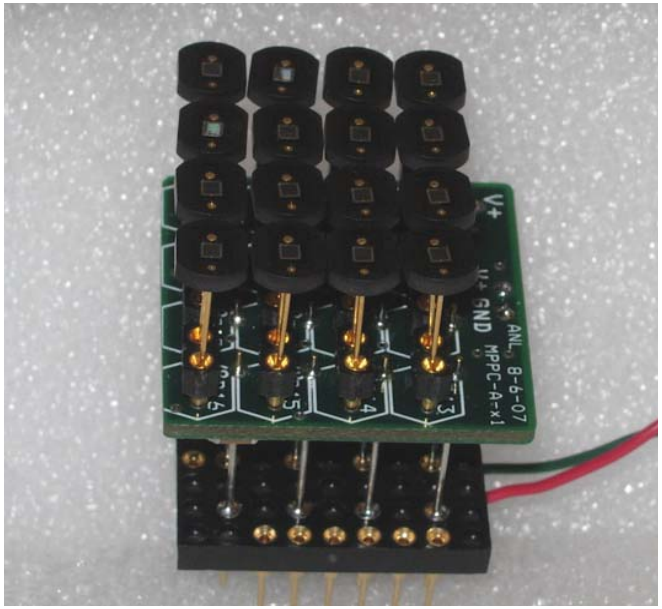

- **Developed integrated readout system**
  - **64 channel**
  - **Amplitude and timestamp**
  - **4 TriP-t chips, AC coupled**
  - **2 TriP-t channels per MPPC for extended dynamic range**
  - **16 layer board**



# Future Directions

- **CMS has proposal to replace current HCAL HPD readout with MPPCs**

- **Interest within the community to employ MPPCs in particle-astrophysics experiments**
  - **MAGIC telescope in the Canary Islands**
  - **Focal Plane Detectors for the Advanced Gamma-Ray Imaging System (AGIS)**
    - Argonne project




- **Interest to develop various ASICs for various applications**
  - **Multi-GHz waveform digitizer ASIC**
  - **Dual-readout**
  - **Integrated readout layer for calorimetry**
  - **…**

# Concluding Remarks

- **Fermilab is pursuing two promising, though challenging, technologies**
  - **3D Vertical Integration**
  - **Multi-Pixel Photon Counters**
- **Working to enable these technologies for future detectors**
- **The 3D MPW runs, sponsored by Fermilab, and the direct bonding R&D, open up the 3D technology to any collaborator**

- **Both technologies have an incredible broad range of application**

- **Opportunities for collaboration are only limited by our imagination (and resources) !**